DEVELOPMENT DESIGN OF BUILT-IN SELF-TEST FOR LSI CIRCUITS: TEST PATTERN GENERATION, OSCILLATION-BASED TESTING, AND CALIBRATION TECHNIQUE

論 文 内 容 の 要 旨

Rising of the transistor technology has evolved the electronic industry substantially. From the visible with normal size, nowadays, modern electronics device is implemented and operated on a Nano-scale and tends to reducing every year. Meanwhile, the size of electronics device is decreasing, the quality is approaching to the opposite direction. In other words, the quantity and diversity of transistors is increasing, and become a high complex network. This situation has led to a great demand of reliable System on Chip (SoC). Testing such devices before a manufacturing process has become a crucial issue. Although, an off-chip testing with automated test equipment has been used commercially, it requires costly measurements with long-time process. For contemporary Large Scale Integrated (LSI) circuits, automated on-chip testing has gained a great attention on either research or industrial area. Built-in Self-Test (BIST) and Design-for-Test (DFT) are the major strategies, which have been widely accepted by meaning of improving observability and controllability during the testing process.

This dissertation presents effective designs of BIST systems for a defect-oriented testing in analog and mixed-signals LSI circuits. Fully on-chip circuitry, high faults detection against catastrophic and parametric variation, and low performance degradation are the objectives of this work. The proposed methods focus on the principal of BIST, i.e. test stimulus generation, test control, and test response analysis. Such methods are implemented for essential LSI building blocks, ranging from transistor-only circuitry such as an operational amplifier (Op Amp) and comparator, to an analog low-pass filter, as well as a large-scale mixed-signals system. The major contributions of this dissertation can be classified into three approaches. The first approach is designing a high-speed random signals generator for the source of test stimulus generation. The second approach is the demonstration of an oscillation-based testing in order to eliminate the large stimulus generator. The third approach involves the combination of self-test and calibration technique for each circuit elements.

The proposed methods of this dissertation begins with a high-data-rate true random bit generator for a cost-effective and high-speed test stimulus generation. This method is a full-custom design of chaos-based True Random-Bit Generator (TRBG) implemented on a 0.18-μm CMOS technology with unique composition of three major components, i.e. (i) chaotic jerk oscillator, (ii) $\Delta\sum$ modulator, and (iii) simple pre/post-processing. A chaotic jerk oscillator is a deterministic source of randomness that potentially offers robust and highly random chaotic signals and exhibits a distinctive property of smoothly balanced-to-unbalanced alternation of double-scroll attractors. The continuous-time 2^{nd}-order $\Delta\sum$ modulator is introduced as a mixed-signal interface in order to increase a resolution of random bit sequences while no extra clock is required. The $\Delta\sum$ modulator is constructed mainly by a folded-cascode amplifier with sufficient gain and phase margin of 64dB and 83^{o}, respectively, and a high-speed comparator with a time constant of 2.7ns. An uncomplicated structure of shift-registers is realized as a post-processing process. The bit sequence of the proposed TRBG successfully passes all statistical tests of NIST SP800-22 test suite, and the ultimate output

bit rate is 50Mbps. The physical layout of a chip area is 212.8×177.11 mm^2 and the DC power dissipation is 1.32mW using a 1.8-V single supply voltage.

The second method, a simple design-for-testability (DFT) technique for analog second-order $\Delta\sum$ modulators is described. The structure of circuit-under-test is modified and operated as two symmetric structure circuits in the test mode. Different DC offset and simple digital counters are connected to the input and output of the circuit in order to reduce testing process complications and costs, with the modulator operated as a simple signal generator in the test mode. A demonstration of the testing process is performed through the switched-capacitor second-order $\Delta\sum$ modulator, which achieves several advantages, including low cost, high-speed testing, and high fault coverage, and covers parametric failure. Also, the overall system was fully fabricated in 0.18-μm CMOS standard technology without the need for additional digital processing units.

Additionally, a phase difference analysis technique is presented in the third method, which is sensitive to the parametric deviations and allows a tolerance band of passive analog components. Test operations can be simply achieved by comparing the phase difference between a reference clock signal and a reconfigured circuit-under-test (CUT) as an oscillator. The difference of phase characteristics between the two signals can be utilized as an indicator for a fault signature, which can be characterized by a compact digital circuit comprising a counter and logic components. Simulation of faults detection reveals a high faults coverage, high-speed testing, and tolerance band controllability. The proposed technique has offered a fully on-chip BIST in 0.18-μm CMOS standard technology with no external test equipment required.

Furthermore, the integration of BIST and calibration technique is proposed in the fourth method. simple circuitry such as a frequency-to-DC circuit, a windows comparator, and basic logic elements are utilized as the faults detection circuits. The calibration system is additionally implemented through the resistor array with a feedback network in order to adjust the gain value of the CUT. Simulation results show the capable of faults detection involves catastrophic and parametric variation. Moreover, the signals-to-noise ratio (SNR) of the CUT can be preserved at the acceptable level against the failure circuitry.