A Fault Signature Characterization Based Analog Circuit Testing Scheme and the Extension of IEEE 1149.4 Standard

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SUMMARY   An analog circuit testing scheme is presented. The testing technique is a sinusoidal fault signature characterization, involving the measurement of DC offset, amplitude, frequency and phase shift, and the realization of two crossing level voltages. The testing system is an extension of the IEEE 1149.4 standard through the modification of an analog boundary module, affording functionalities for both on-chip testing capability, and accessibility to internal components for off-chip testing. A demonstrating circuit-under-test, a 4th-order Gm-C low-pass filter, and the proposed analog testing scheme are implemented in a physical level using 0.18-μm CMOS technology, and simulated using Hspice. Both catastrophic and parametric faults are potentially detectable at the minimum parameter variation of 0.5%. The fault coverage associated with CMOS transconductance operational amplifiers and capacitors are at 94.16% and 100%, respectively. This work offers the enhancement of standardizing test approach, which reduces the complexity of testing circuit and provides nonintrusive analog circuit testing.

key words: analog circuit testing, circuit-under-test, IEEE 1149.4 standard, fault signature characterization

1. Introduction

The emergence of modern system-on-chip (SOC) technology has led to a continuous increase in quantity and diversity of integrated components. Consequently, testing in both product development and mass-production phases of SOC has become more challenging, and now constitutes a major portion of overall cost. On-chip testability features have received considerable attention as a means of reducing testing time and eliminating the necessity for automatic testing equipments (ATE). Several early on-chip testing techniques have been applied successfully in digital circuits in which single stuck-fault models are commonly utilized, and test-pattern algorithms have been developed comprehensively [1]. However, on-chip testing techniques in analog mixed-signal circuits are relatively complicated owing to performance degradation and indecipherable fault models. Accordingly, the testing design approaches taken in analog mixed-signal systems have recently been of much interest to research efforts. The development of testing design approaches can be considered in two aspects, i.e. testing technique and testing system implementation.

One design aspect is the testing technique, which relates to fault signature detection methods, and can be classified into either current or voltage sensing techniques. The current sensing techniques, commonly referred to as I_{DDQ} current sensors [2]–[4], are relatively simple and suitable for detecting bridging faults. However, a circuit-under-test (CUT) may suffer from power supply variations, and inappropriate setting of reference currents may also affect the precision of fault detection owing to a wide range of faulty currents [5]. On the other hand, the voltage sensing techniques include two main categories; the DC voltage sensing such as the built-in voltage sensor [6] and the V_{DDQ} scheme [7], and the AC output response characterizations such as sub-sampling [8], absolute value difference [9], on-chip spectrum analyzer [10], and $\Sigma\Delta$ modulator [11]. These voltage-sensing techniques support non-intrusive implementation, and offer suitability for most types of circuits as only output signals are monitored with no modification in CUTs. Nevertheless, an input stimulus is necessary and hard-to-detect faults are imperceptible at output voltages.

Another design aspect is the testing system implementation of the testing techniques mentioned earlier, involving off-chip and on-chip realizations. The techniques in [2]–[7] are based on design-for-testability (DFT) in which fault signature sensing circuitries are realized on-chip, but fault detection is accomplished off-chip using external measurement devices or digital signal processing. In addition, the IEEE 1149.4 standard provides the internal circuit accessibility for enhancing the off-chip testing through analog access ports and internal test buses. On the other hand, the testing techniques in [8]–[11] are based on built-in self test (BIST), in which both stimulus generation and response verification are accomplished entirely on-chip through built-in hardware. Despite the fact that no external measurement devices are needed for BIST, large area overhead encountered in BIST for the registration of test pattern generation and fault-free bit streams presents a major difficulty.

Consideration of these two design aspects points to a demand for testing techniques with acceptable fault coverage and low performance penalties, implemented in a system that offers both on-chip and off-chip testing for pre-screening of defective chips and for high-quality testing of some critical analog circuits, respectively. Therefore, this paper presents an analog circuit testing scheme. The proposed testing technique is relatively simple based on a fault signature characterization. The testing system implementation, providing both on-chip and off-chip testing, is standardized through an extension of the IEEE 1149.4 mixed-

signal test bus standard by modifying an analog boundary module, and utilizing all existing facilities.

This paper is organized into seven sections as follows. Section 2 provides the background of existing and previous extensions of the IEEE 1149.4 standard. Section 3 proposes the test strategy and fault signature characterization technique. Section 4 subsequently shows the system implementation of the proposed testing technique through the extension of the IEEE 1149.4 standard. As for example, Sect. 5 describes fault models and demonstrates a CUT. Section 6 shows the simulation results and discussion. Conclusion is finally provided in Sect. 7.

2. Existing and Previous Extensions of IEEE 1149.4 Standard

The IEEE 1149.4 mixed-signal test bus standard has been developed for testability enhancements of analog mixed-signal circuits by facilitating two analog access ports and on-chip test buses. Standardizing tests using the IEEE 1149.4 standard resolve the limitation of physical access to internal test points, and interconnecting tests are also applicable. Figure 1 shows the block diagram of the simplified architecture of the IEEE 1149.4 standard. This architecture affords internal components for testing in both digital and analog circuits, comprising a digital boundary module (DBM), analog boundary module (ABM), test bus interface circuit (TBIC), and control circuitries.

As illustrated in Fig. 1, the DBMs scan targeting digital circuits, and shift test data through a serial interface. These DBMs are generally enclosed in digital core circuits and located at input pin (IP), output pin (IP), input and output interfaces to D/A and A/D converters (OI and II). The ABMs provide internal bus connections to each particular CUT. The TBIC conveys input and output analog test signals to ABMs via two analog internal buses (AB1 and AB2), and offers functions for interconnect testing. The control circuitries, consisting of shift registers and decoding logics, control the operation of overall test systems through the four major control signals: test-data-in (TDI), test-data-out (TDO), test-clock (TCK), and test-mode-select (TMS).

Figure 2 shows the circuit configurations of two major blocks, including (a) ABM and (b) TBIC, in the IEEE 1149.4 standard, particularly for testing in analog mixed-signal systems. As shown in Fig. 2 (a), the ABM, comprising a voltage comparator (1-bit digitizer) and six switches. The switch S_D is used for disconnecting the ABM from CUT. The switches S_{B1} and S_{B2} control the connection to the internal analog test buses AB1 and AB2, respectively. The switches S_H and S_L are associated with connections to the voltages V_H and V_L, which perform as standard DC voltage of logical values.

This ABM is capable of two modes of operations, i.e. digital and analog modes. In digital mode, the input is initially digitized by the comparator, and then preloaded in control registers (CRs). The output captured from the comparator is re-loaded into CRs and the decoding logic de-
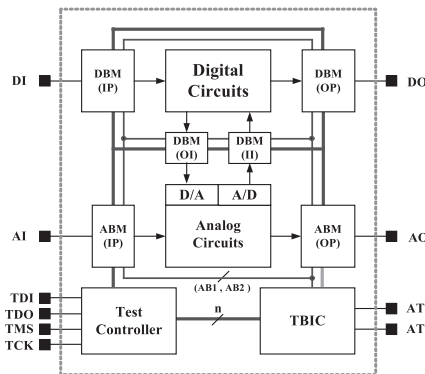

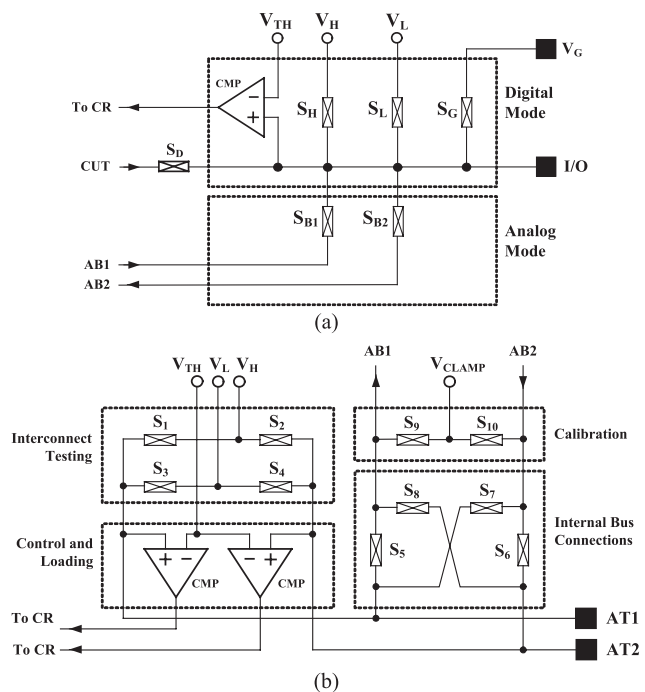**Fig. 1** The block diagram of the simplified architecture of IEEE 1149.4 mixed-signal test bust standard.

Fig. 2 The circuit configurations of two major blocks in the IEEE 1149.4 standard for test accessibility to analog mixed-signal systems; (a) ABM, (b) TBIC.

cides output logics for reporting the test results. In analog mode, an input signal stimulus is sourced via port AT_1 and an output response is provided at port AT_2. In addition, the output response also forms a current return to the ground voltage V_G through the on-resistance of the switch S_G. Fault detection of analog response is accomplished externally through measurement devices such as interfacing testing chips or ATEs. As shown in Fig. 2 (b), the TBIC provides interconnect testing between chips by means of the switches S_1 to S_4, associating with voltages V_H and V_L. Selection of internal bus connections of each analog CUT is accomplished through the switches S_5 to S_8. Calibration of internal bus voltages is also available through the clamp voltage V_{CLAMP}, connecting to the switches S_9 and S_{10}. Additionally, two comparators are employed for controlling the

switch network, and loading signals to the scan paths.

Despite the fact that these existing ABM and TBIC potentially enable the accessibility to internal nodes for EXTEST, several restrictions in analog mixed-signal testing still remain, involving the requirement for duplicated ABMs at all pins, the lack of multiple pin accessibility at one time, and particularly the lack of INTEST capability. Consequently, the extensions to IEEE 1149.4 standard have recently been proposed as solutions for these restrictions. The bridge-for-testability technique [12] was developed for reducing the number of duplicated ABMs. The modified ABM in [13] provides the multiple pin accessibility as well as INTEST capability, specifically for bridging fault testing. It has also been reported that the output of built-in V_{DDQ} and I_{DDQ} monitoring can be scanned out in compliant with the IEEE 1149.4 standard [7]. However, no complete parametric and dynamic INTEST capability with increased observability for both AC and DC fault signatures has been investigated. Consequently, this work aims to resolve this restriction through the extension of the IEEE 1149.4 architecture, and find a suitable testing circuit that can exploit existing facilities including DC voltages, internal test buses and access ports.

3. Proposed Test Strategy and Fault Signature Characterization Technique

3.1 Test Strategy

Figure 3 shows the basic approach block diagram of the proposed testing scheme through the extension of the IEEE 1149.4 standard architecture. Unlike other approaches in which testing circuits are separated from the ABM, it is seen in Fig. 3 that the testing circuit is included in the output ABM, generalizing the design of testing circuits and offering full test functionality with versatility for all types CUTs. In normal operation mode, the CUT obtains the primary input signal $v_{ip}(t)$, and provides the primary output signal $v_{op}(t)$. In test mode, the test signal generator provides two signals, i.e. a test stimulus signal denoted as $v_i(t)$ and a fault-free signal denoted as $v_e(t)$, easing the need for extra area for the registration of test pattern generation and fault-free bit streams. In this work, the test stimulus is specifically a sinusoidal signal, which is an ordinary operating signal in most analog circuits, and has been employed extensively for testing purposes. The test output, denoted as $v_t(t)$, is reported in digital form, complying with both internal scan path operations and external monitoring.

With reference to Fig. 3, the proposed test strategy is the investigation on a response of a CUT to the presence of faults so called a fault signature, denoted as $v_f(t)$. This fault signature can be either single or combined changes in sinusoidal characteristics, involving changes in DC gain, amplitude, frequency and phase shift. This test strategy is purposely applied for the testing of analog portions in mixed-signal systems such as amplifiers and filters. In addition, this test strategy investigates and characterizes all possible
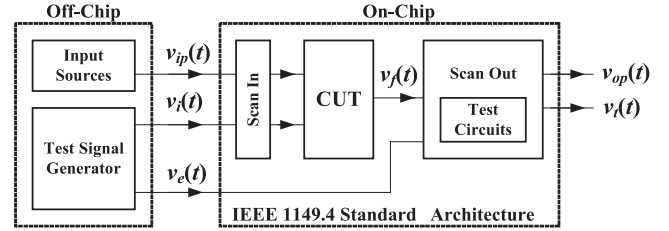

Fig. 3 The block diagram of the basic approach of the proposed testing scheme for analog circuits.

fault signature types, including small and hard changes, at an initial design stage. Therefore, this test strategy offers high fault observability and eliminates the need for pre-simulation of actual fault signature characteristics.

The fault detection technique is a comparison of changes between the fault signature and the fault-free signal in time domain. Primarily, the sinusoidal input test stimulus can be expressed as

$$v_i(t) = V_i + v_i \sin(\omega_i t + \Phi_i) \tag{1}$$

where V_i is DC offset level in volts, v_i is amplitude in volts, ω_i is frequency in radian per second, and Φ_i is phase shift in degree per second. The details of the fault detection technique are described by two cases as follows.

In the case when applying the sinusoidal test stimulus to a fault-free CUT, the expected output signal remains a sinusoid with some specific parameters, depending on operating conditions of the CUT such as amplitude amplification or frequency filtering. When the operating condition of the fault-free CUT is set for testing purposes, this expected output is known. The test signal generator consequently generates the fault-free signal $v_e(t)$, which has the same value as this expected output signal.

In the case when applying the sinusoidal test stimulus to a faulty CUT, the presence of faults may cause some changes. The fault signature may different from the fault-free signal $v_e(t)$ and can be expressed as

$$v_f(t) = V_f + v_f \sin(\omega_f t + \Phi_f) + \Sigma v_f^n \sin(\omega_f t + \Phi_f)^n \tag{2}$$

It is seen in (2) that the fault signature is the summation of three constituents, i.e. a DC offset voltage, a major tone signal, and distortion components. Such differences in sinusoidal characteristics between $v_f(t)$ and $v_e(t)$ are observable through some changes in parameters, ranging from output parameter deviation that exceeds acceptable tolerances to extremely deformed sinusoids. Therefore, this work realizes the comparison between the signals $v_e(t)$ and $v_f(t)$ for fault detection. The comparison process is achieved by characterizing sinusoidal characteristics through the use of two threshold voltages V_H and V_L. This fault detection technique has purposely been proposed for the suitability of the implementation of a testing circuit embedded in the ABM of the IEEE 1149.4 architecture.
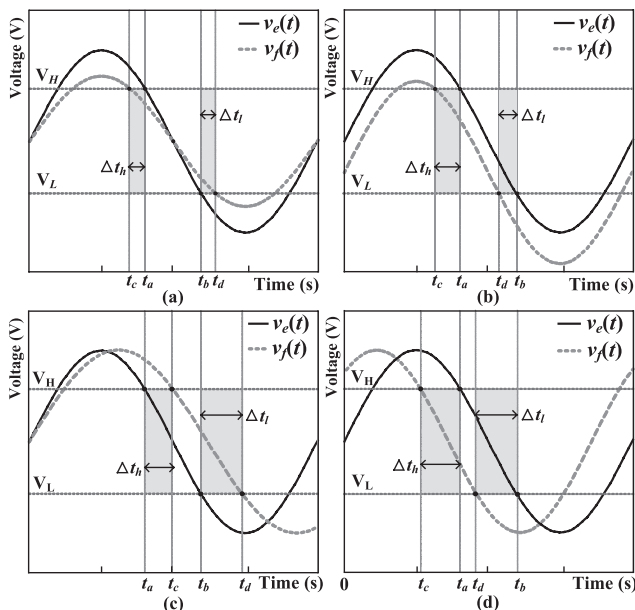
Fig. 4 Examples of fault signature waveforms resulting from small changes in the distinct case $v_{fmax} > V_H > V_L > v_{fmin}$.
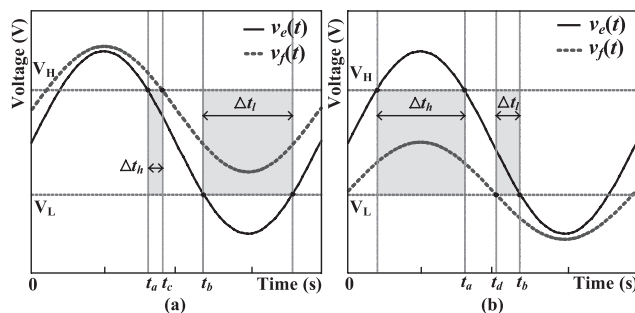

Fig. 5 Examples of fault signature waveforms resulting from hard changes; (a) $v_f(t)$ showing $v_{fmax} > V_H > v_{fmin} > V_L$, (b) $v_f(t)$ showing $V_H > v_{fmax} > V_L > v_{fmin}$.
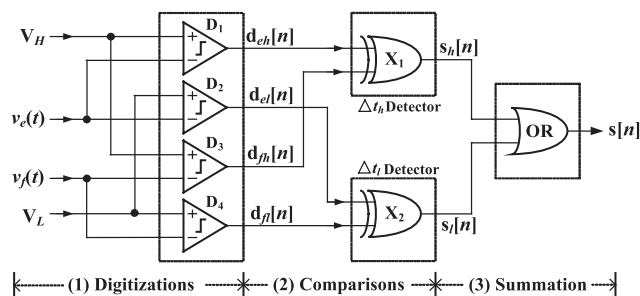

Fig. 6 The circuit diagram of the fault signature characterization-based testing circuit.

3.2 Fault Signature Characterization Technique

Fault signature characterization is accomplished by means of two threshold voltages V_H and V_L as the crossing levels. Fault detection is performed by monitoring the values of crossing time difference between signals $v_e(t)$ and $v_f(t)$. The crossing time difference at V_H is defined as $\Delta t_h = |t_a - t_c|$ where t_a and t_b are time when $v_e(t)$ and $v_f(t)$ cross over V_H, respectively. The crossing time difference at V_L is defined as $\Delta t_l = |t_d - t_b|$ where t_b and t_d are time when $v_e(t)$ and $v_f(t)$ cross over V_L, respectively. This fault signature characterization process classifies fault signatures into two varieties of changes, i.e. small and hard changes.

On the one hand, the small change is defined as occurring in the distinct case $v_{fmax} > V_H > V_L > v_{fmin}$ where v_{fmax} and v_{fmin} are maximum and minimum peak amplitudes of $v_f(t)$, respectively. The measured parameters includes DC level, amplitude, frequency, and phase shift. Figure 4 demonstrates four particular examples of fault signature waveforms resulting from small changes. The monitoring is investigated in the region of $T/4$ to $3T/4$ where T is a signal period. Figure 4 (a) demonstrates the fault signature with a decrease in amplitude, and shows that the values of Δt_h and Δt_l are equal. Increases in amplitude also exhibit similar characteristics. Figure 4 (b) demonstrates the fault signature with a decrease in DC offset level and reveals that Δt_h is greater than Δt_l. In cases where the DC offset increases, Δt_h is smaller than Δt_l. Figure 4 (c) demonstrates the fault signature with a decrease in frequency, and shows that Δt_h is less than Δt_l. In cases where the frequency is higher, Δt_h is greater than Δt_l. Figure 4 (d) demonstrates the fault signature with phase lagging behavior and shows that Δt_h and Δt_l are equal. Phase leading behavior also exhibits

similar characteristics.

On the other hand, the hard change is defined as occurring in other cases except for the case of small changes. This hard change exhibits an enormous amplitude reduction or even steady DC outputs. Therefore, the amplitude of fault signatures dominates the measurement. Figure 5 demonstrates two particular examples of fault signature waveforms resulting from hard changes. The time differences are investigated throughout the signal period. Figure 5 (a) demonstrates the fault signature with the case $v_{fmax} > V_H > v_{fmin} > V_L$. The value of Δt_h is detectable in the similar manner to Fig. 4 (a). As there is no crossing of the fault signature at V_L, the value of Δt_l is obtained at time between two crossing points of the signal $v_e(t)$ at V_L. Figure 5 (b) demonstrates the fault signature with the case $V_H > v_{fmax} > V_L > v_{fmin}$. The value of Δt_l is also detectable as demonstrated in Fig. 4 (a). Similarly, the value of Δt_h is obtained at time between two crossing points of the signal $v_e(t)$ at V_H. In addition to these two cases demonstrated in Fig. 5, the hard changes include hardly deformed sinusoidal characteristics in other three possible cases, i.e. $v_{fmax} > v_{fmin} > V_H$, $V_H > v_{fmax} > v_{fmin} > V_L$, and $V_L > v_{fmax} > v_{fmin}$. In addition, fault signatures can also exhibit DC outputs, including stuck-at-VDD or stuck-at ground. These types of fault signatures provide the values of Δt_h and Δt_l throughout the signal period, and consequently faults are easily detected through this characterization process.

3.3 The Design of Fault Signature Characterization-Based Testing Circuit

Figure 6 shows the circuit diagram of the designed testing circuit that performs fault signature characterization process. As shown in Fig. 6, fault detection process is performed consecutively in three steps, i.e. digitization, comparison and summation. Firstly, the digitization is performed by four comparators D_1 to D_4, which operate as 1-bit A/D converters. The signal $v_e(t)$ is digitized against V_H and V_L through D_1 and D_2, providing two sets of digital output signals $d_{eh}[n]$ and $d_{el}[n]$, respectively. The signal $v_f(t)$ is digitized against V_H and V_L through D_3 and D_4, providing two sets of digital output signal $d_{fh}[n]$ and $d_{fl}[n]$, respectively. Secondly, the comparison is performed by means of two XOR gates X_1 and X_2. This detection process simply monitors the difference between logics 1 and 0, and reports the outputs as 1 when the two inputs have different logical values. In this process, the comparison of $d_{eh}[n]$ and $d_{fh}[n]$ is performed for detecting the values of Δt_h reported as $s_h[n]$. Similarly, the comparison of $d_{el}[n]$ and $d_{fl}[n]$ is performed for detecting the values of Δt_l reported as $s_l[n]$. Finally, the summation of two signal $s_h[n]$ and $s_l[n]$ are carried out through OR gate in order to report a single test output $s[n]$.

4. Testing System Implementation

Figure 7 shows the circuit configuration of the proposed ABM with extended functionality for on-chip and off-chip testing capability. The circuit comprises four major blocks, i.e. (1) an analog CUT, (2) an input ABM, (3) an output ABM, and (4) an internal switching network. First, the CUT can be a class of analog functional blocks such as amplifiers and filters. The primary inputs can be either an external input v_{ip1} or an internal v_{ip2} obtained from a D/A converter,

and a primary output is v_{op}. Second, the input ABM located at the input pin comprises mainly the voltage comparator C_D and the switches S_D, S_G, S_L, S_H, S_{B1}, S_{B2}, and S_{GI}. Third, the output ABM located at the output pin consists of the same components utilized in the input ABM except for the switch S_{GI}, and the testing circuit previously described in Fig. 6 with five control switches S_T. Last, the internal switching network located between the outputs of an internal D/A converter comprises the switches S'_D, S'_{B1}, S'_{B2}, and S'_{GI}, offering of testing accessibility in the case where v_{ip2} is realized.

This ABM is capable of four testing modes as follows. Mode 1 is a traditional digital scan mode where the switches S_D, S_G, S_L, S_H of both input and output ABMs are operating, corresponding to TDI signals, while other switches are opened. This Mode 1 allows the ABM to operate as the DBM by detecting bridging faults at the output terminal through the comparator C_D and shifting to the serial digital test bus. Mode 2 is a traditional external analog test mode where the switches S_{B1} of the input ABM and S_{B2} of the output ABM are closed, while other switches are opened. The input signal stimulus sourced at the port AT_1 is contributed to the CUT through the bus AB_1. The output response from the CUT is provided at the bus AB_2 and subsequently conveyed to the port AT_2 for the external testing.

Mode 3 is an extended external analog test mode where the switch S_{GI} of the input ABM is closed and the alternative input is sourced at V_G terminal. This mode 3 provides the multiple-pin accessibility at one time by means of the direct access to the CUT, and the disconnection of input ABM and internal test buses. The corresponding output can be monitored separately at the output pin by closing the switch S_D of the output ABM. Mode 4 is an extended on-chip testing mode through the signal characterization process where the switches S_D and S_{B1} of the input ABM are closed and all switches S_T of the output ABM are closed, and others are opened. With reference to Fig. 3, the input signal
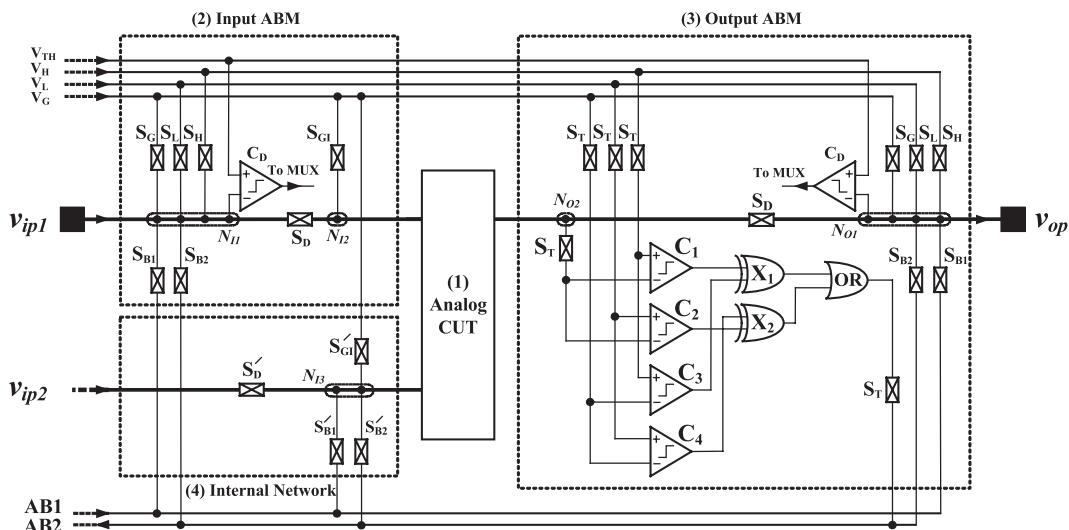

Fig. 7 The circuit configuration of the ABM with on-chip testing circuit.
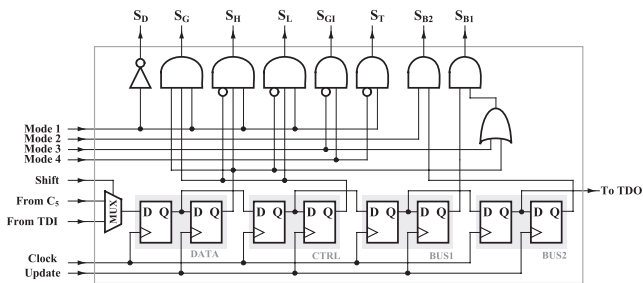
Fig. 8 The block diagram of the control circuitry.

Fig. 9 The circuit diagram of the CUT example.

stimulus $v_i(t)$ sourced at the port AT1 is contributed to the CUT through AB1. The fault signature $v_f(t)$ obtained from the CUT at node N_{O2} and the expected signal $v_e(t)$ sourced at the port V_G are conveyed to the testing circuit. Subsequently, the test circuit processes signal characterizations and provides the test output to the output node N_{O1}.

As the test circuit reports the faultiness by logic 1, the comparator C_D subsequently captures the test output $s[n]$ at node N_{O1} is then loaded in to the serial interface in order to complete a boundary scan throughout the system. This test output also called $v_t(t)$ also visible at the port AT_2 conveyed by the bus AB_2. Figure 8 shows the circuit diagram of the control circuitry, suggesting for the use in a full system implementation. The control and update shift registers, are utilized for loading control instruction and test data. However, the decoding logic is specially designed for accomplishing the four modes of operations. The decoded signals are exploited for controlling all the switches. In addition, the existing TIBC shown in Fig. 2 (b) can be employed directly for multiplexing the input and output test signals.

5. Fault Models and Analog Circuit Testing Demonstrations

5.1 Fault Descriptions and Modeling

Failures in electronic components are generally the effects of chemical and physical processes. Failures caused by chemical effects lead to continuous production of defective components over whole production lines. However, failures caused by physical effects result in defects in individual components, and can be classified as intrinsic and extrinsic failures. Intrinsic failure is a defect that depends on some specific technology and manufacturing process, while extrinsic failure comprises all defects related to component breaks, interconnections or packaging.

Consequently, faults in CMOS integrated circuits based on physical failures are generally classified into two categories, i.e. catastrophic and parametric faults [14], [15]. Parametric faults involve changes in circuits that degrade expected performances. Parametric faults are exclusively caused by intrinsic failures, including gate-oxide shorts and process parameter variations of nominal values. As parametric faults in CMOS technology typically depend on parameter tolerance band acceptability, modeling of paramet-
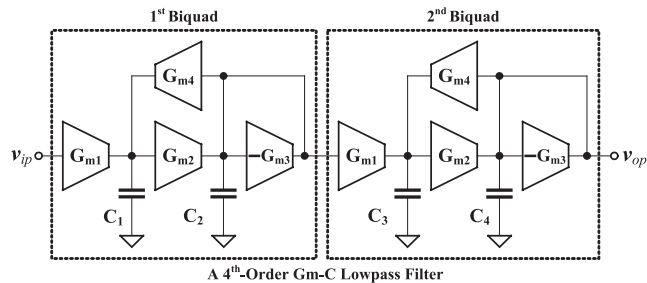
ric faults is relatively complicated at the physical design level, and high-precision testing after fabrication is generally utilized. On the other hand, catastrophic faults involve changes in circuits that cause circuit operations to fail catastrophically. The causes of catastrophic faults include intrinsic failure, including extensive variation in design parameters such as aspect ratio, and extrinsic failure, including resistive shorts and potential opens. Catastrophic faults cover a wide range of realistic failures.

As a number of standard digital fault models are in existence, fault simulations in digital CMOS integrated circuits can be realized at all levels of abstraction, ranging from behavioral to layout levels. However, there are no standard fault models for analog integrated circuits and therefore fault simulations are realized mostly at the transistor level by inserting resistors into the CUT. Insertion of resistors provides a sufficient simulation of the electrical behavior of shorts and opens, and offers low complexity fault modeling suitable for most types of CUT. In this work, shorts are modeled by connecting a small resistor between each pair of terminals, including Gate-Drain short, Gate-Source short, and Drain-Source short. Additionally, opens are modeled by inserting a parallel combination of a large resistor and a small capacitor in series into each terminal, including Drain and Source opens. However, the Gate open is not easily modeled and thus generally excluded from the fault list in many works. As direct insertion of resistor and capacitor at the gate terminal is not effective for simulating real behavior of gate open, this work therefore realizes gate open by means of grounded resistor and capacitor at the two disconnecting terminals [8] in order to eliminate the voltage discontinuity in appropriate simulation in Hspice. Based on the described fault models, fault injections in this work are performed at a time. Shorts were modeled by 1-Ω resistors while opens were modeled by 10-MΩ resistors and 1-pF capacitors [16].

5.2 A Demonstrating Circuit-Under-Test

As a particular example, a baseband 4th-order G_m-C lowpass filter [16] has been chosen as a CUT. The G_m-C lowpass filter has been utilized extensively in base-band sections of RF receivers. These base-band sections are generally implemented by means of CMOS mixed-signal LSI chips, owing to the capability to operate at higher frequency

compared to passive RC filters. Figure 9 shows the block diagram a 4th-order low-pass G_m-C filter, comprising a cascade connection of two identical 2nd-order G_m-C biquads. The values of G_{m1}, G_{m2} and G_{m4} are equal, while the value of G_{m3} is twice, i.e. $2G_{m3} = G_{m1} = G_{m2} = G_{m4}$. The values of capacitors C_1 and C_2 are equal, and capacitors C_3 and C_4 are also equal.

These capacitors were implemented by linear on-chip capacitors. The G_m blocks are balanced CMOS operational transconductance amplifiers (OTA) [17]. With reference to Fig. 9, the total number of 45 faults exists in the OTA, of which 18 are shorts and 27 are opens. Consequently, the total number of 360 faults exists in the fault list. The catastrophic faults of the linear capacitors exhibited the total number of 8 faults, of which 4 were shorts and other 4 were opens. Capacitance variations of the four linear capacitors were also considered at the deviation of 15% from the nominal values.

6. Simulation Results and Discussion

The proposed ABM with testing circuit shown in Fig. 7 and the CUT shown in Fig. 9 were implemented using 0.18-μm standard CMOS technology, and simulated using Hspice. Figure 10 shows the physical layout of the implemented system, including the ABM, CUTs and PADs. The transistor length (L) was kept minimum at 0.18 μm. The sizes of transistor width were optimized. The area overhead is 18.5%. Note that the area overhead depends upon types of CUTs. Particularly, the testing circuit in this work was shifted into the ABM, which is shared for multiple internal analog building blocks. The area overhead may not present the difficulty in the overall system. This layout was initially extracted in order to obtain the circuit netlist prior to the simulation. The evaluation of design and test preprocess were performed in four aspects as follows.

First, the performance of the ABM with testing circuit in Fig. 7 was investigated. The XOR and OR gates were implemented using standard cells while the comparators were particularly designed based on a rail-to-rail complementary NMOS and PMOS configuration [18]. All switches were implemented by a typical CMOS transmission gates. Table 1 summarizes the resulting performances of the ABM with testing circuit. As shown in Table 1, the comparators are capable to operate in a wide voltage comparison range of 0.2 V to 1.6 V with relatively low offset error of 0.042 V throughout this range. Therefore, the voltages V_H and V_L can be adjustable broadly, depending on actual amplitude of a sinusoidal test stimulus. In addition, the maximum operating frequency is 260 MHz, offering a capability to obtain a wide range of input test stimulus frequency prior to this maximum frequency.

Second, the capability of fault signature characterization were investigated and demonstrated. Figure 11 shows the simulated waveforms of the demonstrating fault-free signal $v_e(t)$ of $0.9 + 0.5 \sin(2\pi 1000t)$ and the fault signature $v_f(t)$ with 5% deviation of each sinusoidal parameters, including
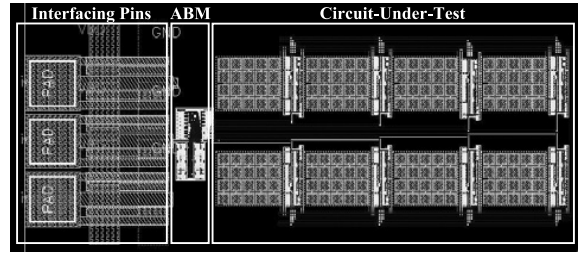

Fig. 10 The physical layout design of the CUT and the IEEE1149.4 standard system showing ABM, CUT and PADs.

Table 1 Summary of the performances of the testing circuit shown in Fig. 7.

Testing Circuit Performances		Values	Units
Comparator Performances	Maximum V_H	1.6	V
	Minimum V_L	0.2	V
	Offset Error	0.042	V
Minimum Detectable Variation		>0.5	%
Maximum Operating Frequency		260	MHz

changes in DC level, amplitude, frequency and phase shift. In this test condition, the voltages V_H and V_L were optimally set at 1.2 V and 0.6 V, respectively. Figure 11 (a) shows the increase in DC level V_f at 0.945 V, and the test output $s[n]$ reports the digital pulse with a pulse width (PW) of 18.72 μs. Figure 11 (b) shows the increase in amplitude v_f at 0.525 V, and $s[n]$ reports a digital pulse with PW of 5.57 μs. Figure 11 (c) shows the decrease in frequency ω_f at 950 Hz, and two pulses $s_{c1}[n]$ and $s_{c2}[n]$ report two digital pulses with PW of 31.69 μs and 47.28 μs, respectively. Figure 11 (d) shows the change in Φ_f at $+18°$, and $s[n]$ reports a digital pulse with PW of 49.94 μs. These four fault signatures in Fig. 11 indicate that the ABM with testing circuit effectively detects the faults that exhibit small variations. Consequently, this technique is potentially applicable for the detection of catastrophic faults, which generally exhibit hardly deformed sinusoidal outputs as previously shown in Fig. 5. Moreover, it can be seen from Table 1 that this ABM with testing circuit could detect a minimum change in each single sinusoidal parameter at 0.5%. Therefore, parametric faults, which generally exhibit a variation in $\pm 5\%$ tolerance band, are also detectable.

Third, the performances of two CUTs were simulated and compared in order to validate testing operations and investigate performance degradation. Such two CUTs are the primitive CUT, called CUT_{EXC}, and the CUT with an inclusion of the IEEE1149.4 standard testing system, called CUT_{INC}. In this work, the CUT was designed with the cutoff frequency and DC gain of 11 MHz and 4 dB, respectively. Table 2 shows the comparison of the performances between these two CUTs, measured at the pads of output pins. Although the performances deviation are expectedly introduced by additional stray capacitances and on-resistances of the switches, the deviation percentage shown in Table 2 are relatively low, including the deviation of the DC gain and
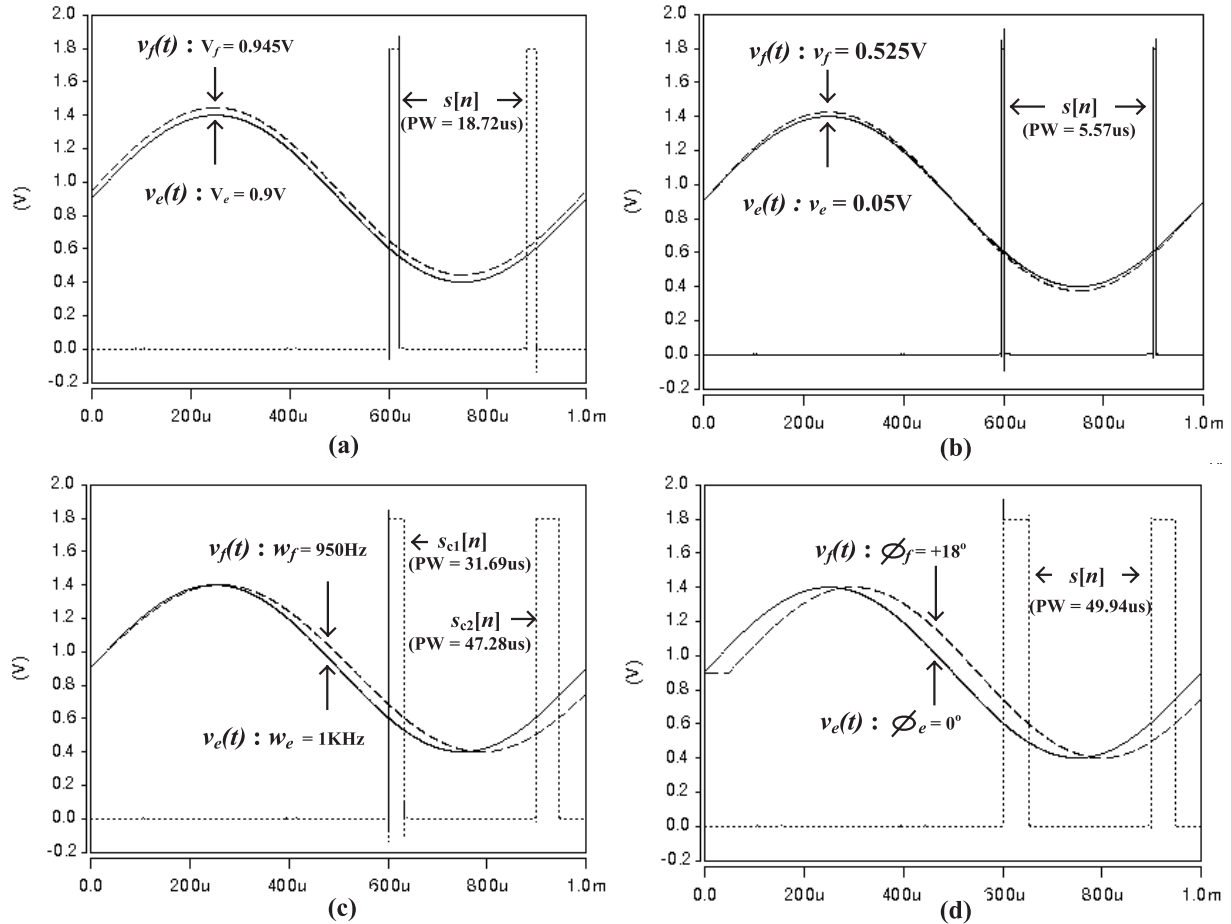
Fig. 11 Simulated waveforms of $v_e(t) = 0.9 + 0.5\sin(2\pi 1000t)$ and $v_f(t)$ with 5% deviation.

Table 2 Comparisons of performances between a primitive CUT and a CUT with an exclusion of the IEEE1149.4 standard testing system.

CUT Performances	Simulated Values			
	CUT_{EXC}	CUT_{INC}	% Dev.	Units
Cutoff Frequency	11	11	-	MHz
DC Gain	4	3.99	0.0025	dB
Linearity (v_{pp}=300mV)	0.0067	0.00664	0.895	%

Table 3 Summary of number of faults, detected and undetected faults, and fault coverage in percentages.

Faults	Simulated Values			
	No. of Faults	Detected	Undetected	Fault Coverage
OTA	360	339	21	94.16%
Capacitor (Catastrophic)	8	8	0	100%
Capacitor 15% Dev	4	4	0	100%

the linearity of values 0.0025% and 0.895%, respectively, while no deviation of the cutoff frequency was evident. It can be concluded that the proposed testing system affects low impacts on primitive CUTs.

Last, fault injections were performed, corresponding the fault models and the fault list of the CUT. Table 3 summarizes number of faults, detected and undetected faults, and fault coverage in percentages. As seen from Table 3, the fault coverage of faults associated in CMOS and capacitors are acceptable at 94.16% and 100%, respectively.

As a result of overall circuit designs and simulation results, significant advantages and some limitations are discussed as follows. The propagation delay of the CUT, resulting from high-frequency operations or process variations, may cause some phase and gain changes. In order to

avoid this problem, the testing condition of the CUT should be performed in a stable region, such as in the filter passband at unity gain, prior the maximum operating frequency of the testing circuit. In addition, the externally supplied fault-free signal should be in synchronization with the input stimulus using, for example, an external phase shifter or an available synchronized signal generator. The extra requirements, compared to the existing configuration, include an additional pin for the expected output signal and some additional transmission gate switches. The limitations of this work include testing for high-frequency circuits such as front-end RF receivers, and testing for analog circuits, which do not operate or provide sinusoidal signals, such as neural oscillators.

In comparisons to other existing works, the advantage of this work is a fully available functionality for both INTEST for on-chip testing with acceptable fault coverage, and the EXTEST for high-quality off-chip testing of some hard-to-detect faults and functional tests. In particular for INTEST, this work provides a non-intrusive and a complete detection of all possible fault signatures in standard environments rather than an individual testing circuits for each specific CUT. The proposed test strategy and technique can be further applied for analog-mixed signal circuits such as phase-locked loops and data converter circuits. Moreover, a complete BIST implementation using the proposed testing technique is also possible for some particular applications by only storing the fault-free signal in the system memory. The future planned work involves the enhancement for high frequency testing and the applications for complete mixed-signal circuits and systems.

7. Conclusions

The analog circuit testing scheme through the extension of the IEEE 1149.4 standard has been presented. The proposed fault signature characterization technique provided the complete detection of sinusoidal fault signatures. The system implementation afforded functionalities for both INTEST for on-chip pre-screening of defective chips, and EXTEST for high-quality off-chip testing. The 4th-order G_m-C low-pass filter with the inclusion of the proposed testing approach was fully implemented in the physical level. The maximum operating frequency of the ABM with testing circuit was measured at 260 MHz, where both catastrophic and parametric faults were potentially detectable at the parameter variation greater than 0.5% with low performance degradation. The fault coverage of faults associated in CMOS and capacitors acceptable at 94.16% and 100%, respectively. This work has offered the enhancement of standardizing test approach, which reduces the complexity of testing circuit, provides non-intrusive testing circuit, and is effectively applicable for pre-screening of defective devices.

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