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Thermal analysis of amorphous oxide thin-film transistor degraded by combination of joule heating and hot carrier effect

Satoshi Urakawa,[1] Shigekazu Tomai,[2] Yoshihiro Ueoka,[1] Haruka Yamazaki,[1] Masashi Kasami,[2] Koki Yano,[2] Dapeng Wang,[3] Mamoru Furuta,[3] Masahiro Horita,[1,4] Yasuaki Ishikawa,[1,4] and Yukiharu Uraoka[1,4]

[1]*Graduate School of Material Science, Nara Institute of Science and Technology, 8916-5 Takayama, Ikoma, Nara 630-0192, Japan*

[2]*Advanced Technology Research Laboratories, Idemitsu Kosan Co., Ltd., Sodegaura, Chiba 299-0293, Japan*

[3]*Environmental Science and Engineering, Kochi University of Technology, Kami, Kochi 782-8502, Japan*

[4]*JSPS, Core Research for Evolutional Science and Technology, Japan Science and Technology Agency, 4-1-8 Honcho, Kawaguchi, Saitama 332-0012, Japan*

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Stability is the most crucial issue in the fabrication of oxide thin-film transistors (TFTs) for next-generation displays. We have investigated the thermal distribution of an InSnZnO TFT under various gate and drain voltages by using an infrared imaging system. An asymmetrical thermal distribution was observed at a local drain region in a TFT depending on bias stress. These phenomena were decelerated or accelerated with stress time. We discussed the degradation mechanism by analyzing the electrical properties and thermal distribution. We concluded that the degradation phenomena are caused by a combination of Joule heating and the hot carrier effect. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4790619]

The roles of organic light-emitting diode (OLED) and system-on-panel (SoP) devices become increasingly important in next-generation information devices with the flexibility of display designs. To realize these devices, some characteristics, such as high electrical properties and a low-temperature process on a large-sale substrate, are indispensable. However, a Si-based process cannot be applied to these devices owing to their high temperature or special treatment, such as laser crystallization. Recently, an a-InGaZnO (IGZO) thin-film has attracted considerable attention as a transparent amorphous oxide semiconductor (TAOS),[1,2] which enables the fabrication of a thin-film transistor (TFT) with high electrical properties on a large-scale substrate at very low temperature. On the other hand, Tomai *et al.* reported that a-InSnZnO (ITZO) replacing gallium with tin in IGZO has excellent properties, such as high mobility.[3] Furthermore, it has been reported that the ITZO TFT shows high reliability under the normal stress condition.[4,5]

To realize the OLED and SoP devices, reliability under electrical stress in TAOS TFTs is one of the most important issues to be resolved. Numerous studies focusing on reliability have been reported. On the other hand, the Joule heating effect of the TFTs might be a significant problem because they are fabricated on low-thermal-conductivity substrates observed similarly to low-temperature-processed poly-Si TFTs. However, the degradation phenomenon induced by the Joule heating of oxide TFT[6] has not been investigated compared with that of Si TFTs.[7–10] Fujii *et al.* have reported the self-heating effect of IGZO TFTs induced by Joule heating under voltage operation.[11] However, the result indicated in their paper has not been sufficient for explaining the degradation phenomenon of the oxide TFTs under electrical stress. Therefore, we have carefully investigated the relationship between the electrical degradation and thermal distribution of the ITZO TFTs by applying severe electrical stresses. Through this study, we detected a change in the thermal distribution of oxide TFTs with stress time, which could never be detected in silicon TFTs.

A schematic cross-sectional view of the bottom-gate ITZO TFT with W/L = 66/45 μm is shown in Fig. 1. First, a chromium (Cr) gate electrode was formed on a glass substrate. The gate insulator of SiO_x (150 nm) was deposited at 350 °C by plasma-enhanced chemical vapor deposition (PECVD). An ITZO layer with a thickness of 45 nm was then deposited at 150 °C from a sintered ITZO ceramic target (Idemitsu Kosan Co., Ltd.) by rf magnetron sputtering with a mixed gas of $Ar/O_2 = 15/15$ sccm at a deposition pressure of 1 Pa. After defining an active channel, a SiO_x film (200 nm) was deposited as an etch-stopper by PECVD. The source and drain electrodes were formed using indium-tin-oxide (ITO) via contact holes. A SiO_x passivation layer (200 nm) was deposited by PECVD. Finally, ITZO TFTs were annealed in N_2 ambient at 350 °C for 1 h before electrical measurement.

To analyze the degradation mechanism, various gate and drain voltages were applied to ITZO TFTs as electric stress. The surface temperature of a TFT under operation was analyzed using a thermal imaging system and an InSb infrared detector with a 256 × 256 pixel CCD (Infra Scope). The detector was sensitive to wavelengths of 3–5 μm. The

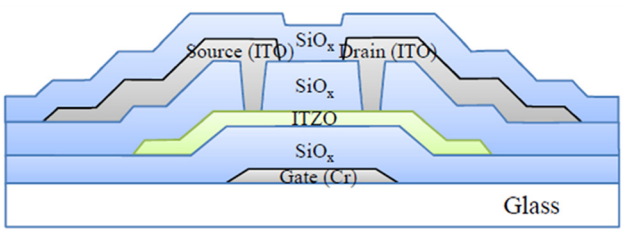

FIG. 1. Cross-sectional view of ITZO thin-film transistor.

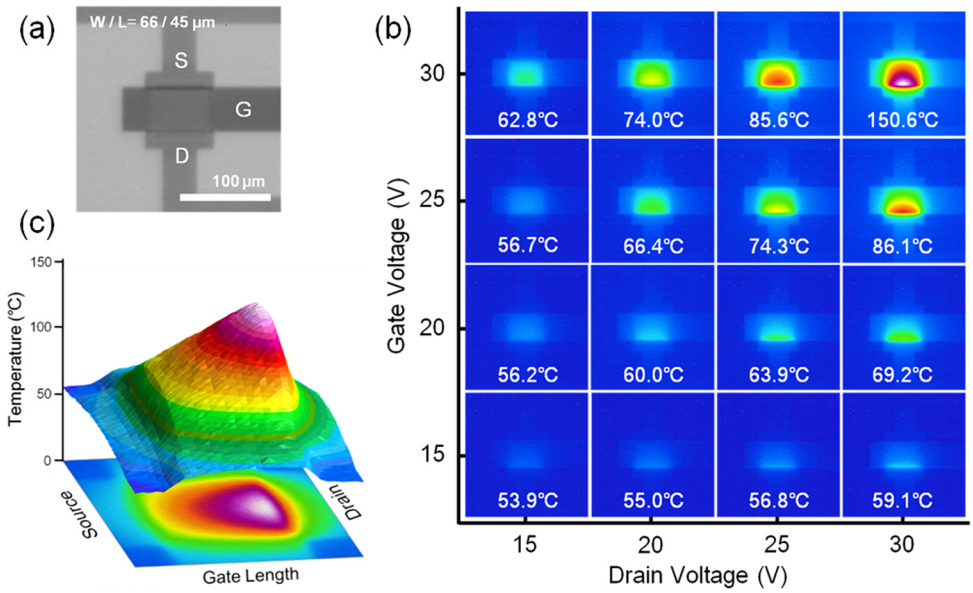

FIG. 2. (a) Optical microscopic image of thin-film transistor with a gate width of 66 μm and a gate length of 45 μm used for thermal analysis. (b) Thermal distribution under various gate and drain voltages. (c) Two-dimensional image of thermal distribution with stress voltage of $V_g = V_d = 30$ V.

sample stage was kept at 50 °C to compensate for the effect of various materials of different emissivities. This compensation enables us to measure the temperature of the sample in the range of 50–250 °C with an accuracy of 0.1 K. The spatial resolution depends on the magnification and decreases to approximately 3 μm.

The thermal distribution of ITZO TFTs under various gate and drain voltages was investigated. The heating phenomenon in the ITZO channel was observed only when both gate and drain voltages were applied. Fig. 2(a) shows the top optical image of the surface of an ITZO TFT with a gate width of 66 μm and a gate length of 45 μm. Fig. 2(b) shows the thermal images of the TFT corresponding to that in Fig. 2(a) under gate and drain voltages from 15 to 30 V. The temperature was increased by increasing the bias voltage, and a maximum temperature of 150 °C was observed under high gate and drain voltages ($V_d = V_g = 30$ V). Fig. 2(c) shows the two-dimensional thermal distribution of the TFT under the above condition. The thermal distribution shows a high level of local heating near the drain region with a temperature gradient relative to that of the source region. The difference in temperature between the source and drain regions is at most 50 °C. Furthermore, the local heating near the drain region was observed at $V_d > V_g$. On the other hand, the heat spread in the entire channel region at $V_d < V_g$. Although the thermal distribution at $V_d = V_g$ is intermediate between these at $V_d > V_g$ and $V_d < V_g$, the highest temperature was observed at $V_d = V_g$.

Fig. 3 shows the thermal distribution of the TFT at $V_g = 30$ V and $V_d = 15$–30 V. Fig. 3(a) shows the thermal distribution at the gate width indicated by an arrow in the left figure. The temperature at the gate width increased symmetrically with increasing drain bias voltage, and the maximum temperature was observed at the center of the channel. However, the thermal distribution at the gate length shown in Fig. 3(b) indicated a different tendency. Although a symmetrical distribution was observed at a low voltage in a linear region, the local thermal distribution near the drain region was observed at a high voltage under a saturation condition as described previously. As a result, it was found that the local heating temperature in the depletion region under a saturation condition and saturation currents generate the maximum temperature of the TFT. A quantitative comparison between experimental and theoretical results is now under way.

To analyze the degradation phenomenon by bias voltage stress application, the thermal distribution of an ITZO TFT at $V_d = V_g = 20$ V for 10 000 s was measured. Fig. 4 shows the changes in the transfer characteristics of the TFT measured with a drain voltage of 5.0 V. The transfer curves show an apparent shift in threshold voltage (V_{th}) and a change in drain current. Initially, the V_{th} was 1.1 V. Under bias stress up to 100 s, the V_{th} shifted to the positive direction to be 1.6 V, and the drain current decreased by 7.4%. Furthermore, the positive shift was saturated in a short stress time, after which the negative shift and drain current increase were observed. Finally, the V_{th} shifted to the negative direction to be −3.5 V, and the drain current increased by 56% compared with that of the TFT under bias stress for 100 s.

The top and bottom plots in Fig. 5(a) show the maximum temperatures and V_{th} shifts with stress time, respectively. Figs. 5(b) and 5(c) show the thermal images and thermal distributions with bias stress time, respectively. As

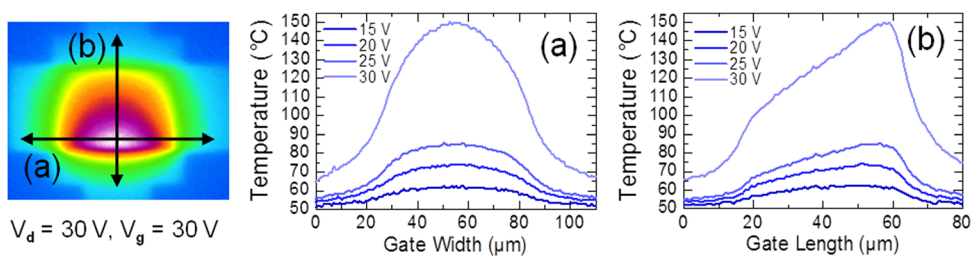

FIG. 3. Thermal distribution (a) along gate width and (b) along gate length.

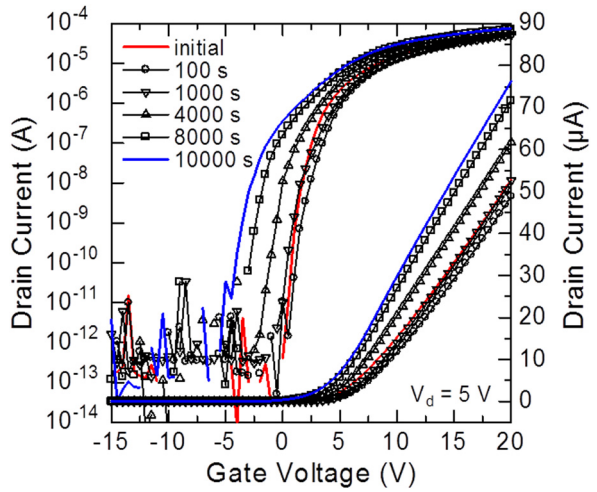

FIG. 4. Change of transfer curve of ITZO TFT with bias stress of $V_g = 20$ V and $V_d = 20$ V.

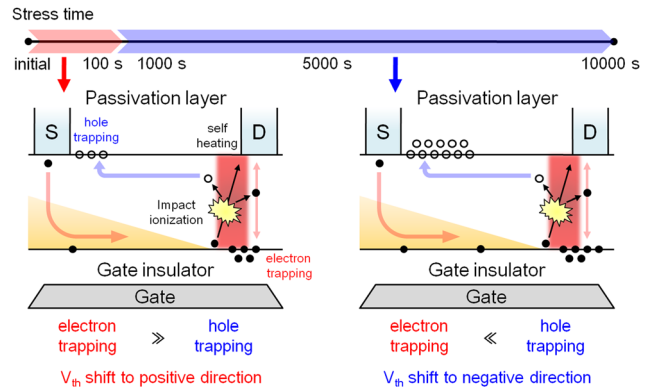

FIG. 6. Degradation model with bias stress of $V_g = V_d = 20$ V in the early period (left) and in the second stage (right).

shown in Fig. 5(a), it was found that the heating temperature under bias stress increased over the stress time range considered and that the maximum temperature increased from 64 to 75 °C. Furthermore, the temperature returned to its initial value (50 °C) immediately during the measurement. On the other hand, when the bias stress was applied again, the temperature increased immediately to that just before the measurement. Therefore, the results indicate that heating is caused by Joule heating in the ITZO channel and that heat is not stored in the channel. It is notable that the temperature decreased slightly after 100 s, as shown in Fig. 5(b), and then it increased. Fig. 5(c) indicates an apparent increase in temperature near the drain region with bias stress. The V_{th} shift to the positive direction and the drain current decrease shown in Fig. 4 correspond well to the temperature decrease, and the V_{th} shift to the negative direction and the drain current increase also correspond well to the temperature increase. These results indicate clearly that the temperature change is closely related to the change in electrical performance.

In this degradation phenomenon, it seems that the V_{th} shift to the positive direction is due to electron trapping and that the negative V_{th} shift is due to hole trapping. It has been reported that the Joule heating of TFTs increased the trap states in the bulk and at the interface, and it also accelerated carrier trapping phenomena.[6] Therefore, it is considered that the degradation phenomena are related to the carrier trapping phenomena at the SiO_2 interface. Now, we discuss the degradation mechanism shown in Fig. 6. Under the saturation condition of $V_d = V_g = 20$ V, an n-channel is formed for electron transportation. Furthermore, a depletion region is formed near the drain region and Joule heating is induced in this region. Simultaneously, a high vertical electrical field is generated in the depletion region near the drain region; thus, electrons gain a high energy from a high electric field and flow into the depletion region.[12,13] Then, these carriers induce impact ionization and generate a hole-electron pair;[14] consequently, the electrons are trapped at the local interface between the channel and the gate insulator near the drain region, while the holes are trapped at the interface between the back channel and the passivation layer. Therefore, it seems that the electrical properties related to V_{th} and drain current were deteriorated by the hole and electron trapping phenomena.

It has been reported that electron mobility is higher than hole mobility for ITZO.[3] Hence, in the early period of bias stress, electron trapping into the gate insulator occurs conspicuously followed by hole trapping into the passivation layer. Therefore, it seems that the V_{th} shift to the positive direction and the drain current decrease were mainly induced by electron trapping. Furthermore, although the trapped area for electron is the local interface near the drain edge, the trapped area for hole is wide range at the interface. Therefore, in the second stage of bias stress, the trap states at the gate insulator interface is saturated by electron trapping immediately, and hole trapping into the passivation layer interface near the source region proceeds. Then, the accumulation of holes near the source region reduces the electrical potential wall between the source and the semiconductor and accelerates electron injection from the source.[15] Consequently, it seems that the drain current increase occurred. The drain current increase accelerates Joule heating in the depletion region and the heating accelerates the thermal vibration of atoms for the ITZO channel. Probability that

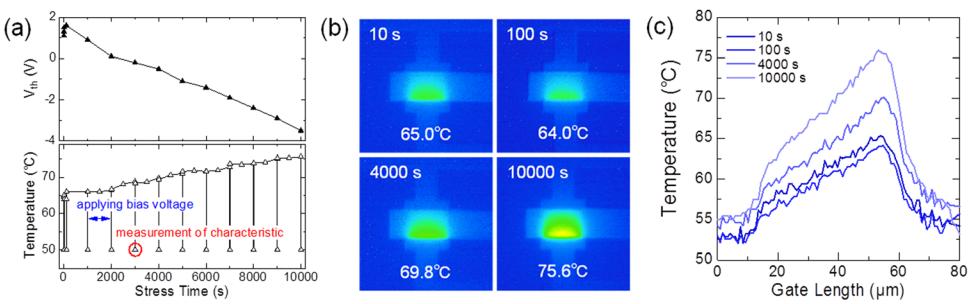

FIG. 5. (a) Change of threshold voltage (top) and maximum temperature (bottom). (b) Temperature and thermal distribution after the stress time of 10, 100, 4000, and 10 000 s. (c) Change of thermal distribution along gate length.

electrons collide with the lattice is increased by the thermal vibration. Therefore, electron energy is decreased, and hence impact ionization is suppressed. However, the generation of traps and carrier trapping phenomena are accelerated by Joule heating.

In order to indicate that the degradation does not occur only by either the joule heating or hot carrier effect, we compared the degradation phenomena under different stress condition as shown in Fig. 2(b). For the different heating condition of $V_g = 20\,V$, $V_d = 30\,V$ (69.2 °C) and $V_g = 25\,V$, $V_d = 30\,V$ (86.1 °C), although the latter temperature is higher, the former electric field near the drain junction is higher. However, the former V_{th} shit was 2.5 V, and the latter V_{th} shift was 9.2 V under bias stress for 1000 s. Therefore, it is considered that the degradation was accelerated by Joule heating. On the other hand, for the same heating condition of $V_g = 25\,V$, $V_d = 30\,V$ (86.1 °C) and $V_g = 30\,V$, $V_d = 25\,V$ (85.6 °C), although the former V_{th} shift was 9.2 V, the latter V_{th} shift was 6.7 V. Therefore, it is considered that the degradation was accelerated by higher electric field at drain edge even under same heating condition. We suppose that generation of hole is due to hot carrier effect at drain edge and hole trapping is accelerated by Joule heating; therefore, the degradation reported in this paper was caused by the combination of hot carrier effect and Joule heating.

In previous poly-Si TFTs, thermal and hot carrier degradations have been treated as different issues.[7,8] Therefore, we can conclude that the degradation observed in this study is unique in the history of TFTs. Hereafter, the performance of oxide TFTs will increase further with the development of fabrication technology. The obtained results suggest that heat dissipation by circuit design or choice of film material from a thermal view point is also important.

In this study, we performed the thermal analysis of oxide TFTs using an infrared microscope to investigate the degradation mechanism. As a result of the thermal analysis of ITZO TFTs under bias stress, local heating was observed near the drain region similarly to that in the case of Si TFTs. Then, we applied a positive bias stress to the TFTs and evaluated the change in thermal distribution. We detected a change in the thermal distribution of oxide TFTs with stress time, which could never be detected in Si TFTs. As a result of discussion, we concluded that the degradation phenomena are caused by a combination of Joule heating and the hot carrier effect, unlike in the case of poly-Si TFTs.

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