論 文 内 容 の 要 旨

With the development of advanced technology, the scale of circuit becomes larger and larger, and the testing technology becomes more and more complex. In circuit design, adding test circuit is a cost-saving way, whether it is prototype circuit or mass production circuit. In prototype circuit, the built-in self-test can help the design quickly locate the fault when testing the circuit. When the circuit is mass-produced, part of the test circuit is reserved, and the circuit performance can also be detected to eliminate defective products.

However, there are still many analog mixed-signal circuits without corresponding testing strategies. Therefore, the circuits under tested in this dissertation have two characteristics, one is that the circuit is a mixed-signal circuit; the other is that the circuit has a rarely relevant test strategy. At the same time, the purpose of this dissertation is to combine the built-in self-test technology to detect the fault of these circuits.

In the first part of this dissertation, a built-in self-test (BIST) scheme for detecting catastrophic faults in bootstrapped switches is proposed. The clock signal and the gate voltage of the sampling Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOSFET is greater than or equal to the supply voltage when the switch is turn on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by Simulation Program with Integrated Circuit Emphasis (SPICE). The simulated fault coverage is approximately 87.9% with 66 test circuits.

In the second part of this dissertation, a built-in self-test scheme for detecting catastrophic faults in dynamic comparators. In this scheme, a feedback loop is designed using the characteristics of the comparator. By monitoring the voltage in the feedback loop to determine the presence of circuit fault. The proposed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by SPICE. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the propose BIST scheme, six faults were injected into the real circuit. The test results are consistent with the simulation results.

In the third part of this dissertation, a compact window comparator for extreme voltage is proposed. Extreme voltage means that the voltage is close to the ground or close to the supply voltage. However, detection of extreme voltage is suffered by the threshold voltage of a transistor. This paper proposes a new compact window comparator, which can be used to detect extreme voltage. In this window comparator, a source follower is used to translate the extreme voltage to the voltage suitable for detection. The test results verify the proposed compact window comparator in Rohm 180nm Complementary Metal Oxide Semiconductor (CMOS) technology.