Defect-oriented Built-In Self-Test for Analog Mixed-Signal Circuits

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Abstract

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With the development of advanced technology, the scale of circuit becomes larger and larger, and the testing technology becomes more and more complex. In circuit design, adding test circuit is a cost-saving way, whether it is prototype circuit or mass production circuit. In prototype circuit, the built-in self-test can help the design quickly locate the fault when testing the circuit. When the circuit is mass-produced, part of the test circuit is reserved, and the circuit performance can also be detected to eliminate defective products.

However, there are still many analog mixed-signal circuits without corresponding testing strategies. Therefore, the circuits under tested in this dissertation have two characteristics, one is that the circuit is a mixed-signal circuit; the other is that the circuit has a rarely relevant test strategy. At the same time, the purpose of this dissertation is to combine the built-in self-test technology to detect the fault of these circuits.

In the first part of this dissertation, a built-in self-test (BIST) scheme for detecting catastrophic faults in bootstrapped switches is proposed. The clock signal and the gate voltage of the sampling Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOSFET is greater than or equal to the supply voltage when the switch is turn on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by Simulation Program with Integrated Circuit Emphasis (SPICE). The simulated fault coverage is approximately 87.9% with 66 test circuits.

In the second part of this dissertation, a built-in self-test scheme for detecting catastrophic faults in dynamic comparators. In this scheme, a feedback loop is designed using the characteristics of the comparator. By monitoring the voltage in the feedback loop to

determine the presence of circuit fault. The proposed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by SPICE. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the propose BIST scheme, six faults were injected into the real circuit. The test results are consistent with the simulation results.

In the third part of this dissertation, a compact window comparator for extreme voltage is proposed. Extreme voltage means that the voltage is close to the ground or close to the supply voltage. However, detection of extreme voltage is suffered by the threshold voltage of a transistor. This paper proposes a new compact window comparator, which can be used to detect extreme voltage. In this window comparator, a source follower is used to translate the extreme voltage to the voltage suitable for detection. The test results verify the proposed compact window comparator in Rohm 180nm Complementary Metal Oxide Semiconductor (CMOS) technology.

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1 Introduction

Performance testing schemes for analog mixed-signal circuits are usually standardized. The circuit performance parameters are obtained through a series of inputs and outputs. However, in the face of defect testing, analog mixed-signals are extremely complex and costly. Because some defects will cause the performance of the analog circuit to decline sharply, while some defects have little effect on the performance of the analog circuit under certain circumstances. This chapter mainly introduces some built-in self-test technology for analog mixed-signal circuits, the fault model used in this dissertation, the object circuits under test in this dissertation ,and the organization of this paper

1.1 An Overview of BIST Technology for Analog Mixed-signal Circuit

Analog signal refers to the information represented by a continuously changing physical quantity, and its signal is continuous in time and amplitude. Digital signal refers to the information represented by discrete changing physical quantity, and its signal is discrete in time and amplitude. Analog mixed-signal circuits are circuits that contain both analog and digital signals.

Analog to-digital converter (ADC) is a typical analog mixed signal circuit, which converts analog signals to digital signals. In 2004, ***Dongmyung Lee*** et al. published a build-in self-test scheme based on code width to test the faults in ADC [1]. The simulation results show that the fault coverage is approximately 99% in 138 test circuits.

Digital to-analog converter (DAC) is a typical analog mixed-signal circuit, which converts digital signals to analog signals. In 2013, ***Jun Yuan*** et al. published a built-in self-test scheme based on a resistance matching to the faults in DAC [2]. The test scheme is for the R-2R network and the operational amplifier in R-2R DAC. The simulation results show that the fault coverage is 96% for the R-2R network and 82.6% for the operational

amplifier.

A photon counting circuit is a typical analog mixed-signal circuit, which converts the photon signal to the current analog signal by the single photon avalanche diode, and then converted it to a voltage analog signal by an amplifier before being converted to a digital signal. In 2022, ***S. Isaak*** et al. published a built-in self-test module for faults in photon counter [3]. The measurement results show that the fault coverage is at least 90% within a 16-bit parallel photon counting circuit.

Throughout the test schemes of these analog mixed-signal circuits, there are still some analog mixed-signal circuits with little research.

1.2 Objectives of this Dissertation

In this dissertation, two simple analog mixed-signal circuits without much test research were selected as the circuits under test.

The first simple analog mixed-signal circuit is the bootstrapped switch. In this circuit, the input signal (analog signal) is transmitted through CMOS sampling transistor. The impedance of the CMOS sampling transistor is converted between low impedance and high impedance under the control of a digital circuit, and the circuit uses bootstrap technology to reduce the correlation between the transistor impedance and the input signal.

The second simple analog mixed-signal circuit is the dynamic comparator. In this circuit, the two input signals (analog signal) are compared in size through the input transistor, and the output is determined by the size of the input signal. If the positive voltage is greater than the negative voltage, the output is logic “1”; if the positive voltage is less than the negative voltage, the output is logic “0”. At the same time, the dynamic comparator has reset and latch functions under the control of digital signal. After the dynamic comparator is reset, the output is logic “0”.

1.3 Fault modeling for Circuits

The catastrophic faults simulated in this dissertation target the open and short of CMOS transistors. As shown in Figure 1.1, there are six types of faults. The gate-drain short (GDS) of the transistor is simulated as a serial connection with a 10 Ω resistor between the gate and drain. The gate-source short (GSS) of the transistor is simulated as a serial connection with a

10 Ω resistor between the gate and source. The drain-source short (DSS) of the transistor is simulated as a serial connection with a 10 Ω resistor between the drain and source. The gate open (GO) of the transistor is simulated as a parallel connection with a 10M Ω resistor and a 100f F capacitor at the gate. The drain open (DO) of the transistor is simulated as a parallel connection with a 10M Ω resistor and a 100f F capacitor at the drain. The source open (SO) of the transistor is simulated as a parallel connection with a 10M Ω resistor and a 100f F capacitor at the source.

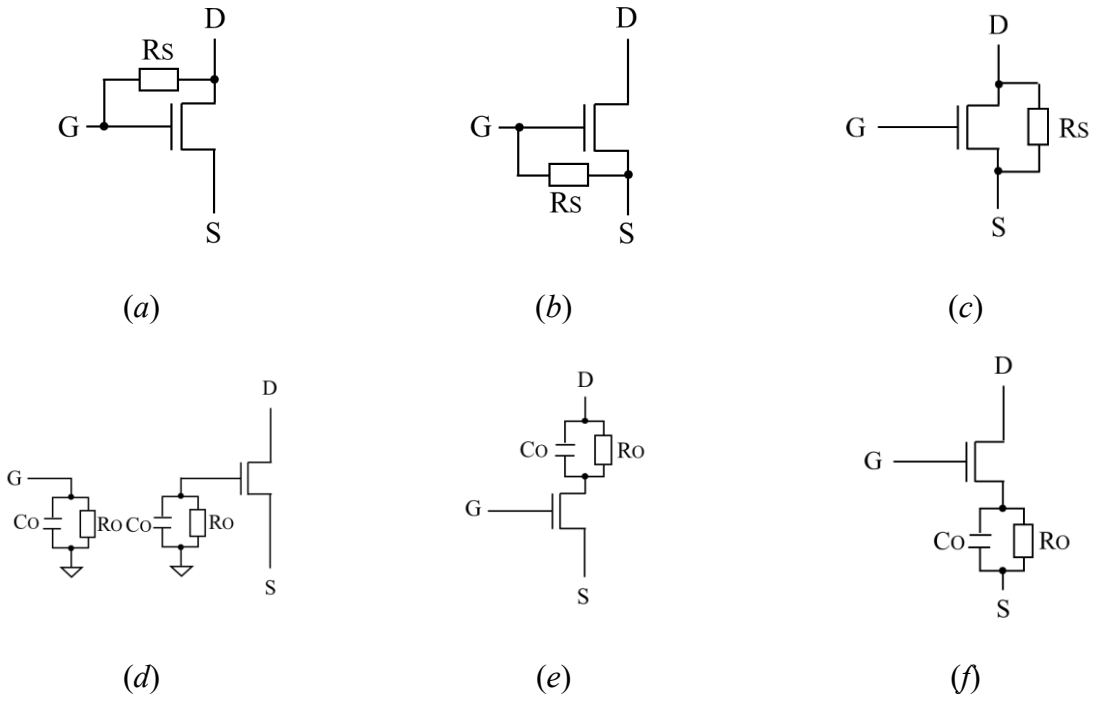

Figure 1.1 The fault types simulated in this dissertation. (*a*) the gate-drain short (GDS) of the transistor; (*b*) the gate-source short (GSS) of the transistor; (*c*) the drain-source short (DSS) of the transistor; (*d*) the gate open (GO) of the transistor; (*e*) the drain open (DO) of the transistor; (*f*) the source open (SO) of the transistor

1.4 Dissertation Organization

In this dissertation, Rohm 180nm CMOS technology is used to design a built-in self-testing scheme for two analog mixed-signal circuits and a simple window comparator for testing. The whole structure of the paper is arranged as follows.

The chapter 2 presents the proposed BIST scheme for bootstrapped switches. The clock signal and the gate voltage of the sampling MOS transistor are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOS

transistor is greater than or equal to the supply voltage when the switch is turn on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test (CUT) are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.9% with 66 test circuits.

The chapter 3 presents the proposed BIST scheme for dynamic comparator. In this scheme, a feedback loop is designed using the characteristics of the comparator. By monitoring the voltage in the feedback loop to determine the presence of circuit fault. The pro-posed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the propose BIST scheme, six faults were injected into the real circuit. The test results are consistent with the simulation results.

The chapter 4 presents the proposed compact window comparator for extreme voltage. Extreme voltage means that the voltage is close to the ground or close to the supply voltage. In this window comparator, a source follower is used to translate the extreme voltage to the voltage suitable for detection. The proposed window comparator is realized with transistor level. The simulation results verify the proposed compact window comparator in 180nm CMOS technology.

The chapter 5 summarizes the research content and results of this dissertation, and looks forward to the future improvement direction of the BIST scheme.

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2 A BIST Scheme for Bootstrapped switches

This chapter proposes a built-in self-test (BIST) scheme for detecting catastrophic faults in bootstrapped switches. The clock signal and the gate voltage of the sampling MOS transistor are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOS transistor is greater than or equal to the supply voltage when the switch is turned on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test (CUT) are realized at the transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.9% with 66 test circuits.

2.1 Introduction

Fault diagnosis is an important element in the design and test of integrated circuits. Especially with the development of CMOS circuits, it is more and more difficult to detect faults only with limited input and output ports. BIST is a viable approach that has been used by many researchers [1–9].

For data converter fault diagnosis schemes, there are schemes based on Differential Non-Linearity (DNL) test data [1], based on code-width [2], based on a resistance matching [3], and so on. For amplifier fault diagnosis schemes, there is a scheme by using an RF peak detector and two comparators [4], a scheme by checking the stable output of transient response [5], a scheme based on chaotic oscillation [6], and so on. For sample and hold circuit

fault diagnosis schemes, there is a scheme by online balance self-checking [7], a scheme by measuring performance parameters [8], a scheme by monitoring the same output with common-mode input [9], and so on.

Bootstrapped switches are widely used in many mixed-signal circuits [10–13]. For example, they are used in sample and hold circuits to achieve rail-to-rail switching functions [10,11], used in charge pump circuits to improve energy harvesting by node pre-charging [12,13], and so on. There are also reports on improving the performance of bootstrap switches [14–16]. For example, the body effect compensation technology is used to improve the linearity of the bootstrapped switch [14,15], the dual-channel sampling switch technology is used to improve the accuracy and linearity of the bootstrapped switch [16], and so on. However, there are few reports on the fault diagnosis schemes for bootstrapped switches.

Consequently, this paper proposes a BIST scheme for detecting catastrophic faults in bootstrapped switches. Section 2.2 previews the bootstrapped switch under testing. Section 2.3 presents the BIST implementation. Section 2.4 sets the simulation result by HSPICE. Section 2.5 discusses the results and gives the conclusion.

2.2 The Circuit under Test

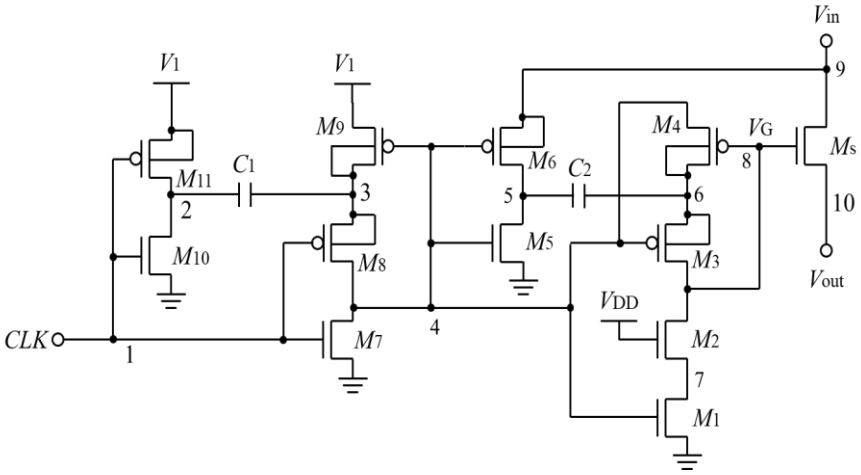
In this study, the bootstrapped switch in [17] was used as the circuit under test. The circuit and the designed size of elements are shown in Figure 2.1. *CLK* is the clock signal, which controls the "ON" phase and "OFF" phase of the bootstrapped switch. V_{in} is the input signal. V_{out} is the output signal. V_G is the gate voltage of the sampling MOS transistor.

When the bootstrapped switch is in the "ON" phase, the *CLK* is "1". Then, the voltage of Node 4 is pulled down to GND via M_7 and the voltage of Node 2 is pulled down to GND via M_{10}. Then, the voltage of Node 3 is pulled up to V_{DD} via M_9, the voltage of Node 5 follows the voltage of V_{in} via M_6 and the voltage of Node 8 follows the voltage of Node 6 via M_3. The voltage of Node 5 is transmitted to Node 6 via C_2, so the voltage of Node 6 is the voltage of V_{in} plus the voltage previously-stored at node 6.

When the bootstrapped switch is in the "OFF" phase, the *CLK* is "0". Then, the voltage of Node 2 is pulled up to V_{DD} via M_{11} and the voltage of Node 4 follows the voltage of Node 3 via M_8. Then, the voltage of Node 3 is pulled up to $2V_{DD}$ via C_1, so the voltage of Node 4 is

$2V_{DD}$. Then, the voltage of Node 8 is pulled down to GND via M_2 and M_1. Then, the voltage of Node 6 follows the voltage of Node 4 via M_4.

So, the voltage of Node 6 is $2V_{DD}$ in the "OFF" phase and $2V_{DD}$ plus the voltage of V_{in} in the "ON" phase.



M_S:20μm/0.2μm	M_7:4μm/0.2μm
M_1:1μm/0.2μm	M_8:4μm/0.2μm
M_2:1μm/0.2μm	M_9:4μm/0.2μm
M_3:2μm/0.2μm	M_{10}:2μm/0.2μm
M_4:2μm/0.2μm	M_{11}:4μm/0.2μm
M_5:2μm/0.2μm	C_1:600fF
M_6:4μm/0.2μm	C_2:600fF

Figure 2.1 The bootstrapped switch in [17] and the designed size of elements

The Bootstrapped technique improves linearity by increasing the voltage at the node to lower and stabilize the on-resistance of the sampling switch. In this study, the transmission voltage reached $2V_{DD}$, which was difficult to set up the test circuit.

2.3 The proposed BIST Scheme

When the bootstrapped switch is in the "ON" phase, the gate voltage of the sampling MOS transistor has a stable voltage. When the bootstrapped switch in the "OFF" phase, the gate voltage of the sampling MOS transistor is GND. According to this characteristic, the gate voltage of sampling MOS transistor and *CLK* signal are used as observation signals.

Due to the bootstrapped switch in this study, in the "ON" phase, the gate voltage of the sampling MOS transistor is $2V_{DD}$. If the power supply voltage is 1.8V, then the gate voltage of the sample MOS transistor is 3.6V. Such a high voltage is not suitable for observation.

To solve this problem, a low power supply voltage is provided to the bootstrapped switch. As a result, an appropriate voltage can be obtained on the sampling MOS transistor

during the “ON” phase.

The testing strategy is if the response analysis module meets the following conditions, output “F = 0”, it indicates that the circuit is fault-free; otherwise output “F = 1”, indicates that the circuit has faults.

1. When “CLK = 1”, the gate voltage of the sampling MOS is a constant value. In this study, the value is determined by a window comparator.

2. When “CLK = 0”, the gate voltage of the sample MOS is GND. In this study, the GND is determined by a phase inverter.

The proposed BIST schematic is shown in Figure 2.2. The CLK signal of the bootstrapped switch and the gate voltage of the sampling MOS (V_G) are connected to the response analysis module as the input. The response analysis module analyzes the two-observation signal to determine whether the circuit has a fault. The EN is an enabling signal that controls whether the analysis module works. The power supply voltage of the bootstrapped switch is V_{DD1}. The power supply voltage of the response analysis is V_{DD2}.

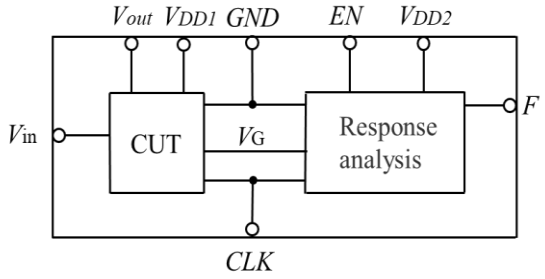


Figure 2.2 The proposed BIST schematic

The schematic of the response analysis module is shown in Figure 2.3. When “EN = 0”, the response analysis module is not working. The CLK signal and V_G signal do not affect the response analysis module. The output F is “1”. When “EN = 1”, the analysis module works. If the output is “1”, it indicates that the circuit is fault-free. If the output is “0”, it indicates that the circuit has faults. Because the bootstrapped switch is sensitive to the changes of V_G signal, a source follower is used to collect the V_G signal.

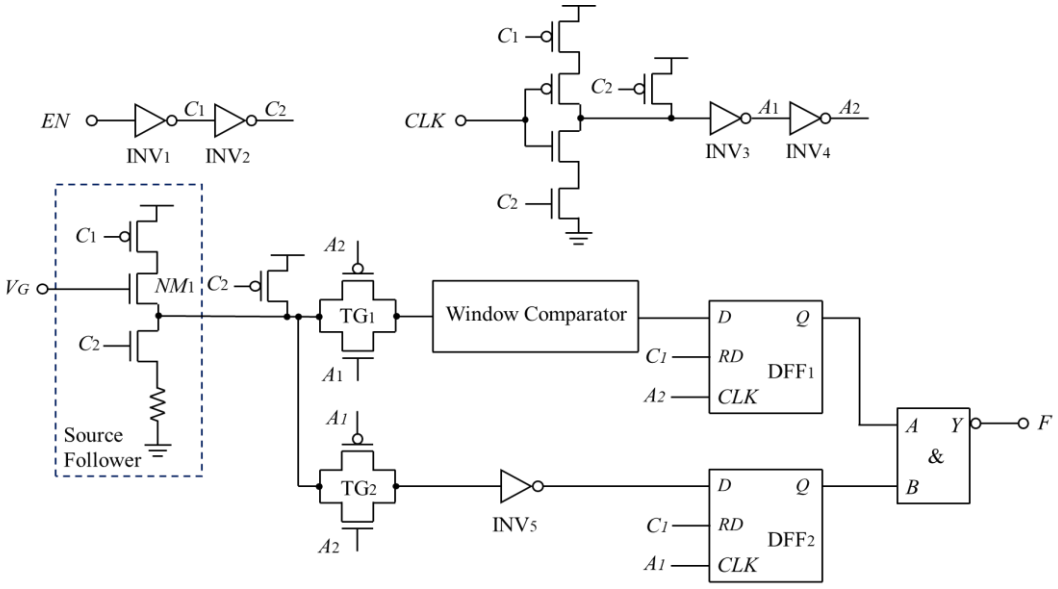


Figure 2.3 The schematic of the response analysis module

The schematic of the window comparator in [5] is shown in Figure 2.4. The window comparator outputs a high potential within the designed input range. The input range can be adjusted by adjusting the W/L of the four inverters.

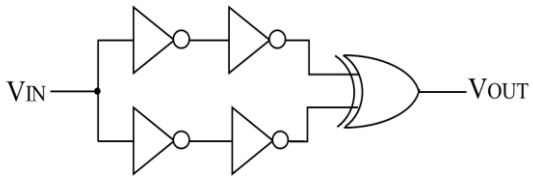


Figure 2.4 The schematic of the window comparator

2.4 Simulation Results

To obtain the influence information of BIST on the bootstrapped switch, the performance simulation of the bootstrapped switch with and without the test circuit was carried out. As shown in Figure 2.5, the bootstrapped switch and a 20-pF capacitor are combined into a track and hold circuit. The CUT schematic is shown in Figure 2.1. The schematic of CUT with BIST is shown in Figure 2.2.

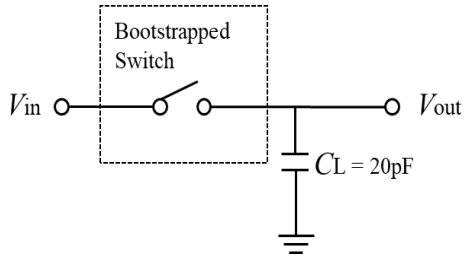


Figure 2.5 The performance simulation schematic for bootstrapped switch

The *CLK* signal is a 10 M Hz square wave and the input signal is a sine wave with an amplitude of 1.8 V and a frequency of 4.96 M Hz. After the spectrum analysis of the circuit, the performance parameters in Table 2.1 were obtained. The simulation results show that the BIST scheme has no obvious burden on the CUT. Note a slight decrease in SNR, which is due to the additional noise provided by NM_1. The V_{GS} of the M_S with BIST scheme is higher than that of the M_S without the BIST scheme, which results in the on-resistance of the M_S with the BIST scheme being lower than that of the M_S without the BIST scheme. Therefore, the parameters except SNR are slightly improved.

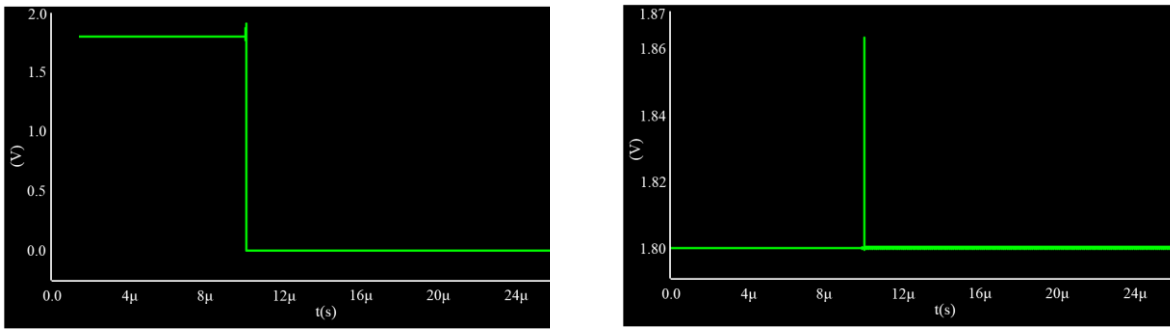
To evaluate the proposed BIST scheme, a fault attachment script was used to add the six faults to the MOS transistor of the bootstrapped switch except for the M_S. The fault of DSS, DO and SO of M_S does not cause voltage changes at the gate voltage of M_S which as observation voltage. Therefore, this BIST scheme cannot detect the fault of DSS, DO and SO of M_S. However, the M_S connects the input and output signals, a fault in the M_S can be easily detected by other methods. Therefore, the M_S is not used as a test object. The total number of fault circuits is 66.

Table 2.1 Parameters comparison with and without BIST circuit

Parameter	CUT	CUT with BIST
ENOB (bits)	9.45	9.46
SINAD (dB)	58.69	58.73
SNR (dB)	83.35	83.23
SFDR (dBc)	58.94	58.98
THD (dB)	−58.70	−58.74

The V_{DD1} and the input signal are set to 0.6 V, thus the V_G is approximately 1.56 V during the "ON" phase. Therefore, the output voltage of the source follower is carefully designed to be approximately 0.7 V, when the input voltage of the source follower is approximately 1.56 V. To cope with the possible deviation of the circuit manufacturing, the window voltage of the window comparator is designed to be 0.5 V to 0.9 V

Figure 2.6 shows the output signal by transient simulation. Figure 2.6(*a*) shows the result of fault-free. When BIST is off, the output is "*F* = 1"; when BIST is on, the output is "*F* = 0" which indicates that the circuit is fault-free. Figure 2.6(*b*) shows the result of a fault with gate-source short with the M_1. When BIST is off, the output is "*F* = 1"; when BIST is on, the output is "*F* = 1" which indicates that the circuit has faults.



(*a*) (*b*)

Figure 2.6 The output signal by transient simulation (*a*) fault-free; (*b*) fault with GSS with the M_1

Table 2.2 Simulation results of injected and defected fault

Fault Types	Injected Faults	Detected Faults
GDS	11	11
GSS	11	11
DSS[1]	11	10
GO[2]	11	4
DO	11	11
SO	11	11

[1] The undetected MOS transistors is M_2. [2] The undetected MOS transistors are M_1, M_2, M_3, M_4, M_5, M_9 and M_{10}.

Table 2.2 shows the simulation results with 66 test circuits. The fault coverage of the BIST scheme is approximately 87.9%. The 200 times Monte-Carlo simulation results show that the BIST scheme works well. Extreme process simulation results show that the fault coverage of the BIST scheme is approximately 75.8%, 78.8%, 89.4% and 84.8% at FF, FS, SS and SF corner, respectively.

2.5 Discussions and Conclusion

The function of M_2 is to relieve the pressure of M_1, that is, to prevent the drain-source voltage of M_1 from being greater than V_{DD}. M_2 can be equivalent to resistance. Therefore, the BIST scheme cannot be detected to the fault of DSS of M_2.

Note that the BIST scheme has low fault coverage for the gate open of the MOS transistor. This issue is discussed with the fault of GO of M_1.

Figure 2.7 shows the transient simulation of the gate voltage of M_1 with the fault of GO with M_1. Although the gate of M_1 is open, the gate voltage of M_1 is still high and low at the right time sequence due to the presence of parasitic capacitance. Therefore, M_1 can be turned on and off at the correct timing with the gate open. This indicates that the effect of this type of fault on the circuit is not catastrophic. However, this fault may still affect the circuit performance, and subsequent research will be carried out to address this issue.

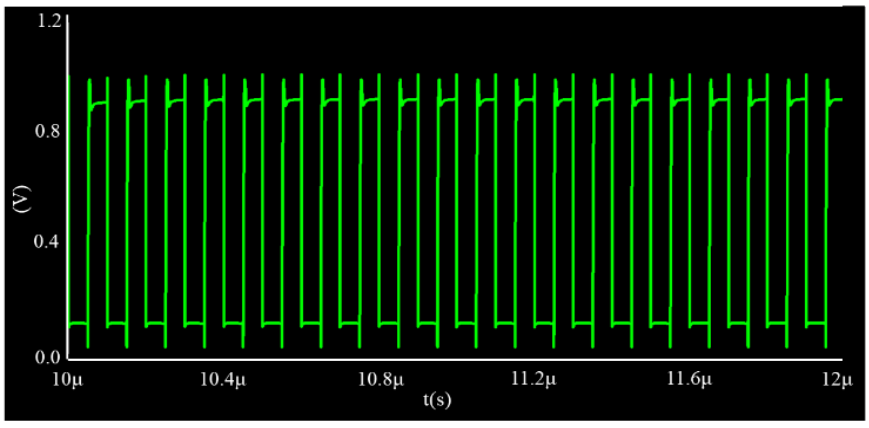


Figure 2.7 The gate voltage of M1 with the fault of GO of M1.

Bootstrapped switches are an indispensable type in analog circuits, but there are few fault diagnosis schemes for them. Thus, this dissertation proposed a bootstrapped switch BIST

scheme for detecting catastrophic faults. According to the characteristics of the bootstrap switch, the clock signal and the gate voltage of the sampling MOS transistor are used as the observation signals. However, the gate voltage of the sampling MOS transistor reaches $2V_{DD}$ during sampling, which is not conducive to observation. In this paper, the method of low power supply voltage is adopted to solve this problem. The proposed BIST scheme was designed and simulated in 0.18 μm CMOS technology. The HSPICE simulation results show that the fault coverage is approximately 87.9% with 66 test circuits. However, in the real circuit, the test result of this BIST scheme may be lower than the simulation results due to noise, technology, or any uncertainty. Therefore, we plan to test and evaluate the prototype chip after it is delivered in the future.

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3 A BIST Scheme for Dynamic Comparators

This chapter proposes a built-in self-test (BIST) scheme for detecting catastrophic faults in dynamic comparators. In this scheme, a feedback loop is designed using the characteristics of the comparator. By monitoring the voltage in the feedback loop to determine the presence of circuit fault. The proposed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the propose BIST scheme, six faults were injected into the real circuit. The test results are consistent with the simulation results.

3.1 Introduction

Test and diagnosis techniques develop with the progress of technology and the increase of integration. Built-in self-test (BIST) is one of most challenging techniques for the integrated circuits. BIST can help save cost on the first design [1-3].

Several BIST scheme were reported for performance or failure. A BIST circuit is proposed to obtain the attenuation/frequency distortion, the variation of gain with in-put level, and the signal-to-total distortion through the DAC to the ADC in [4]. A BIST circuit is proposed to fault diagnosis of ADC by code-width test in [5]. A BIST circuit is proposed to fault diagnosis of operational amplifier by Chaotic oscillation in [6]. A BIST circuit is proposed to fault diagnosis of sample-and-hold circuits based on the common-mode in [7]. However, there are still many mixed signal circuits that do not have a corresponding BIST scheme for fault diagnosis.

Comparator is a typical mixed signal circuit; its input is analog signal and the output is digital signal. As a special comparator, dynamic comparator is widely used because of its high speed and low power consumption. The test strategy is proposed for the offset of comparator

in [8-9].

However, there are few works on the fault diagnosis scheme for the dynamic comparator. In this work, a BIST scheme is proposed for detecting catastrophic faults in dynamic comparator. Section 3.2 previews the dynamic comparator under testing. Section 3.3 present the proposed BIST scheme. The simulation results and test results are set in section 3.4 and 3.5, respectively. Finally, Section 3.6 discusses the results and gives the conclusion.

3.2 The Circuit under Test

The dynamic comparator in [10] is shown in Figure 3.1 as the circuit under test (CUT). *CLK* is the clock signal, which controls the "RESET" phase and "COMPARE" phase of the dynamic comparator. V_N and V_P are the input signals for two comparison signals. ON and OP are the output signals for the comparison results.

In the "RESET" phase, *CLK* is logic "0". The voltage of nodes 1, 2, 3 and 4 are pulled up to V_{DD} via M_{10}, M_{11}, M_8 and M_9, respectively. The output signals O_N and O_P are both logic "0".

In the "COMPARE" phase, *CLK* is logic "1". The voltage of node 5 is pulled down to GND via M_1. The voltages of nodes 1 and 2 decrease from the V_{DD} at different rates, respectively. The descent rate depends on the magnitude of the input signals V_N and V_P, respectively. As the voltage of nodes 1 and 2 fall to V_{DD} - V_{THN}, the voltage of nodes 3 and 4 decrease from the V_{DD} at different rates, respectively. The descent rate depends on the magnitude of the voltage of nodes 1 and 2, respectively.

Due to the difference in the rate of descent, the node voltage that drops slowly will eventually be pulled up to V_{DD} by the latch structure $M_{4\text{-}7}$ until it stabilizes.

As amplifier with similar structure, there are many testing schemes, but few BIST schemes for dynamic comparators. Because of the latch structure, the output of the dynamic comparator only has logic "1" and logic "0". This special property leads to the difference between the properties of dynamic comparators and amplifier. Therefore, it is necessary to design a BIST scheme specifically for dynamic comparators.

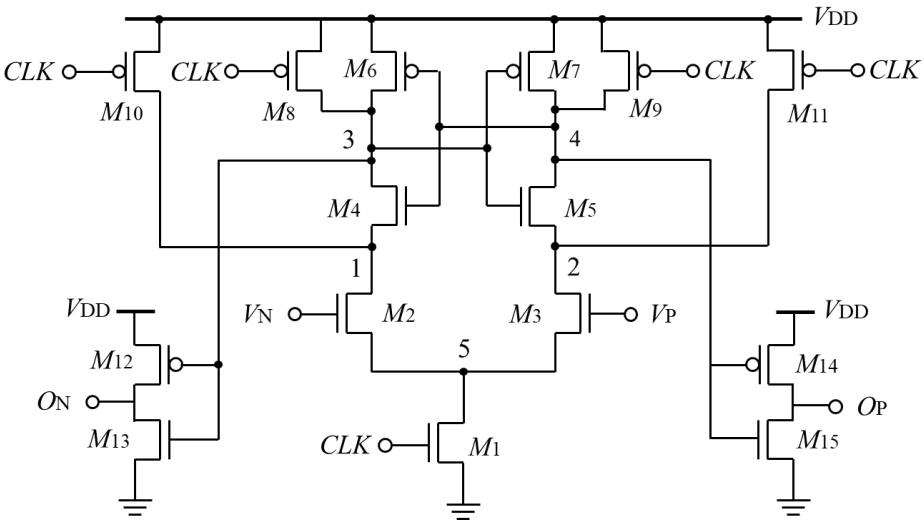


Figure 3.1 The dynamic comparator in [10].

3.3 The proposed BIST Scheme

The proposed BIST scheme for the dynamic comparator is shown in Figure 3.2. In this schematic, the properties of the comparator are used to establish a feedback loop, and by monitoring the voltage in the feedback loop to determine the presence of circuit fault.

When the BIST scheme work, *EN* is logic "1". Two NOR gates constitute an RS trigger. If V_P is greater than V_N, the O_P is logic "1" and the O_N is logic "0" in the "COMPARE" phase. Then, the voltage of node 6 will be logic "0". Then, the voltage of node 7 will increase via M_{13}. Until the voltage of node 7 is higher than V_P. Then, the O_P is logic "0" and the O_N is logic "1" in the "COMPARE" phase. Then, the voltage of node 6 will be logic "1". Then, the voltage of node 7 will reduce via M_{12}. Until the voltage of node 7 is lower than V_P. V_N will fluctuate repeatedly up and down around V_P.

Therefore, the voltage of the V_N can be monitored to determine whether there is a fault in the circuit. If the voltage of V_N fluctuates around V_P in a range, the circuit is fault-free, and this causes the window comparator to output logic "1". Otherwise, the window comparator outputs logic "0". According to the simulation results, the window boundary of the window comparison was designed to be 0.85V to 0.95V

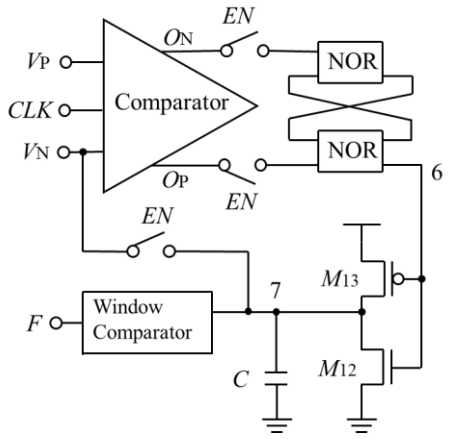


Figure 3.2 The proposed BIST scheme for dynamic comparator.

The structure of the window comparator in [11], which is used in this case is shown in Figure 3.3. The window comparator compares the input voltage to the window boundary. The Window boundary is determined by lower limit voltage (V_L) and upper limit voltage (V_H). If the input signal (V_{IN}) is between the lower limit voltage (V_L)and upper limit voltage (V_H), the output signal is logic "1". If the input signal (V_{IN}) is lower than the lower limit voltage (V_L) or higher than the upper limit voltage (V_H), the output signal is logic "0". The window boundary can be adjusted by adjusting the W/L of the four inverters.

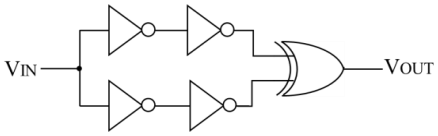


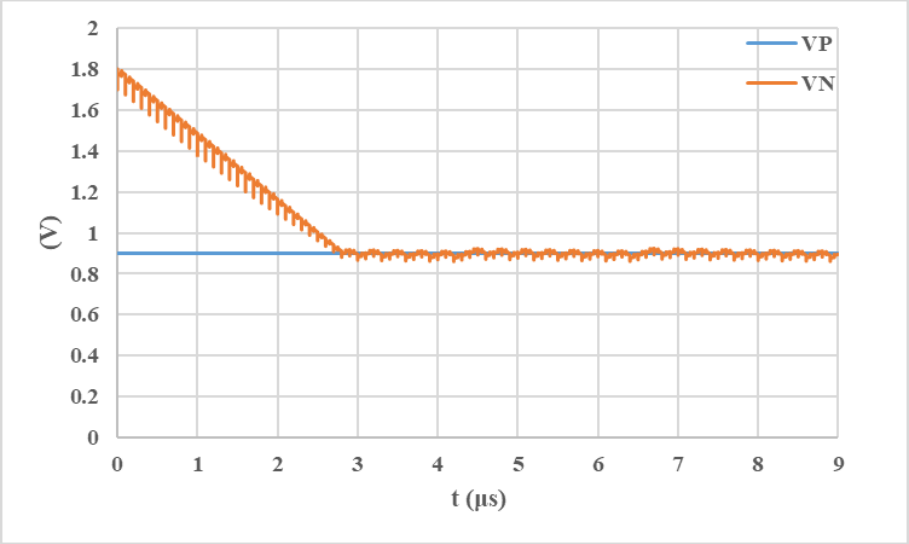
Figure 3.3 The structure of the window comparator in [11].

3.4 Simulation Results

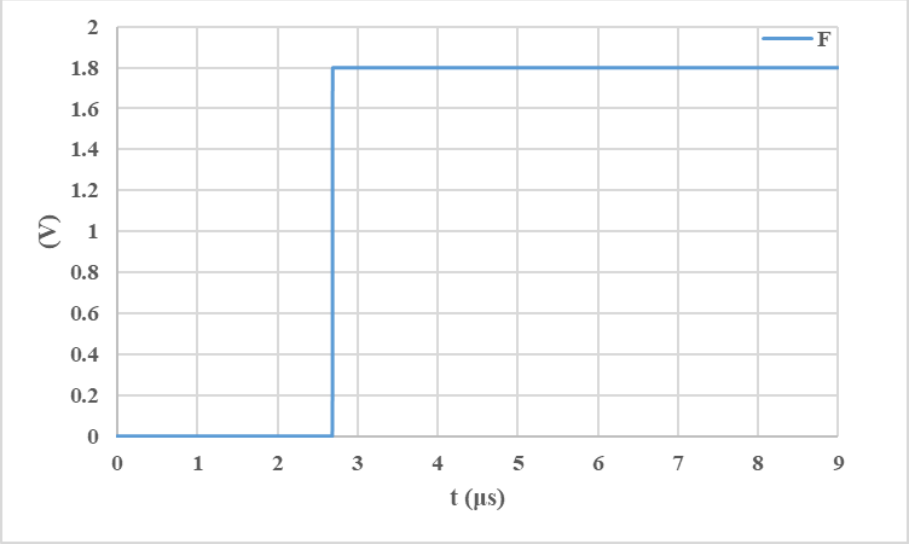
In this case, all possible catastrophic short and open faults with MOS transistors were considered. The short fault was performed by a serial connection with a 10 Ω resistor, and the open fault was performed by a parallel connection with a 10M Ω resistor and a 100f F capacitor. The six types of catastrophic faults were gate-drain short (GDS), gate-source short (DSS), drain-source short (DSS), gate open (GO), drain open (DO), and source open (SO). Moreover, only a signal fault was injected in the simulation, and the total number of fault circuits was 90.

Figure 3.4 shows the simulation results of the fault-free state. Figure 3.4(*a*) and Figure 3.4(*b*) are the transient simulation waveforms of V_N and V_P and *F*, respectively. At the

beginning of the test, the voltage of V_N is much higher than that of V_P. Furthermore, the output signal V_N is outside the window. Therefore, the output signal F is logic "0". Because of the feedback system, the voltage of V_N continues to drop and finally enters the oscillation interval, fluctuating around the voltage value of V_P. Furthermore, the output signal V_N is in the window. Therefore, the output signal F becomes logic "1". The faulty circuits with GOs of $M_{1,8\text{-}15}$ showed similar results.



(*a*)

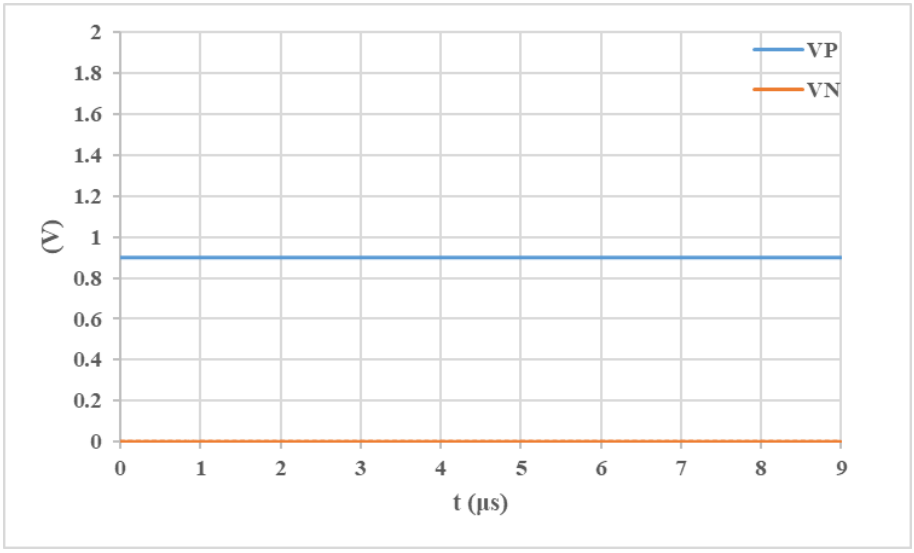


(*b*)

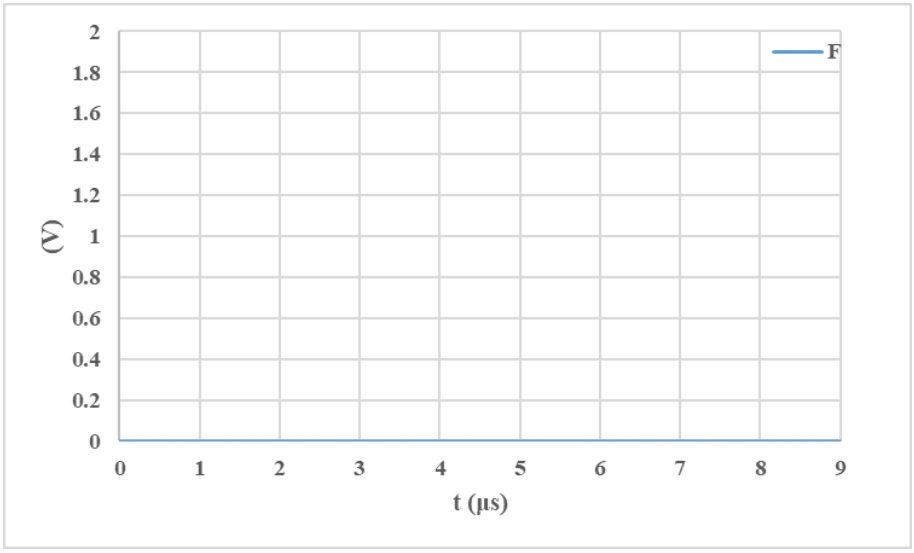
Figure 3.4 The fault-free simulation result. (*a*) V_P and V_N signal (*b*) F signal

The first fault type is when the voltage of V_N is always lower than 0.85V, which is the

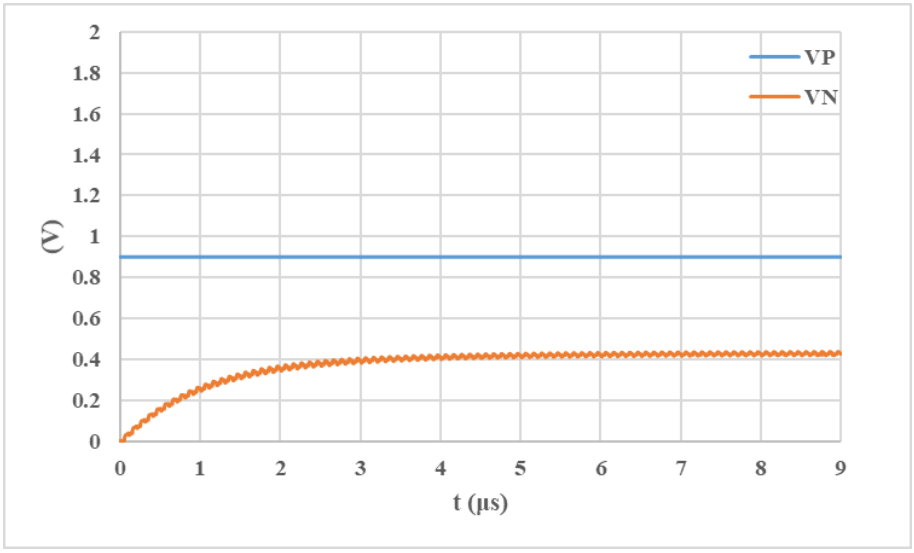
lower bound of the comparator window. The output signal F is always logic "0", which indicates the circuit has a fault. Figure 3.5(a) and Figure 3.5(b) show the simulation result of the faulty circuit with a GDS of M_1. The faulty circuits with GSSs of $M_{8\text{-}11,13}$ showed similar results. Figure 3.5(c) and Figure 3.5(d) show the simulation result of the faulty circuit with a GDS of M_{10}. The faulty circuits with GDSs of $M_{12,13}$ and a DSS of M_{12} showed similar results.



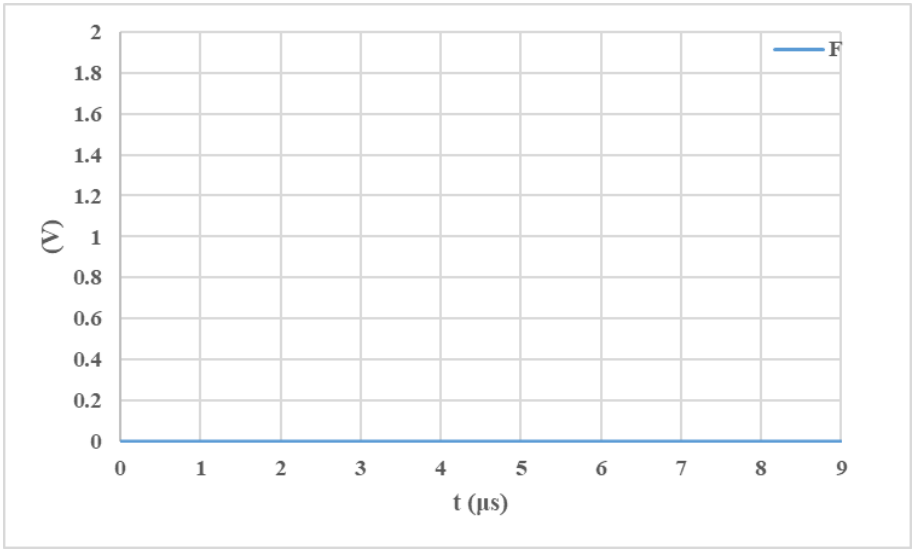
(a)



(b)



(*c*)

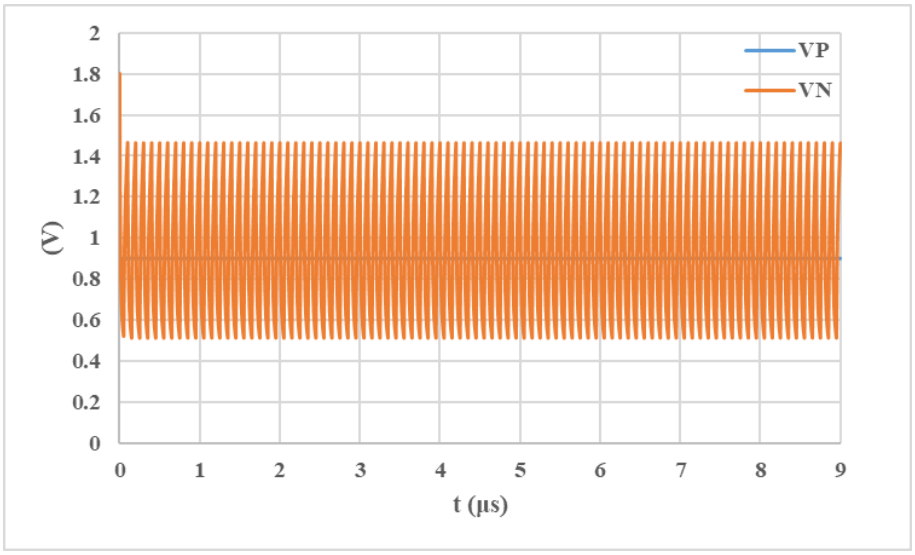


(*d*)

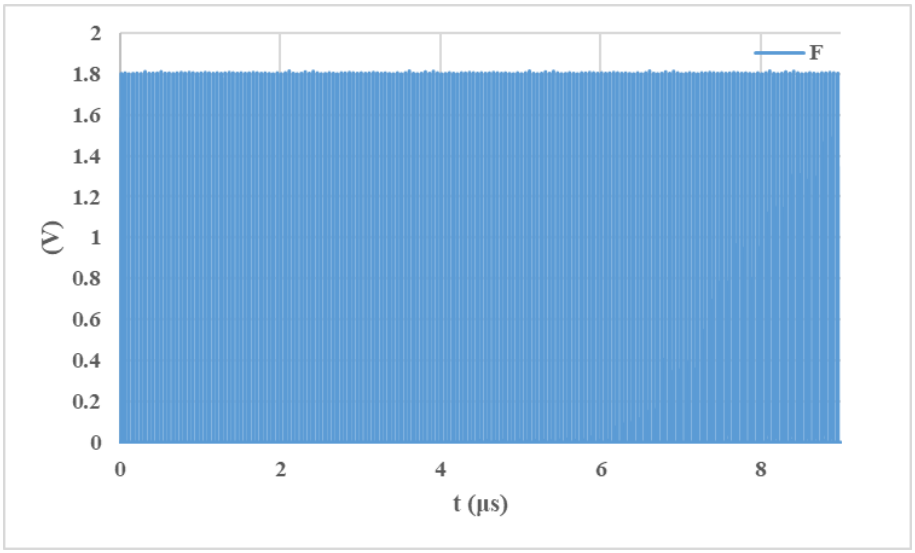
Figure 3.5 The first fault type. (*a*) VP and VN signal of faulty circuit with a GDS of M1, (*b*) F signal of faulty circuit with a GDS of M1, (*c*) VP and VN signal of faulty circuit with a GDS of M10, and (*d*) F signal of faulty circuit with a GDS of M10.

The second fault type is that the oscillating range of the V_N voltage crosses the window boundary of the window comparator. The output signal *F* has a periodic pulse, which indicates the circuit has a fault. Figure 3.6(*a*) and Figure 3.6(*b*) show the simulation result of the faulty circuit with a GDS of M_2. Figure 3.6(*c*) and Figure 3.6(*d*) show the simulation result of the faulty circuit with a DO of M_8. The faulty circuits with SOs of $M_{8,9}$ showed similar results. Figure 3.6(*e*) and Figure 3.6(*f*) show the simulation result of the faulty circuit

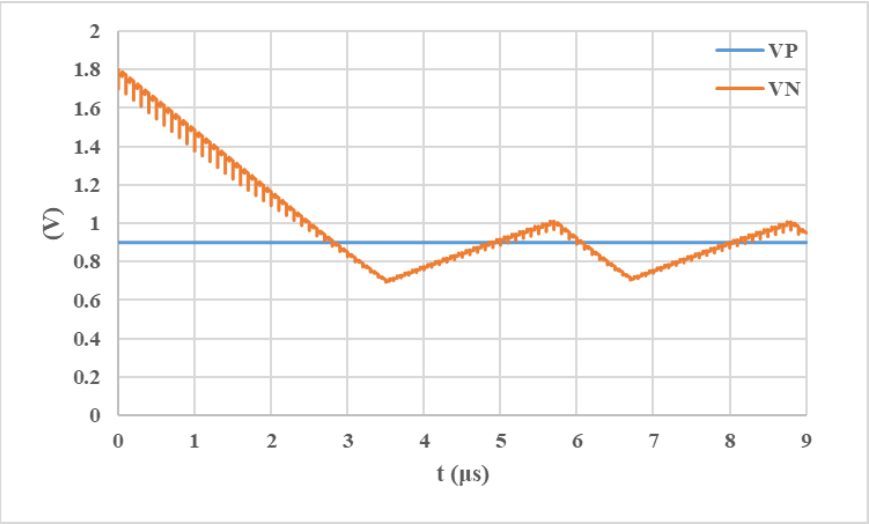
with a DO of M_{11}. The faulty circuits with a GO of M_7 and SOs of $M_{7,11}$ showed similar results. Figure 3.6(*g*) and Figure 3.6(*h*) show the simulation result of the faulty circuit with a SO of M_6. The faulty circuits with a SO of M_{10} showed similar results.



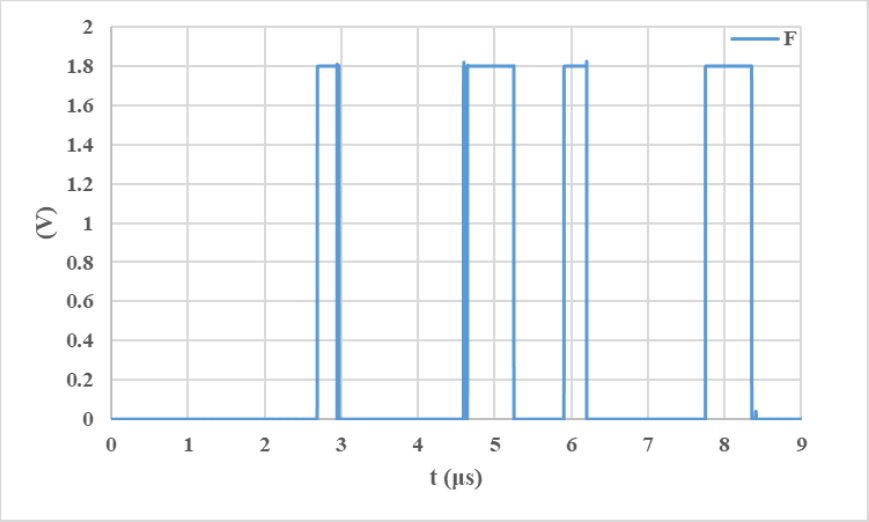
(*a*)



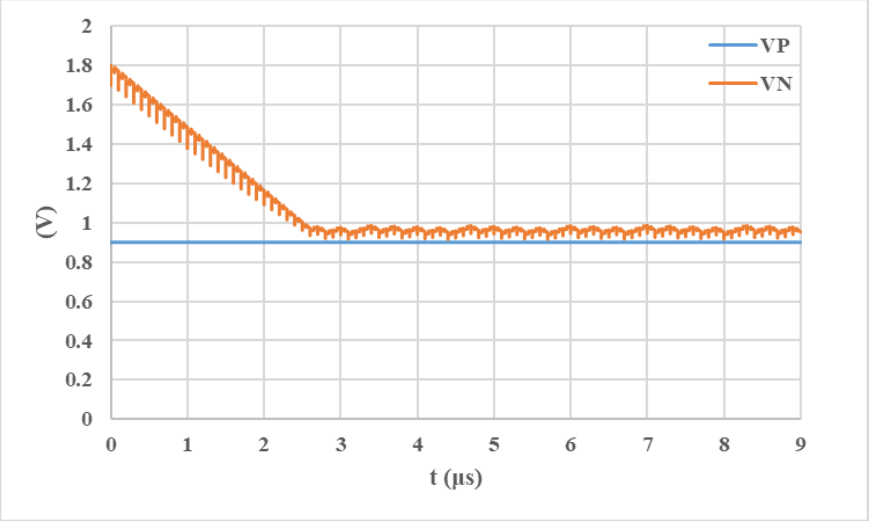
(*b*)



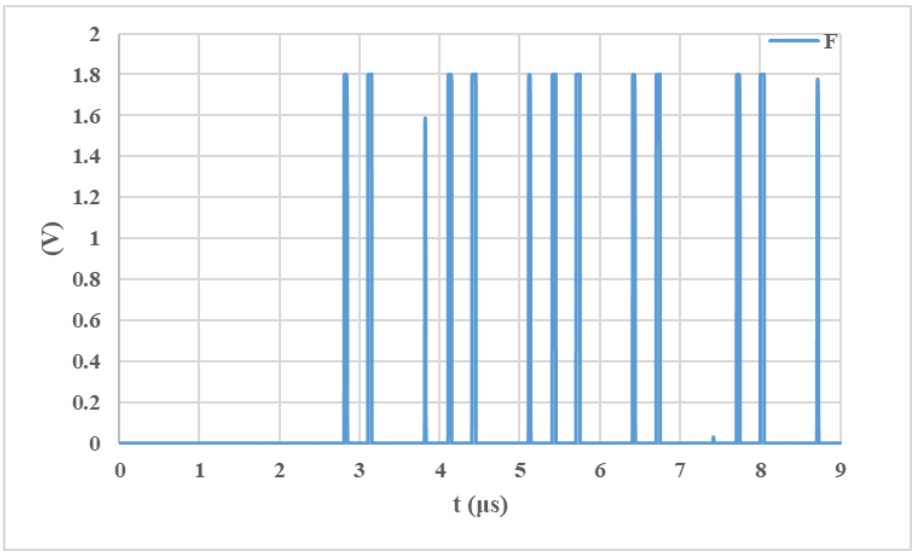
(*c*)



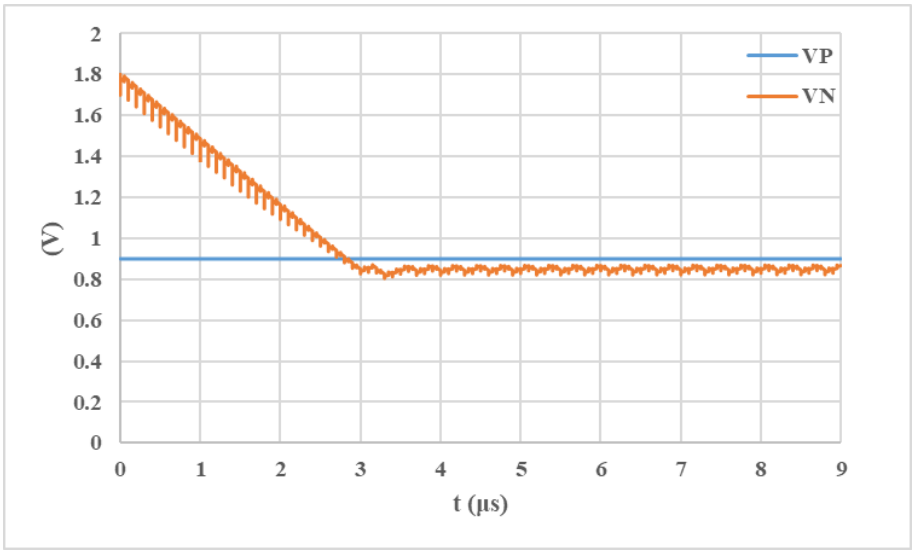
(*d*)



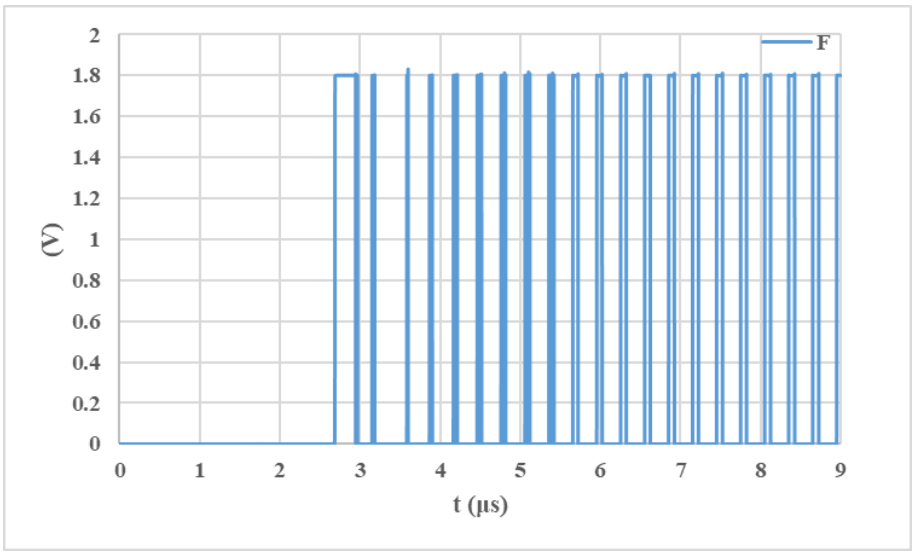
(*e*)



(*f*)



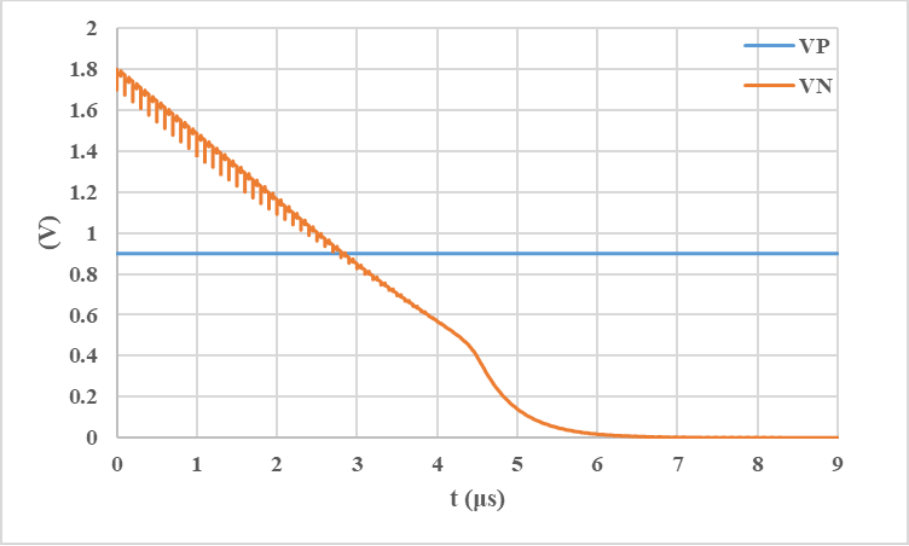
(*g*)



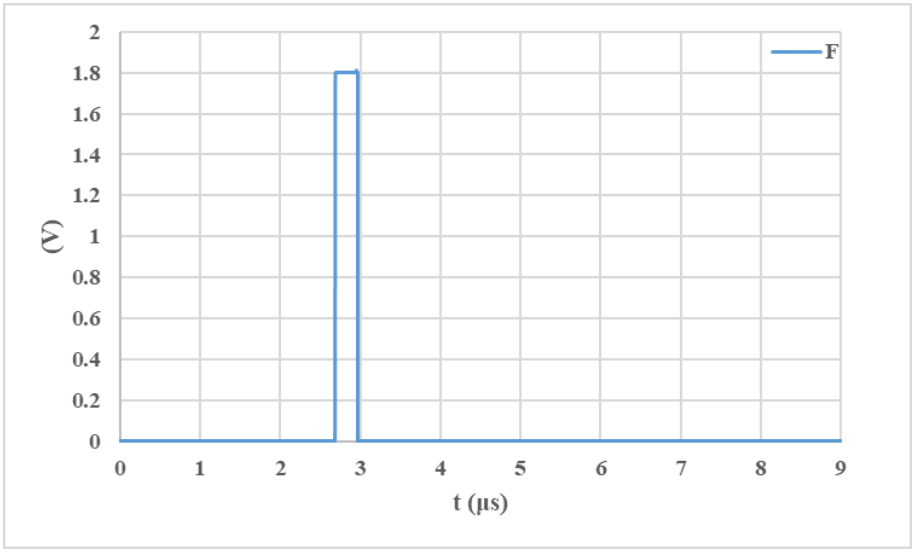
(*h*)

Figure 3.6 The second fault type. (*a*) V_P and V_N signal of faulty circuit with a GDS of M_2, (*b*) *F* signal of faulty circuit with a GDS of *M2*, (*c*) V_P and V_N signal of faulty circuit with a DO of M_8, (*d*) *F* signal of faulty circuit with a DO of M_8, (*e*) V_P and V_N signal of faulty circuit with a DO of M_{11}, (*f*) *F* signal of faulty circuit with a DO of M_{11}, (*g*) V_P and V_N signal of faulty circuit with an SO of M_6, And (*h*) *F* signal of faulty circuit with an SO of M_6.

The third fault type is when the voltage of V_N crosses the upper and lower boundaries of the window comparator a finite number of times. The output signal *F* has a finite pulse, which indicates the circuit has a fault. Figure 3.7(*a*) and Figure 3.7(*b*) show the simulation result of the faulty circuit with a GDS of M_3. The faulty circuits with GDSs of $M_{4\text{-}7}$, DSSs of $M_{2,7,9,11,15}$, GSSs of $M_{1,5,6,14}$, DOs of $M_{3,5,14}$, and SOs of $M_{3,5,14}$ showed similar results. Figure 3.7(*c*) and Figure 3.7(*d*) show the simulation result of the faulty circuit with a GDS of M_8. The faulty circuits with an SO of M_{12} showed similar results. Figure 3.7(*e*) and Figure 3.7(*f*) show the simulation result of the faulty circuit with a DSS of M_{13}. The faulty circuits with a DO of $M_{9,12}$ showed similar results. Figure 3.7(*g*) and Figure 3.7(*h*) show the simulation result of the faulty circuit with a DSS of M_4. The faulty circuits with GDSs of $M_{9,11}$, a GSS of M_2, a GO of M_3, and DOs of $M_{6,10,13}$ showed similar results.



(*a*)



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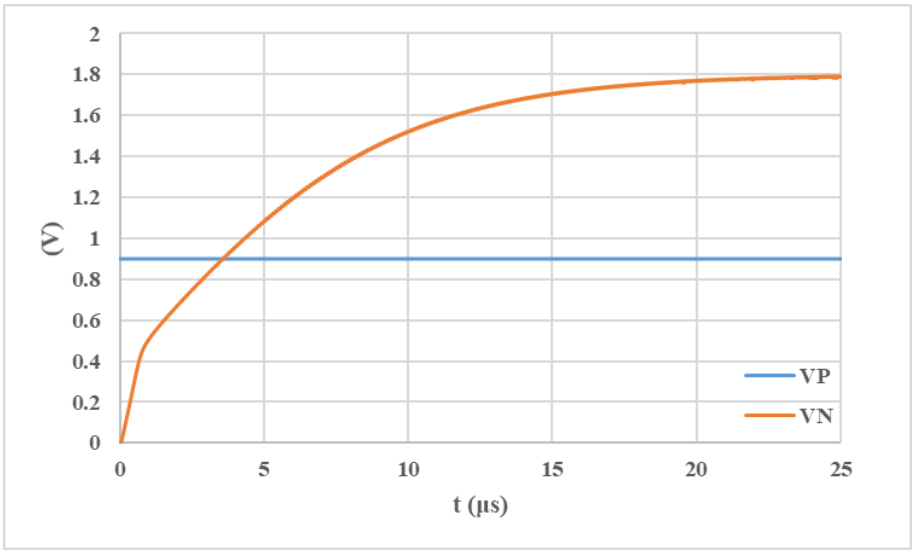

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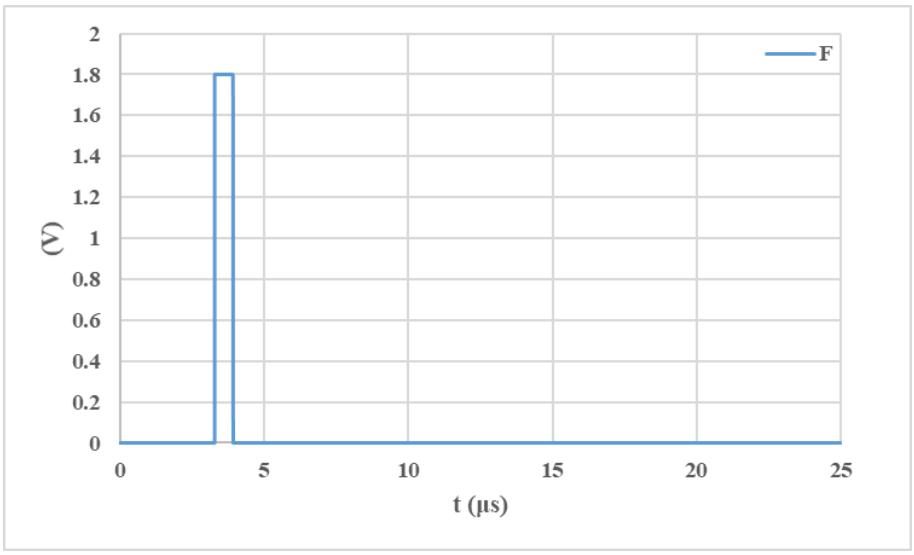
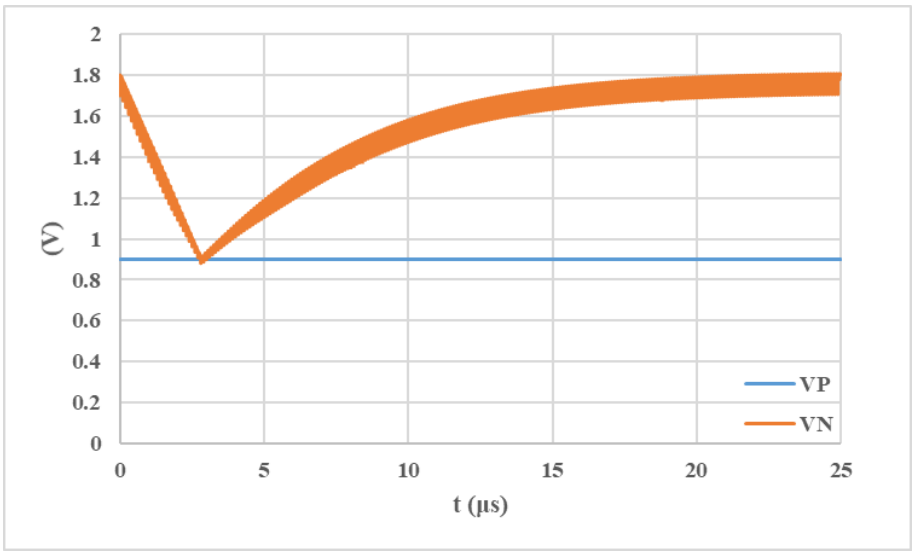


(*d*)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1.2
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25
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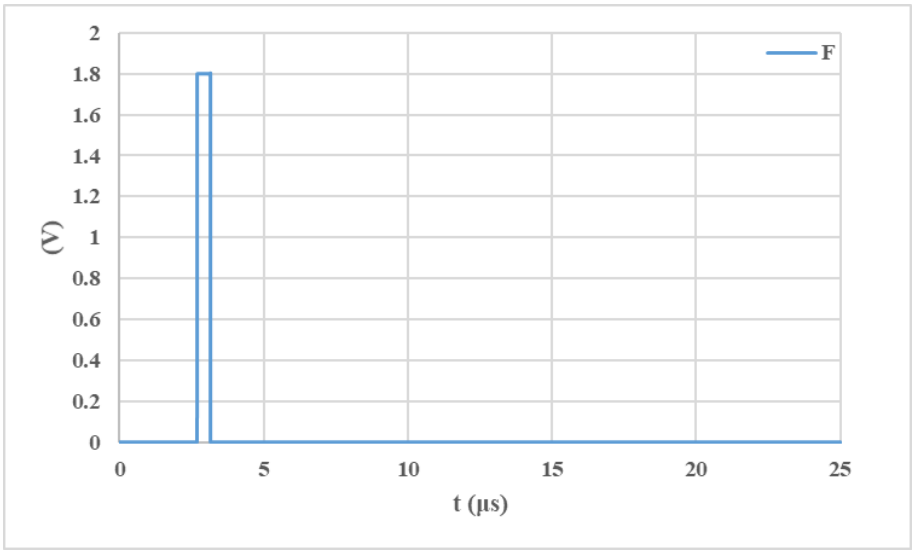
VP
VN

(*e*)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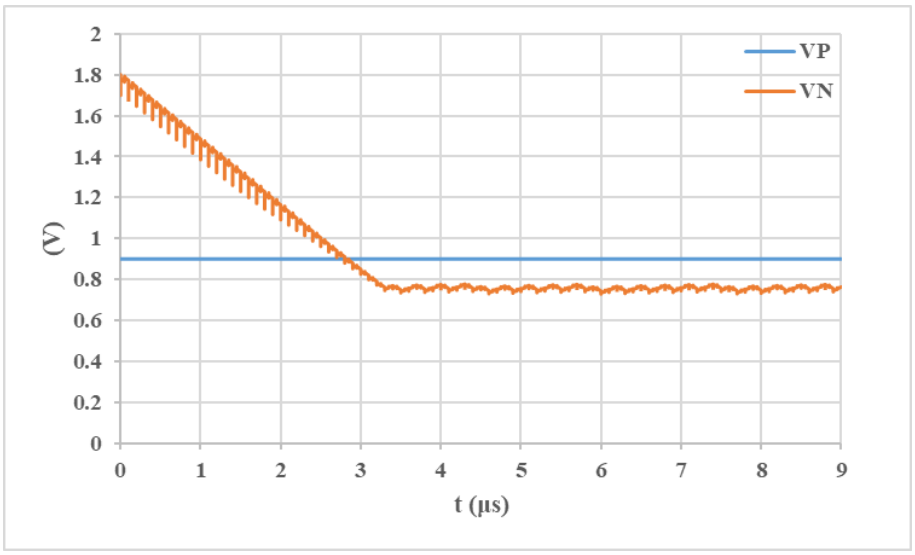
(*f*)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3
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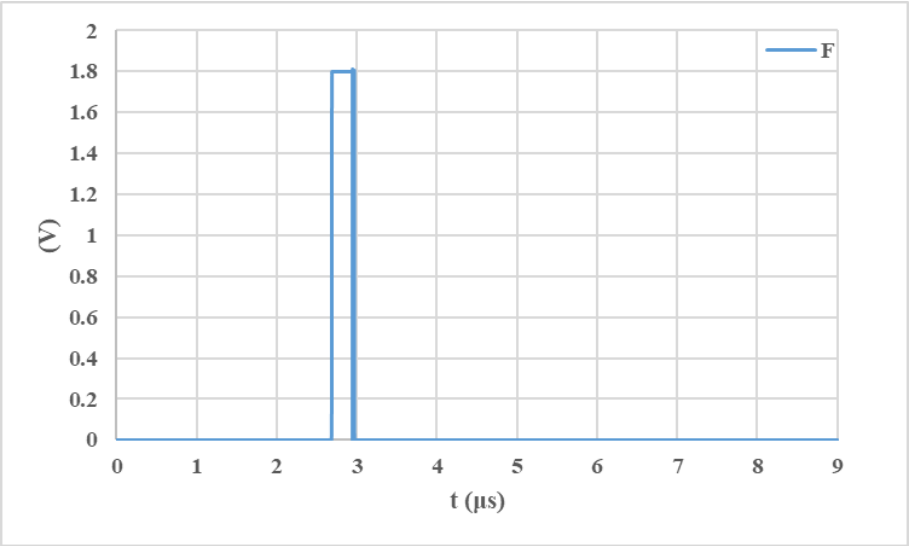
9
t (µs)
VP
VN

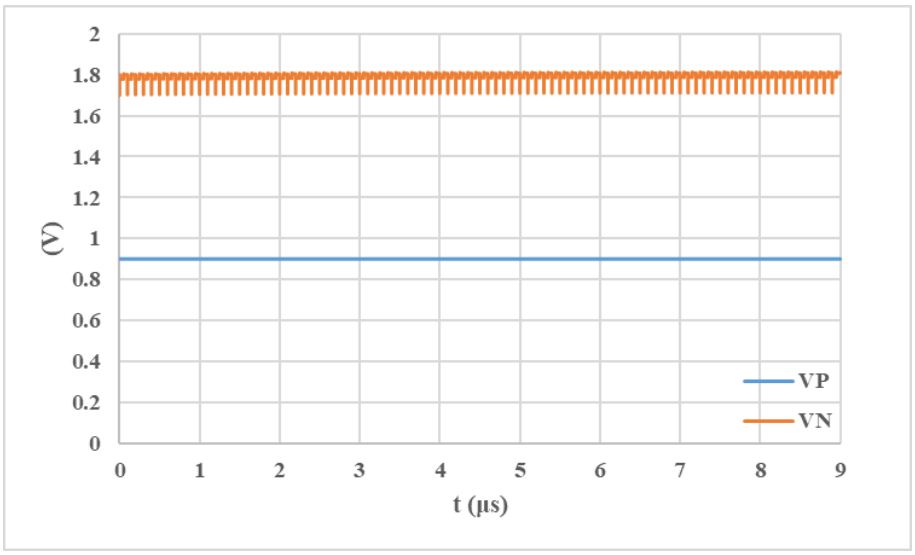
(*g*)



(*h*)

Figure 3.7 The third fault type. (*a*) V_P and V_N signal of faulty circuit with a GDS of M_3, (*b*) *F* signal of faulty circuit with a GDS of M_3, (*c*) V_P and V_N signal of faulty circuit with a GDS of M_8, (*d*) *F* signal of faulty circuit with a GDS of M_8, (*e*) V_P and V_N signal of faulty circuit with a DSS of M_{13}, (*f*) *F* signal of faulty circuit with a DSS of M_{13}, (*g*) V_P and V_N signal of faulty circuit with a DSS of M_4, and (*h*) *F* signal of faulty circuit with a DSS of M_4.

The fourth fault type is when the voltage of V_N is always higher than 0.95 V, which is the upper bound of the comparator window. The output signal *F* is always logic "0", which indicates the circuit has a fault. Figure 3.8(*a*) and Figure 3.8(*b*) show the simulation result of the faulty circuit with a GDS of M_{14}. The faulty circuits with a GDS of M_{15}, DSSs of $M_{1,3,6,8,10,14}$, GSSs of $M_{3,4,7,12,15}$, DOs of $M_{1,2,4,15}$, and SOs of $M_{1,2,4,15}$ showed similar results. Figure 3.8(*c*) and Figure 3.8(*d*) show the simulation result of the faulty circuit with a DSS of M_5. The faulty circuits with a DO of M_7 showed similar results.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8
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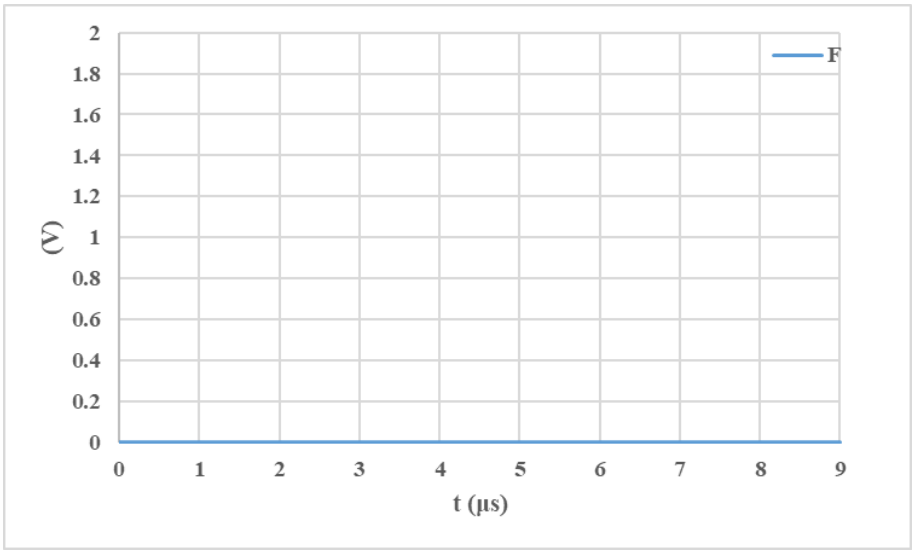
VP
VN

(*a*)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7
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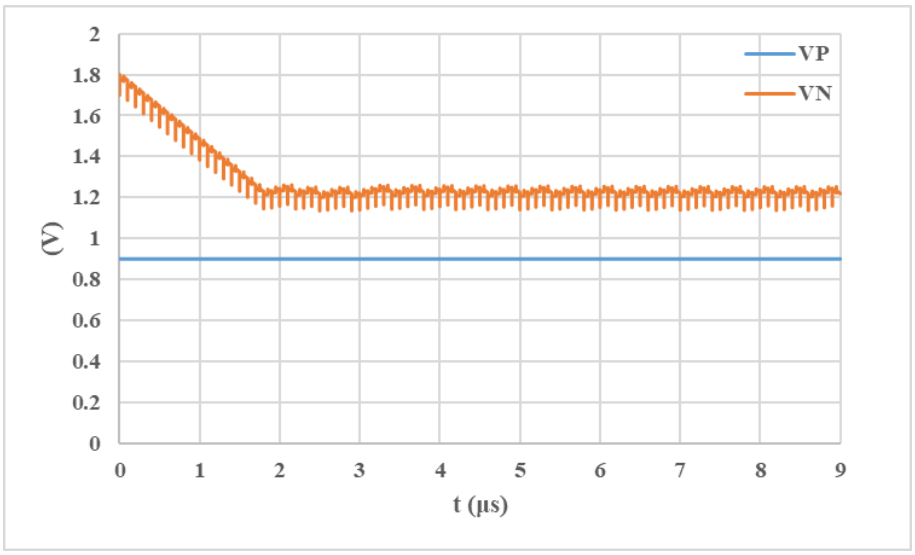
9
t (µs)
F

(*b*)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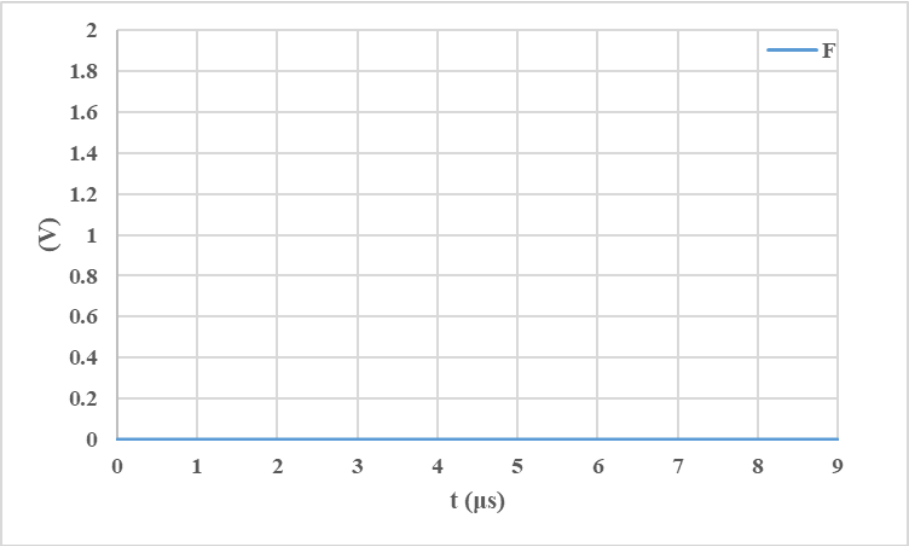
t (µs)
VP
VN

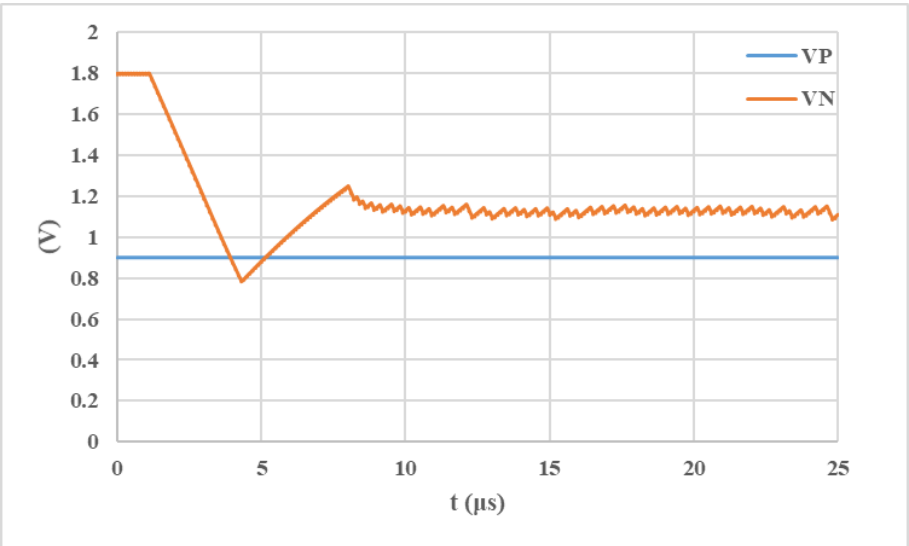
(*c*)



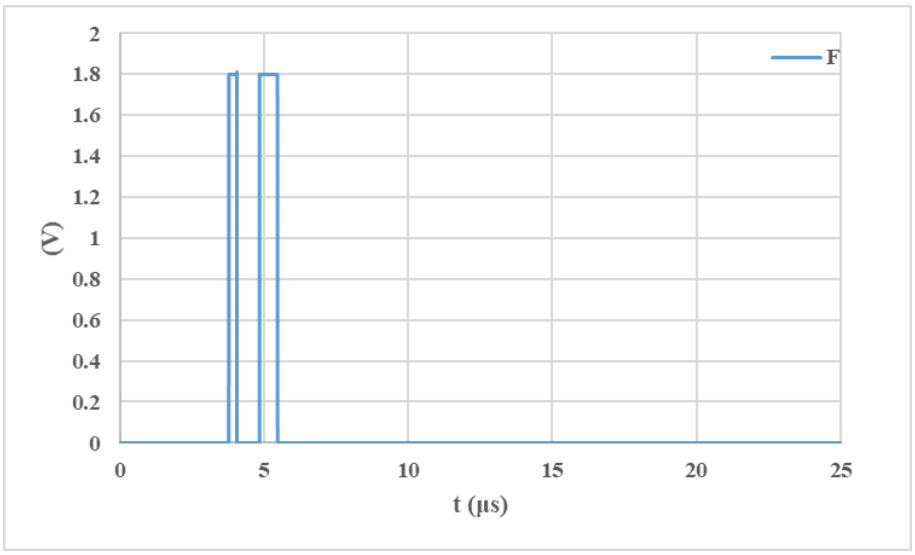
(*d*)

Figure 3.8 The fourth fault type. (*a*) V_P and V_N signal of faulty circuit with a GDS of M_{14}, (*b*) *F* signal of faulty circuit with a GDS of M_{14}, (*c*) V_P and V_N signal of faulty circuit with a DSS of M_5, and (*d*) *F* signal of faulty circuit with a DSS of M_5.

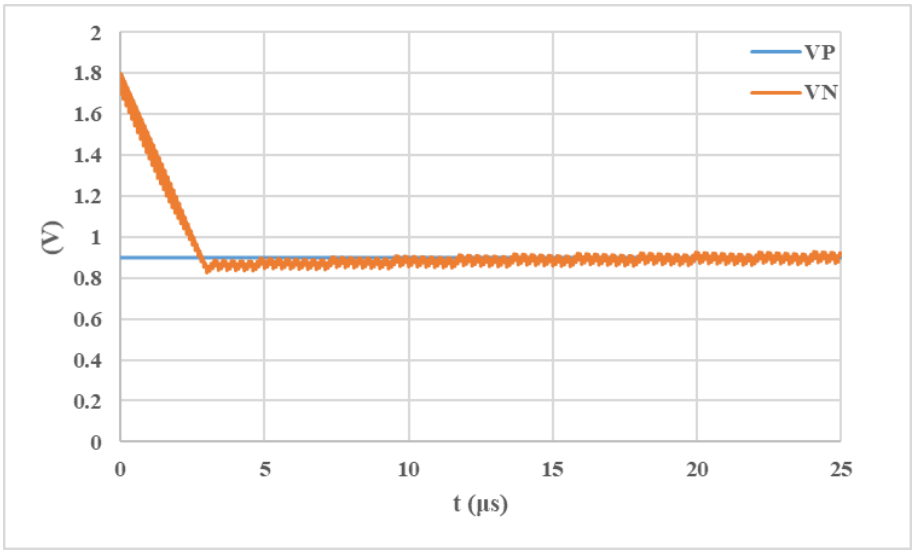
Figure 3.9(*a*) and Figure 3.9(*b*) show the simulation result of the faulty circuit with a GO of M_2. Figure 3.9(*c*) and Figure 3.9(*d*) show the simulation result of the fault circuit with a GO of M_4. The faulty circuits with a GO of M_6 showed similar results. Figure 3.9(*e*) and Figure 3.9(*f*) show the simulation result of the faulty circuit with a GO of M_5. Considering that in the actual test, if the output signal *F* performs a limited pulse it may not be observed, the GO fault types of $M_{4,6}$ were regarded as undetected.



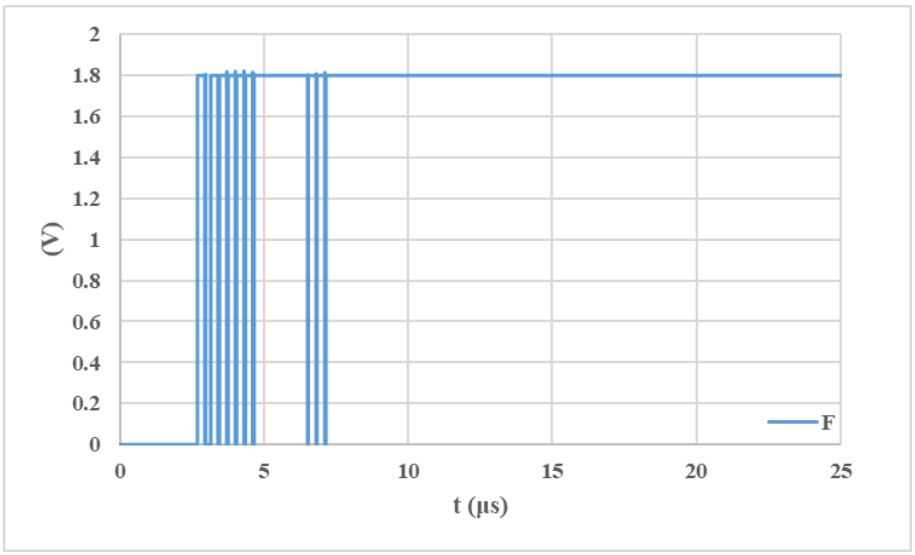
(*a*)


F
(V)
t (µs)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
5
10
15
20
25

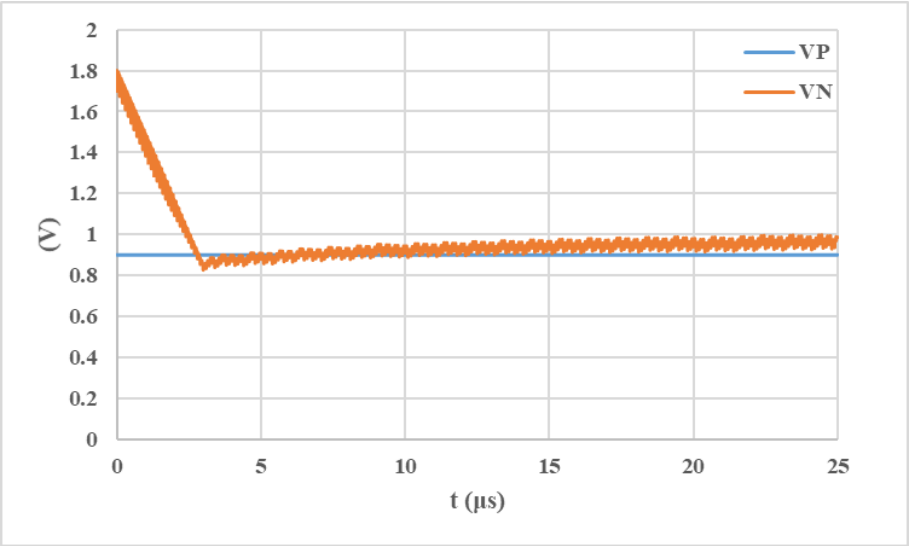
(*b*)


VP
VN
(V)
t (µs)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
5
10
15
20
25

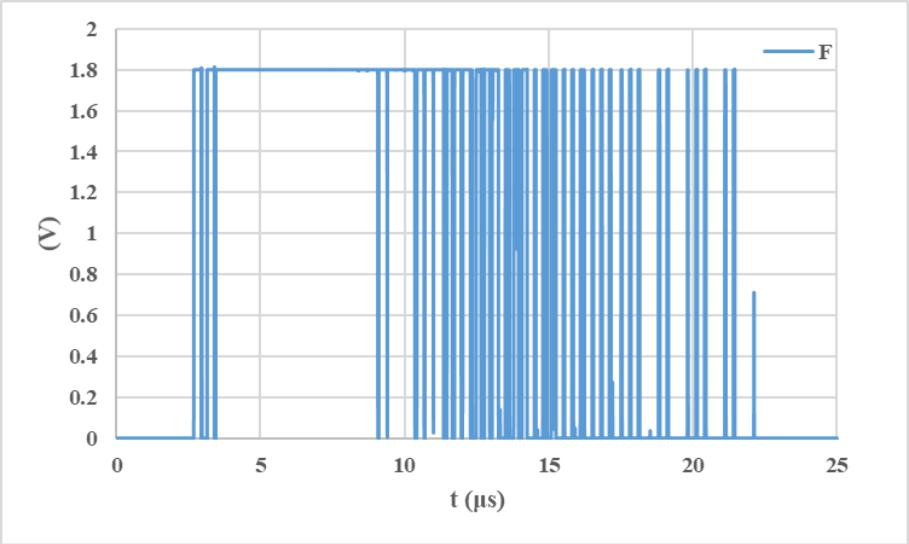
(*c*)


F
(V)
t (µs)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
5
10
15
20
25

(*d*)



(*e*)



(*f*)

Figure 3.9 The fifth fault type. (*a*) V_P and V_N signal of faulty circuit with a GDS of M_{14}, (*b*) *F* signal of faulty circuit with a GDS of M_{14}, (*c*) V_P and V_N signal of faulty circuit with a DSS of M_5, (*d*) *F* signal of faulty circuit with a DSS of M_5, (*e*) V_P and V_N signal of faulty circuit with a GO of M_5, and (*f*) *F* signal of faulty circuit with a GO of M_5

In summary, there are three scenarios for the *F* signal. The first case is the steady state of logic "1" at the end; the second case is the steady state of logic "0" at the end; and the third case is to always transform between logic "0" and logic "1". The first case is recorded as fault-free, and the other two cases are recorded as fault recognition. The simulation results shown in Table 3.1 were determined by the results after 25 µs. The simulated fault coverage is approximately 87.8% with 90 test circuits.

Table 3.1 Simulation results of injected and detected fault.

Fault Types	Injected Faults	Detected Faults
GDS	15	15
GSS	15	15
DSS	15	15
GO [1]	15	4
DO	15	15
SO	15	15

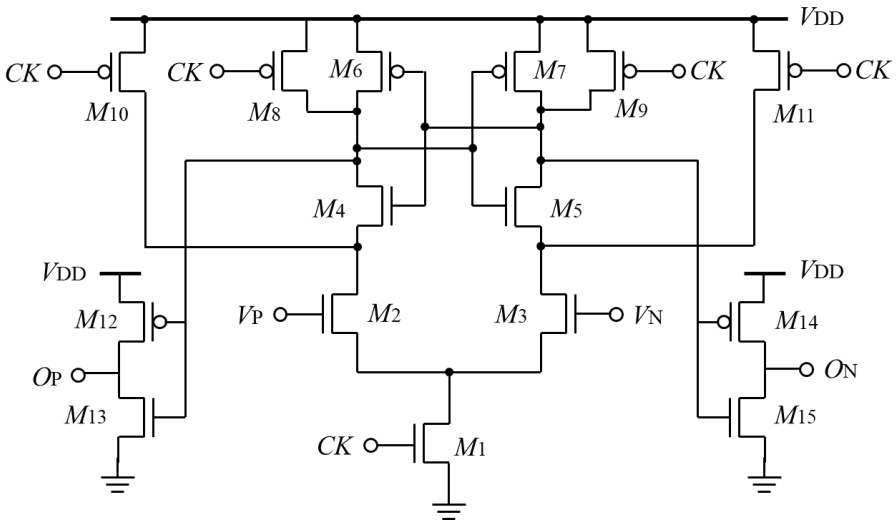
[1] The detected MOS transistors are M_2, M_3, M_5, and M_7.

3.5 Test results

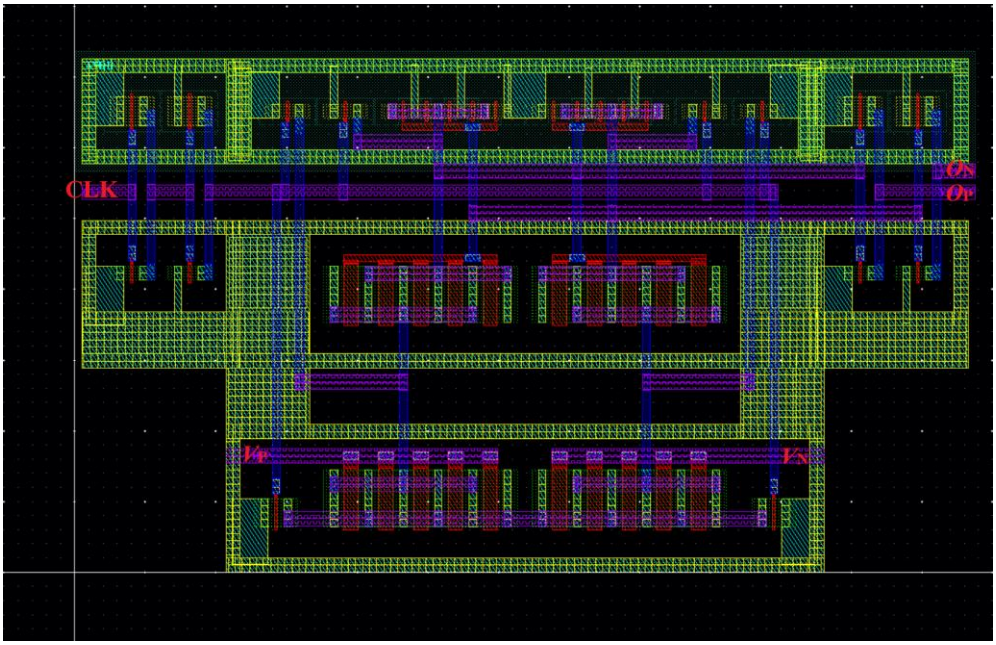
To further verify the feasibility of the BIST scheme, one fault-free circuit and six faulty circuits were implemented in ROHM 180nm CMOS technology. The specific six fault circuits were DO of M_1, GO of M_2, SO of M_3, DSS of M_4, GDS of M_5, and GSS of M_6.

3.5.1 The circuit under test

Figure 3.10 shows the schematic and layout design of the fault-free circuit. The circuit layout is divided into four parts, the first part is the input buffer ($M_{16\text{-}19}$) of the *CLK* signal; the second part is the input MOS transistor ($M_{2,3}$) and the switch (M_1), the third part is the back-to-back inverter ($M_{4\text{-}7}$) and the switch ($M_{8\text{-}11}$), the fourth part is the output buffer ($M_{12\text{-}15}$). The whole layout adopts a symmetrical structure, the overall current flow from top to bottom.



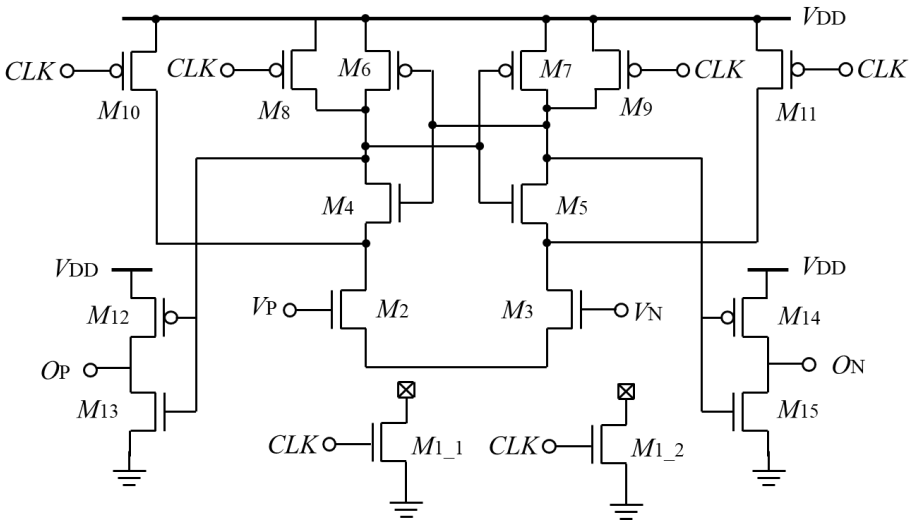
(*a*)



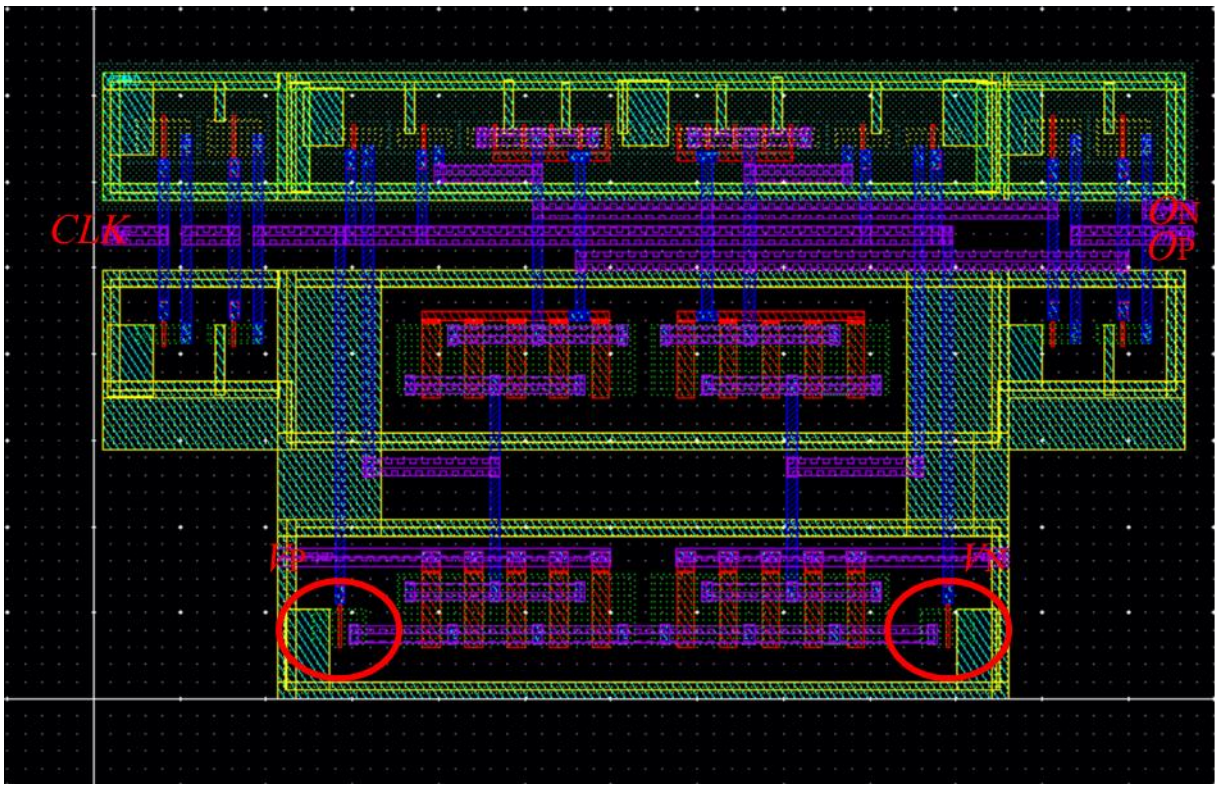
(*b*)

Figure 3.10 The schematic and layout design of the fault-free circuit. (*a*) the schematic of the circuit, (*b*) the layout of the fault-free circuit

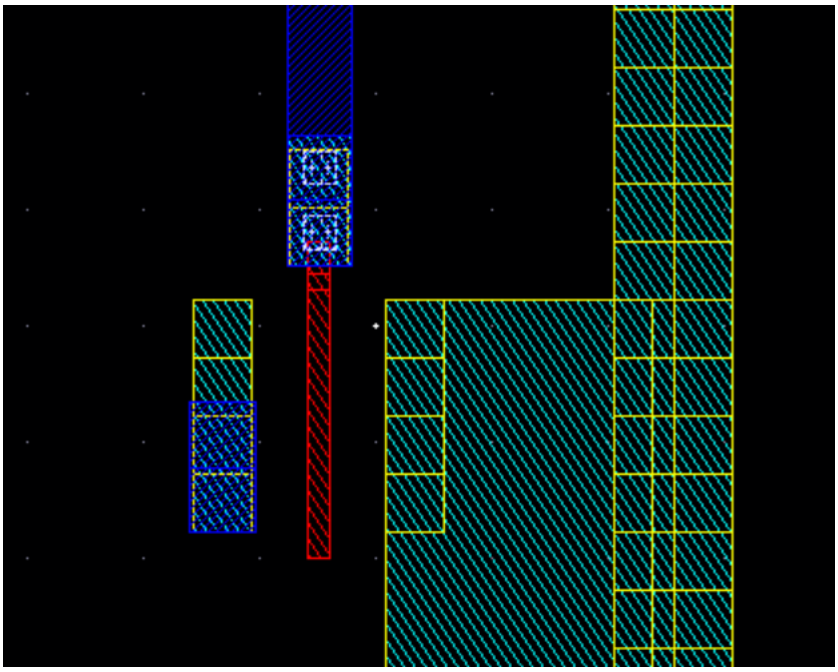
Figure 3.11 shows the schematic and layout of the injection fault type of DO of M_1. Because M_1 was divided into two parallel MOS transistors in the actual layout design, the corresponding schematic was changed to that shown in Figure 3.11(*a*) and Figure 3.11(*b*). The open drain of the M_1 transistor is designed to remove the connecting holes between the first and second layers of metal. The detail was shown in Figure 3.11(*c*).


VDD
CLK
CLK
M6
M7
CLK
CLK
M10
M8
M9
M11
M4
M5
VDD
VDD
M12
VP
M2
M3
VN
M14
OP
ON
M13
M15
CLK
M1_1
CLK
M1_2

(*a*)


CLK
ON
OP

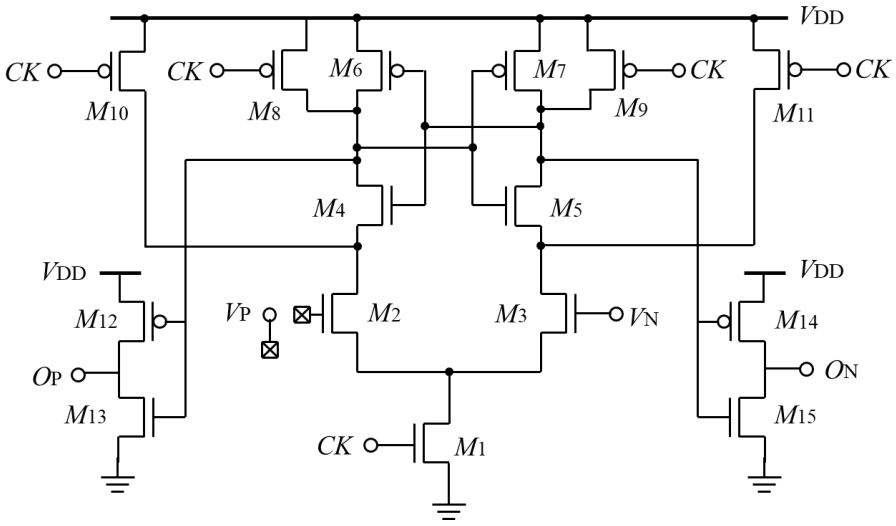
(*b*)



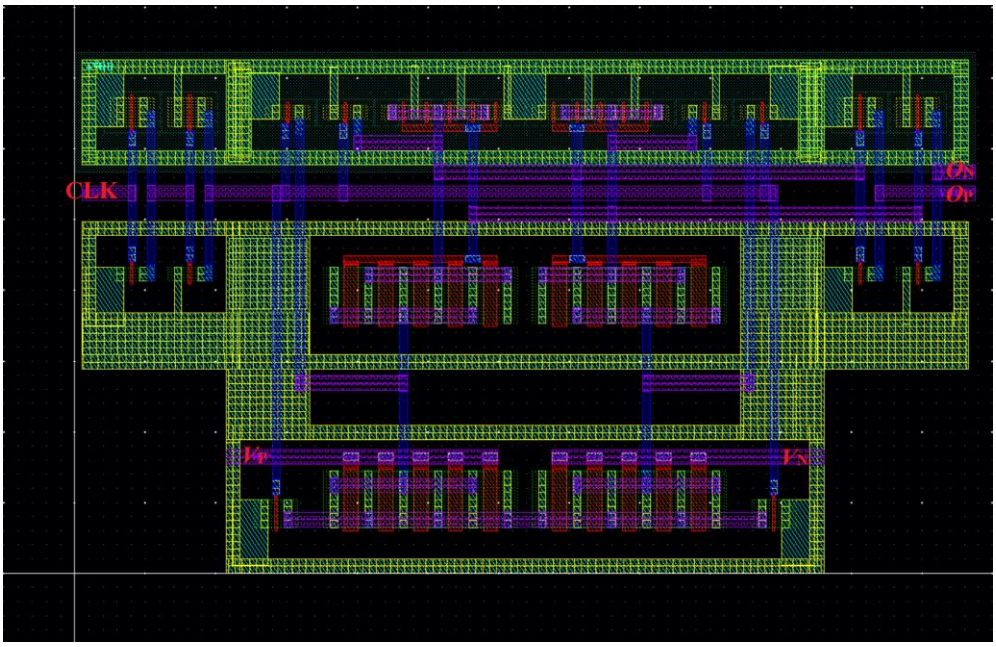
(*c*)

Figure 3.11 The schematic and layout design of the DO of M_1. (*a*) the schematic of the DO of M_1, (*b*) the layout of the DO of M_1, (*c*) the detail of the DO of M_1

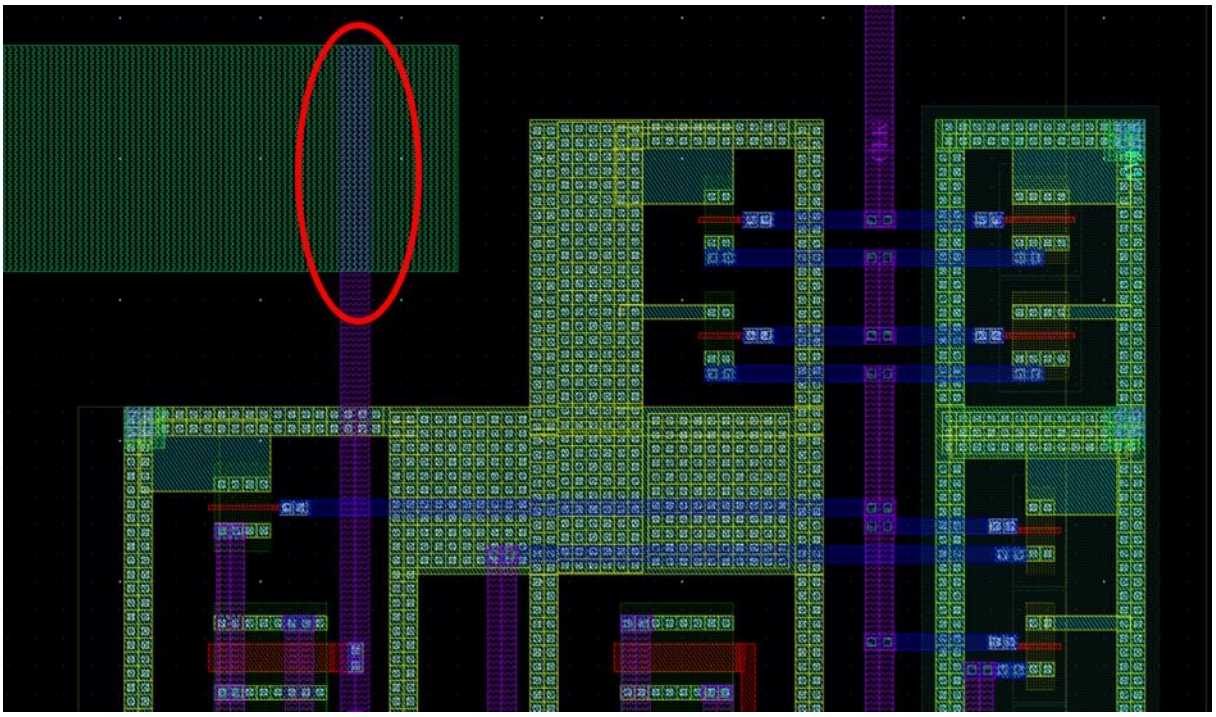
Figure 3.12 shows the schematic and layout of the injection fault type of GO of M_2. The open gate of the M_2 transistor is designed to remove the connecting holes between the third and fourth layers of metal. The detail was shown in Figure 3.12(*c*).



(*a*)



(*b*)

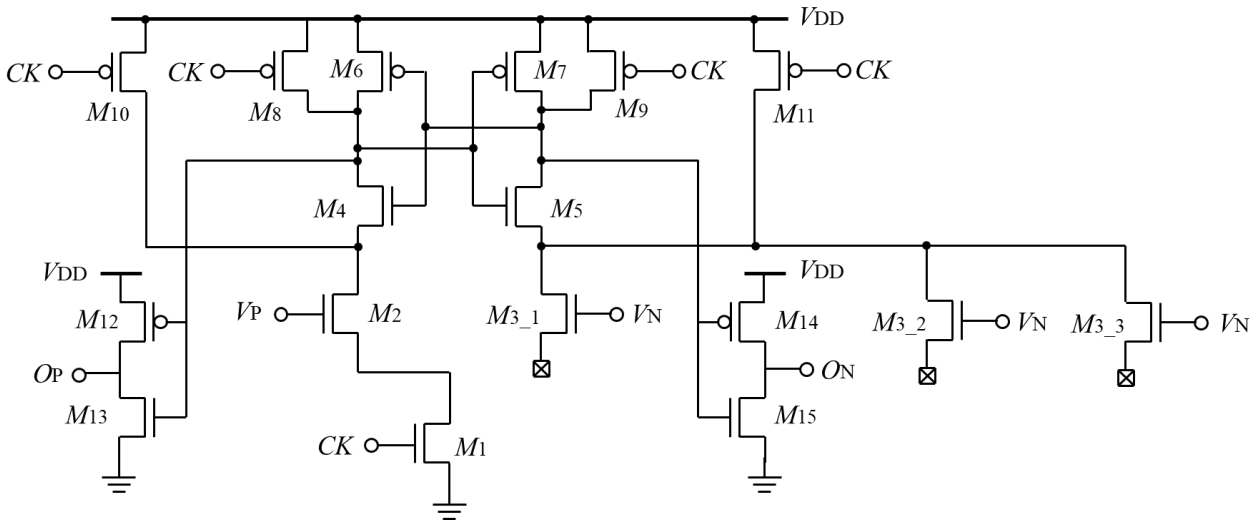


(*c*)

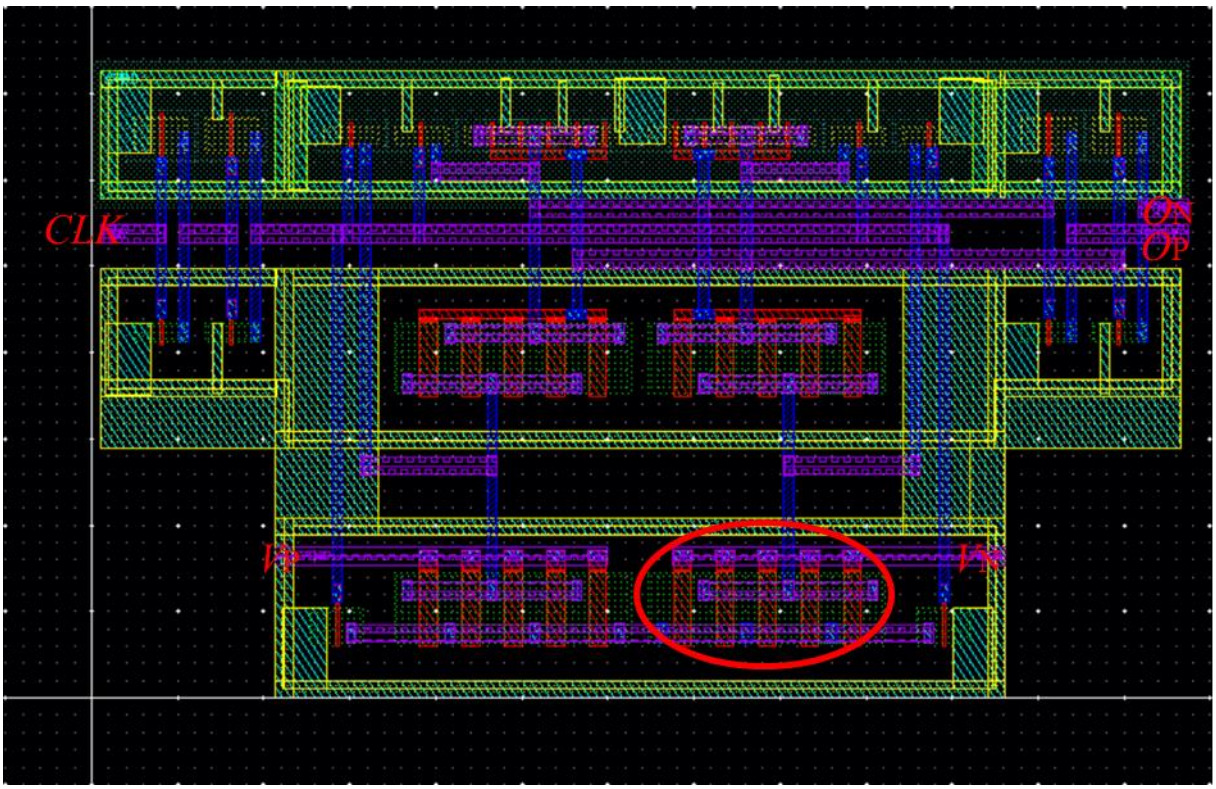
Figure 3.12 The schematic and layout design of the GO of M_2. (*a*) the schematic of the GO of M_2, (*b*) the layout of the GO of M_2 (*c*) the detail of the GO of M_2

Figure 3.13 shows the schematic and layout of the injection fault type of SO of M_3. Because M_3 was divided into five parallel MOS transistors in the actual layout design, the corresponding schematic was changed to that shown in Figure 3.13(*a*) and Figure 3.13(*b*).

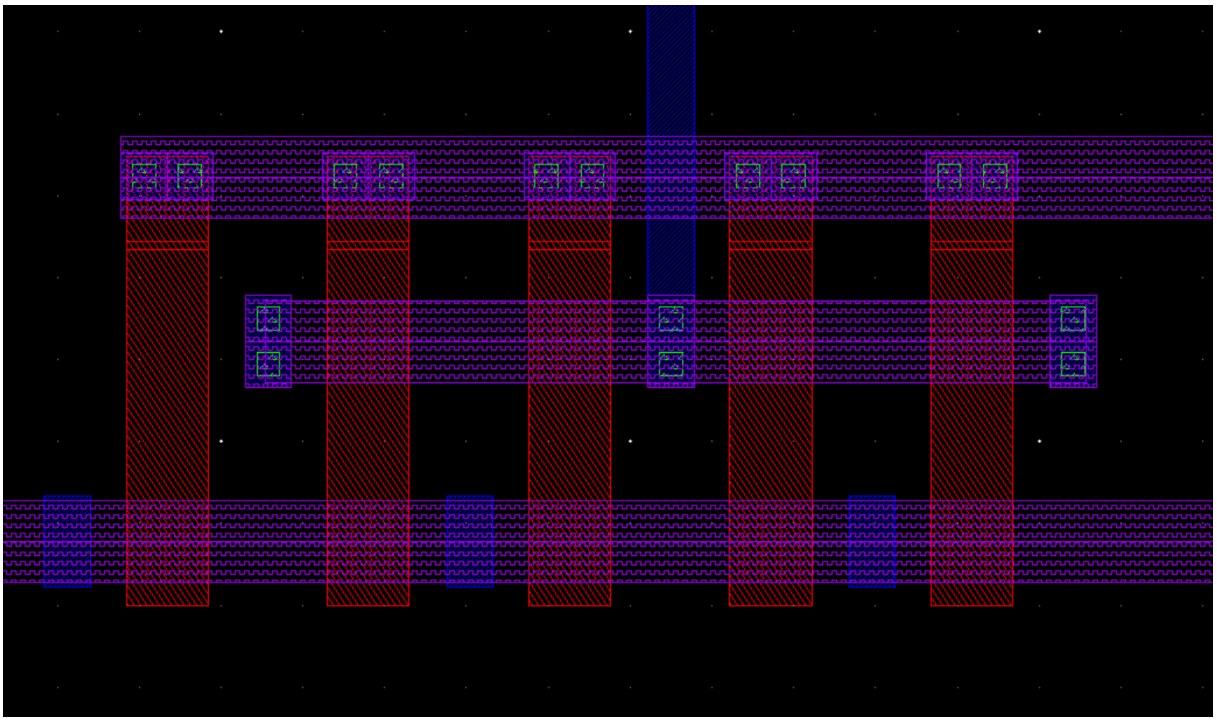
The open source of the M_3 transistor is designed to remove the connecting holes between the second and third layers of metal. The detail was shown in Figure 3.13(*c*).



(*a*)



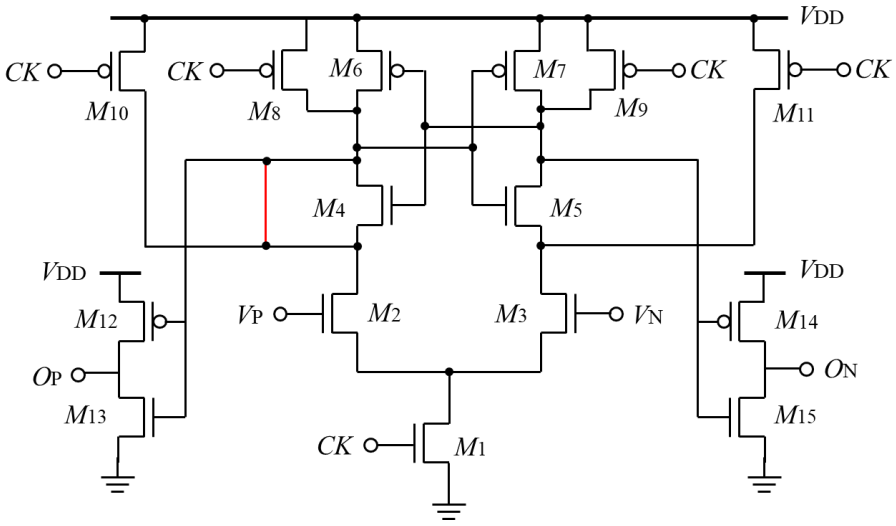
(*b*)



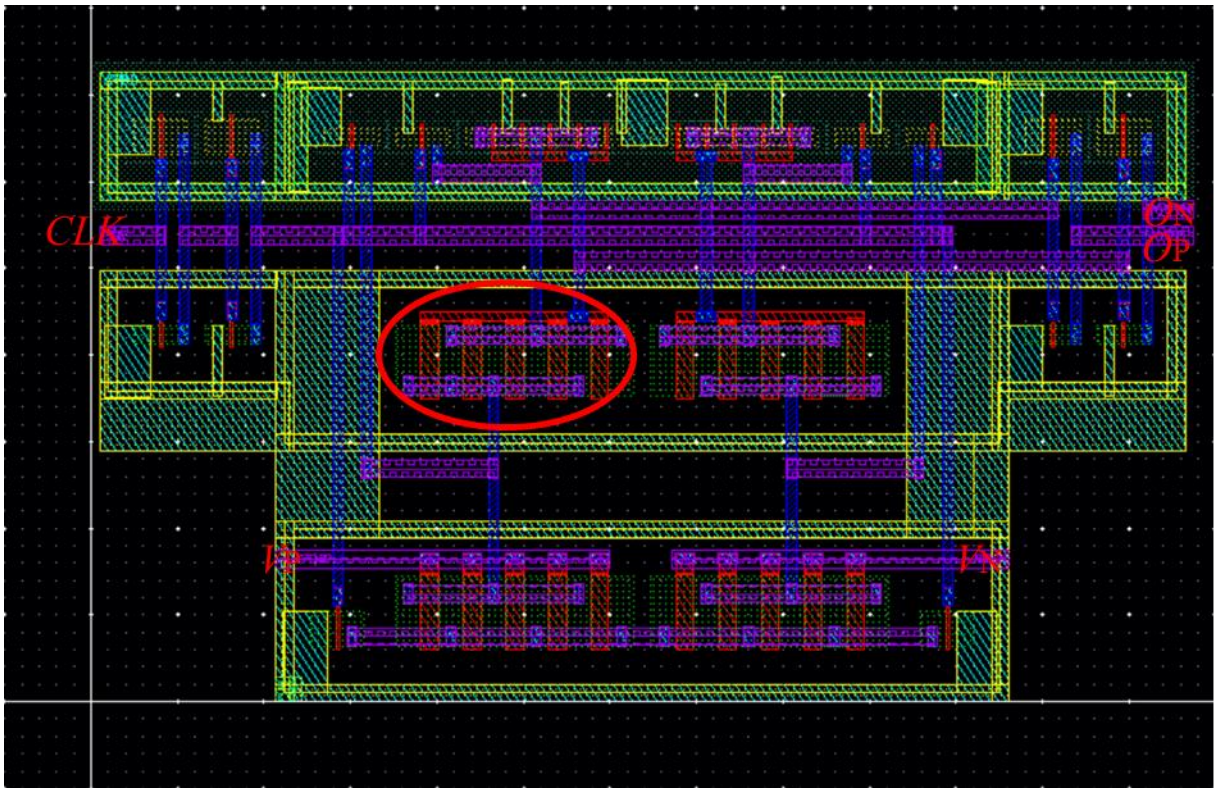
(*c*)

Figure 3.13 The schematic and layout design of the SO of M_3. (*a*) the schematic of the SO of M_3, (*b*) the layout of the SO of M_3, (*c*) the detail of the SO of M_3

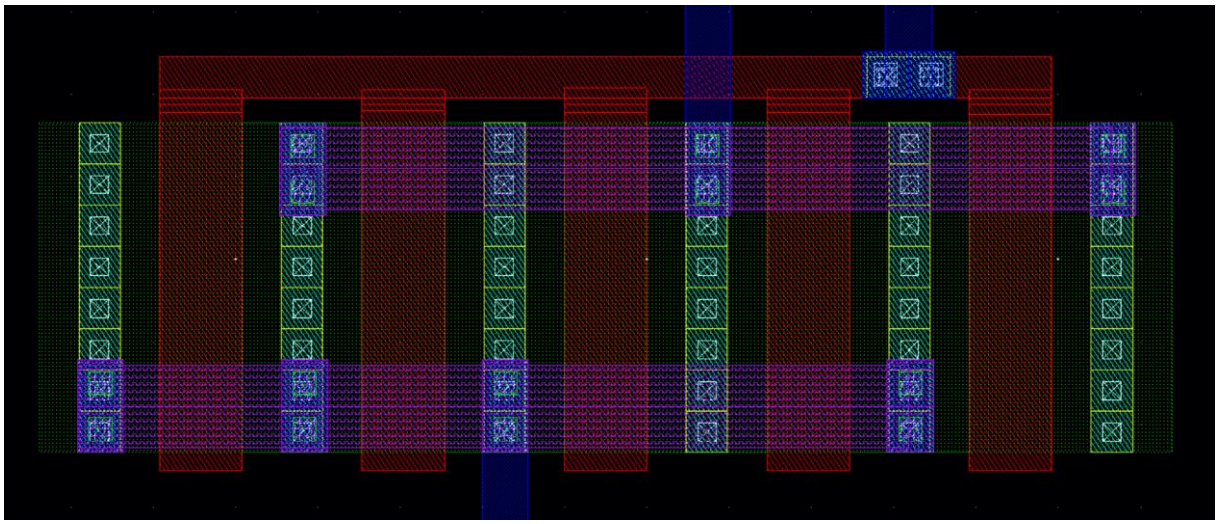
Figure 3.14 shows the schematic and layout of the injection fault type of DSS of M_4. The short between the drain of the M_4 transistor and the source of the M_4 transistor is designed to add a connection of the layer form the first metal to the third metal. The detail was shown in Figure 3.14(*c*).



(*a*)



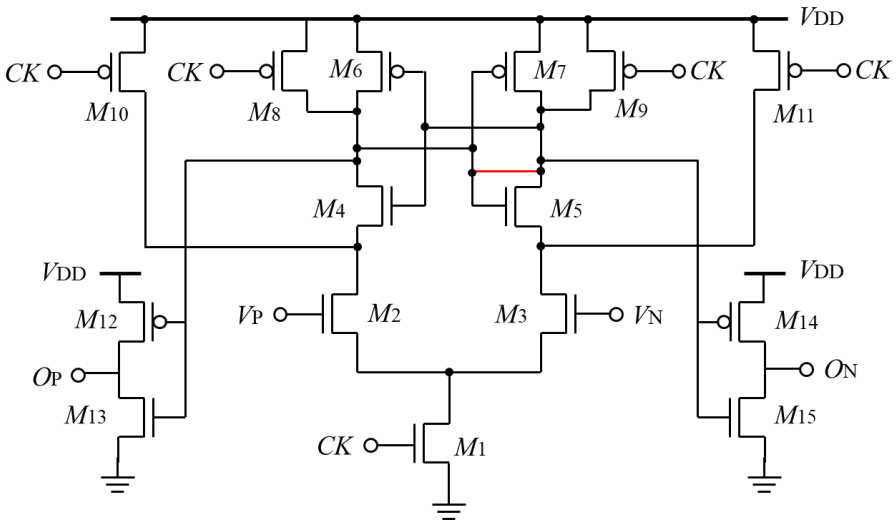
(*b*)



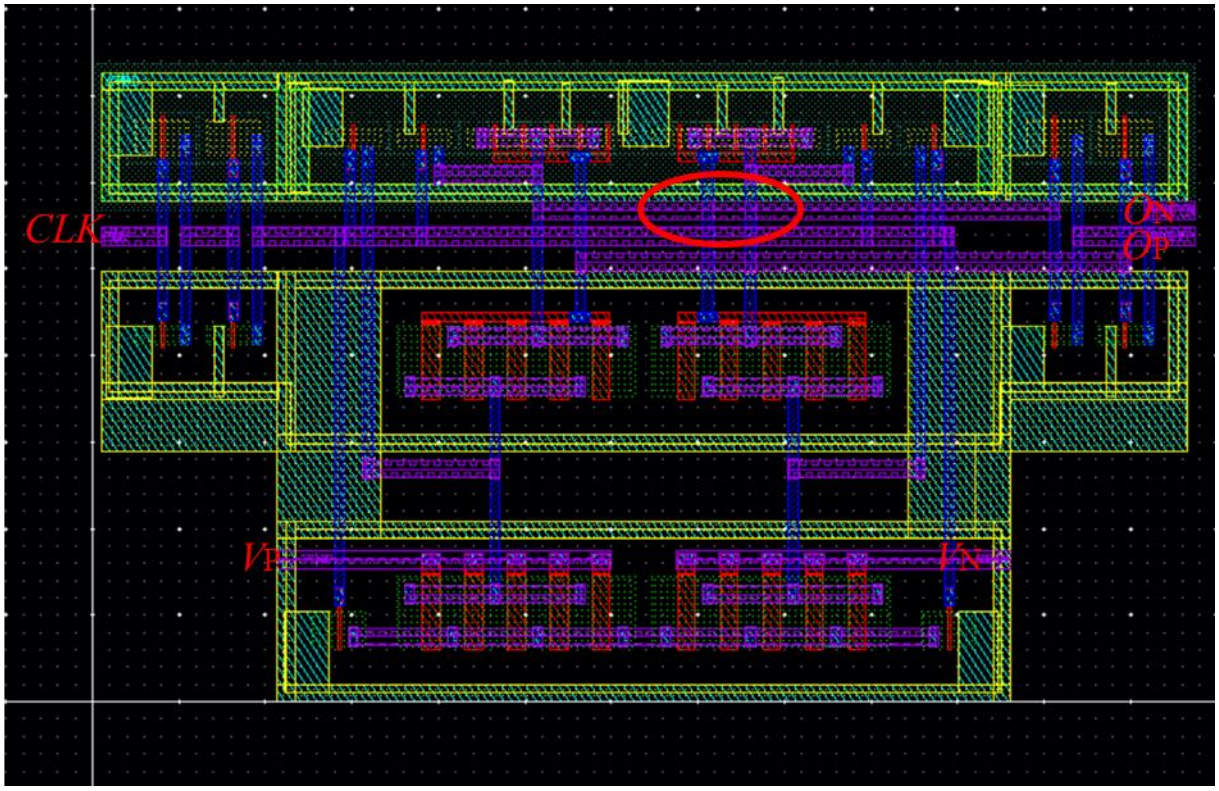
(*c*)

Figure 3.14 The schematic and layout design of the DSS of M_4. (*a*) the schematic of the DSS of M_4, (*b*) the layout of the DSS of M_4, (*c*) the detail of the DSS of M_4

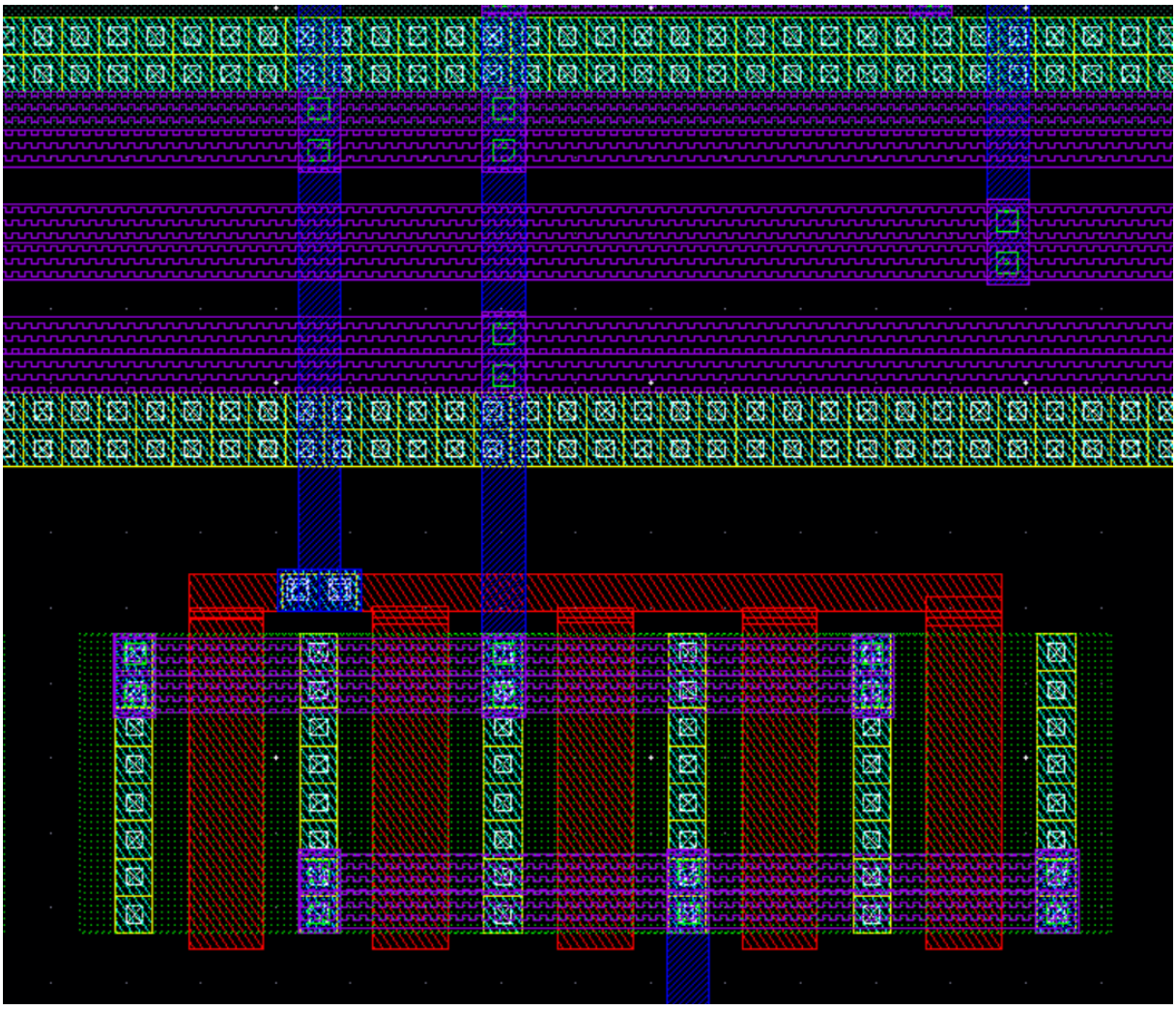
Figure 3.15 shows the schematic and layout of the injection fault type of GDS of M_5. The short between the gate of the M_5 transistor and the drain of the M_5 transistor is designed to add a connection of the layer form the second metal to the third metal. The detail was shown in Figure 3.15(*c*).


VDD
CK
CK
M6
M7
CK
CK
M10
M8
M9
M11
M4
M5
VDD
VDD
M12
VP
M2
M3
VN
M14
OP
ON
M13
M15
CK
M1

(*a*)


CLK
ON
OP
VP
VN

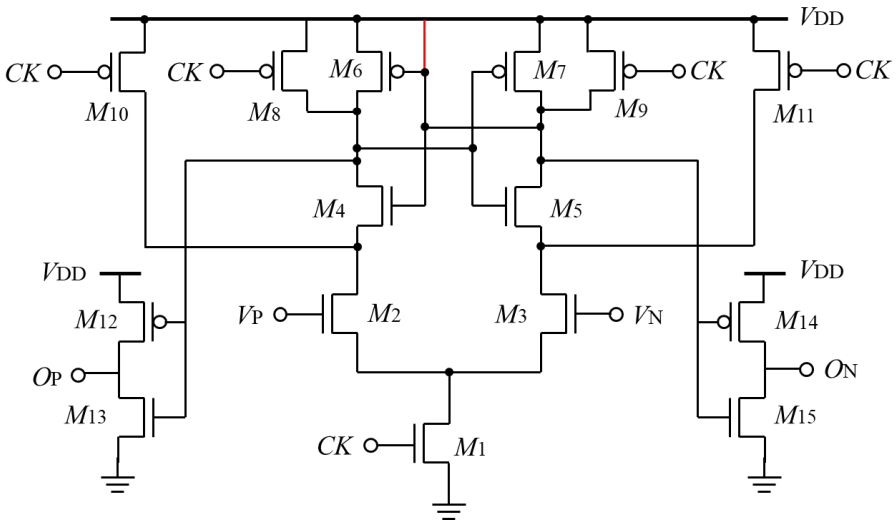
(*b*)



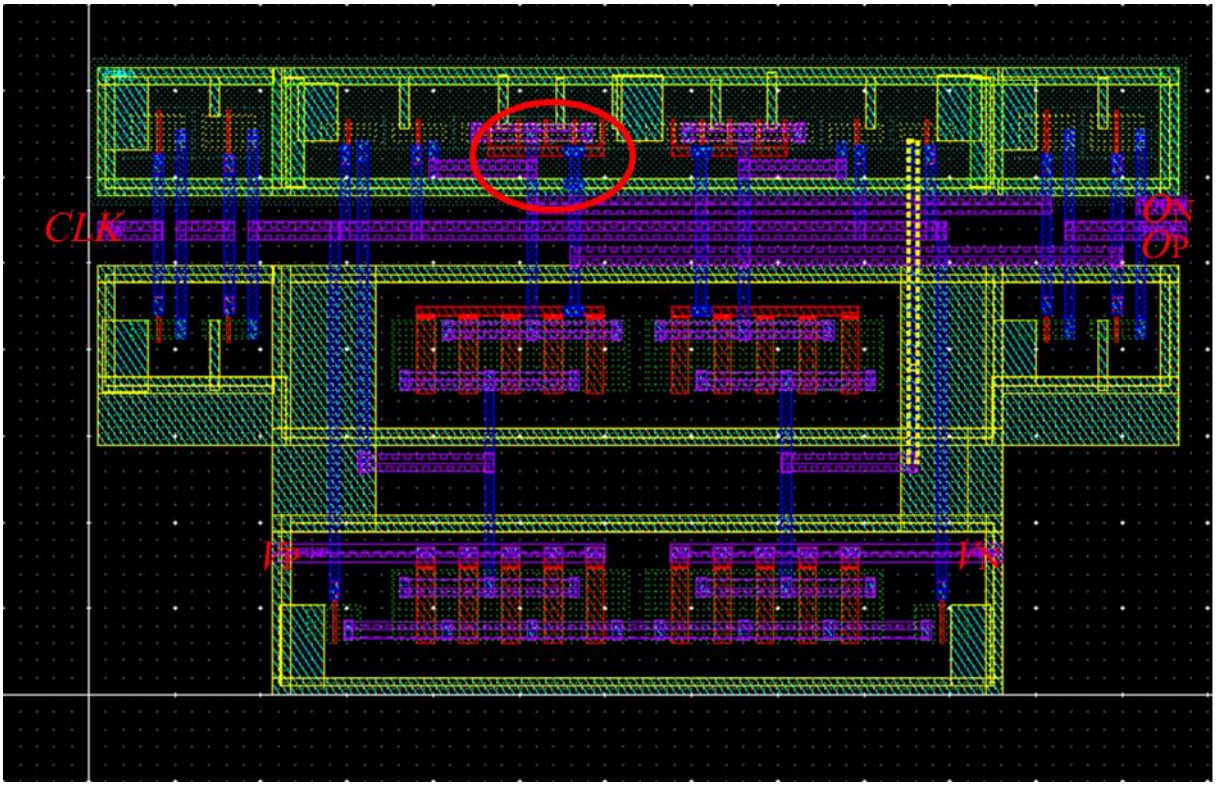
(*c*)

Figure 3.15 The schematic and layout design of the GDS of M_5. (*a*) the schematic of the GDS of M_5, (*b*) the layout of the GDS of M_5, (*c*) the detail of the GDS of M_5

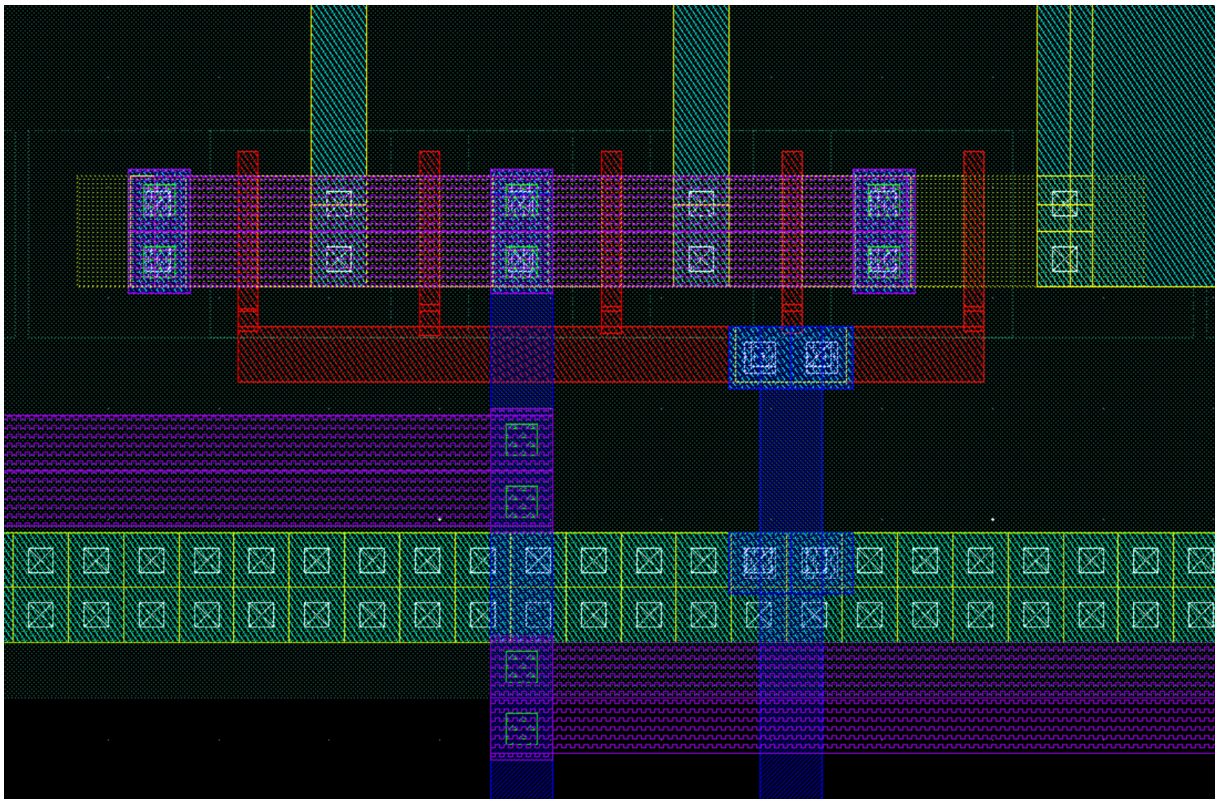
Figure 3.16 shows the schematic and layout of the injection fault type of GSS of M_6. The short between the gate of the M_6 transistor and the source of the M_6 transistor is designed to add a connection of the layer form the first metal to the second metal. The detail was shown in Figure 3.16(*c*).


VDD
CK
CK
M6
M7
CK
CK
M10
M8
M9
M11
M4
M5
VDD
VDD
M12
VP
M2
M3
VN
M14
OP
ON
M13
M15
CK
M1

(*a*)


CLK
ON
OP
VP
VN

(*b*)

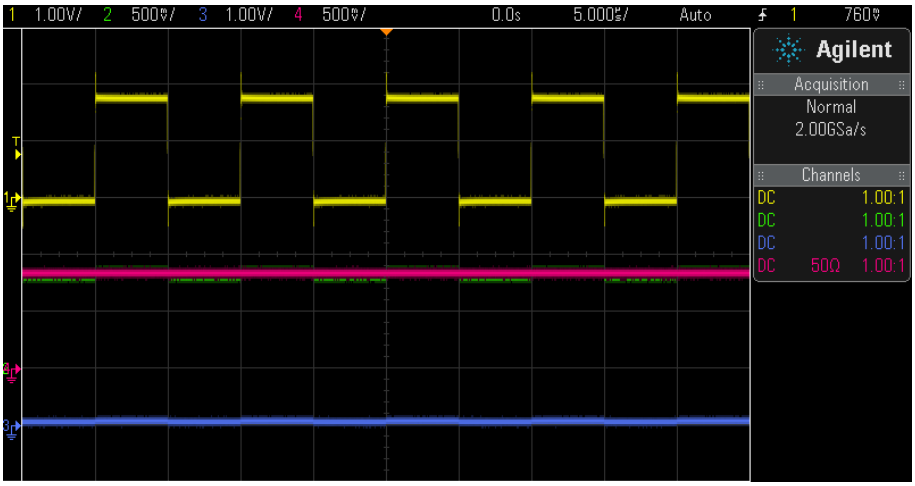


(*c*)

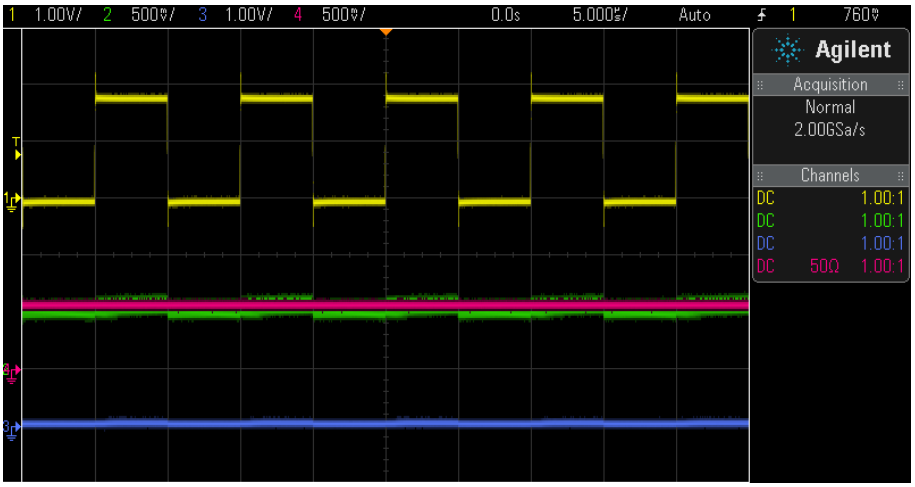
Figure 3.16 The schematic and layout design of the GSS of M_6. (*a*) the schematic of the GSS of M_6, (*b*) the layout of the GSS of M_6, (*c*) the detail of the GSS of M_6

3.5.2 Test results

Figure 3.17 shows the test result of the fault-free circuit. Channel 1 is the *CLK* signal, channel 2 is the V_N signal, channel 3 is the *F* signal, and channel 4 is the V_P signal. As shown in Figure 10a, the voltage of the V_P signal is 900 mV, and the voltage of the V_N signal fluctuates around 900 mV. Similarly, as shown in Figure 10b, the voltage of the V_P signal is 600 mV, and the voltage of the V_N signal fluctuates around 600 mV. As analyzed, the V_N signal can follow the V_P signal.



(*a*)



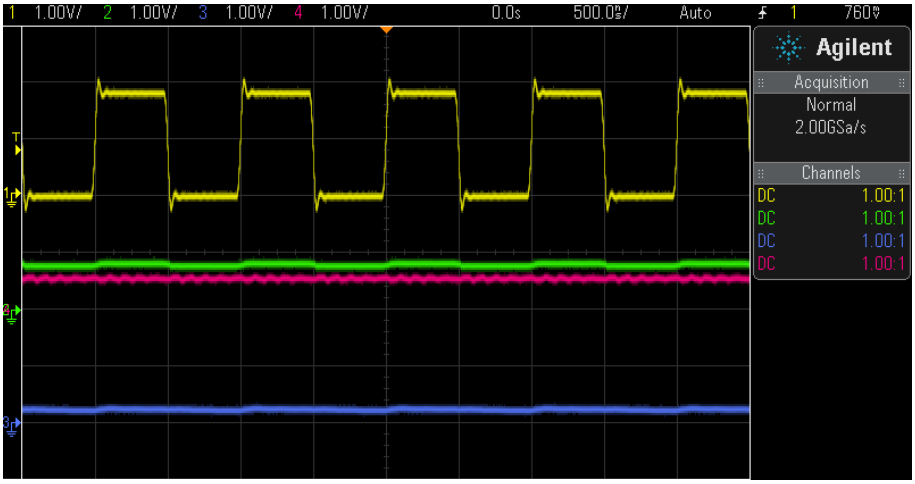
(*b*)

Figure 3.17 The test results of the fault-free circuit. (a) with VP = 900 mV, and (b) with VP = 600 mV.

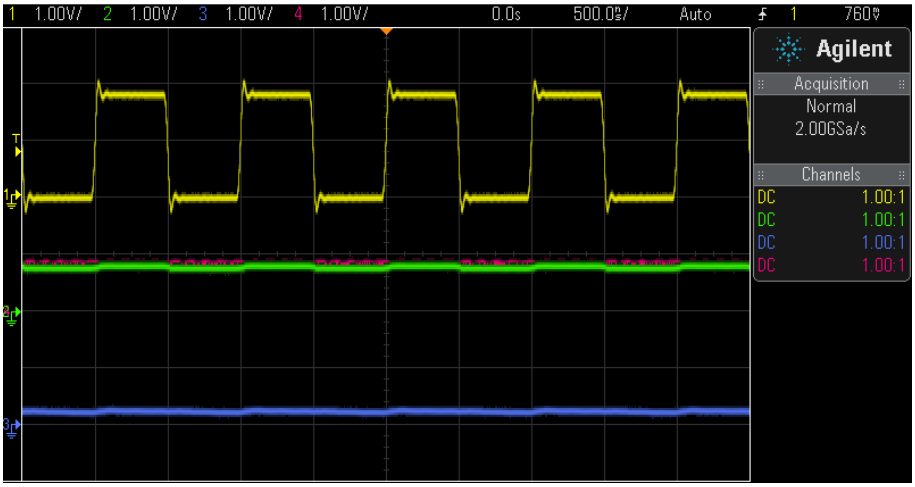
The window boundary of the comparator was designed to be from 850 mV to 950 mV. Unfortunately, the window comparator did not identify correctly. Fortunately, the feasibility of the scheme can still be seen. The fault-free circuit and the faulty circuits with a DSS of M_4 both show the results.

Figure 3.18 shows the test result of the faulty circuit with a DO of M_1. As shown in Figure 11a, the voltage of the V_P signal is 900 mV, and the voltage of the V_N signal fluctuates around 900 mV. The difference is, as shown in Figure 11b, that the voltage of the V_P signal is 600 mV, and the voltage of the V_N signal fluctuates around 900 mV. The voltage of V_N is maintained at 900 mV. As analyzed, the V_N signal cannot follow the V_P signal. However, the voltage of V_N is maintained at 900 mV. The five faulty circuits with a DO of M_1, GO of M_2,

SO of M_3, GDS of M_5, and GSS of M_6 all show the results.



(*a*)



(*b*)

Figure 3.18 The test results of a faulty circuit with a DO of M1. (a) with VP = 900 mV, and (b) with VP = 600 mV.

Although the test proved the feasibility of the solution, it was unusual for the V_N to maintain a voltage of 900 mV in the faulty circuit. The authors believe that this is probably the highest voltage a circuit can measure. Because there is no input buffer added at the input side, this may result in a maximum voltage of 1.8 V inside the circuit, but only 900 mV is measured

3.6 Discussions and Conclusion

Although the test proved the feasibility of the solution, it was unusual for the V_N to

maintain a voltage of 900 mV in the faulty circuit. The authors believe that this is probably the highest voltage a circuit can measure. Because there is no input buffer added at the input side, this may result in a maximum voltage of 1.8 V inside the circuit, but only 900 mV is measured.

To confirm this conjecture, the voltage of the V_N port was not detected, and the test was carried out. Figure 3.19 shows the test results of the fault-free circuit without the V_N port. Channel 1 is the *CLK* signal, channel 3 is the *F* signal, and channel 4 is the V_P signal. The *F* signal will periodically exhibit logic "1". This indicates that the voltage of the V_N signal reaches the window boundary.

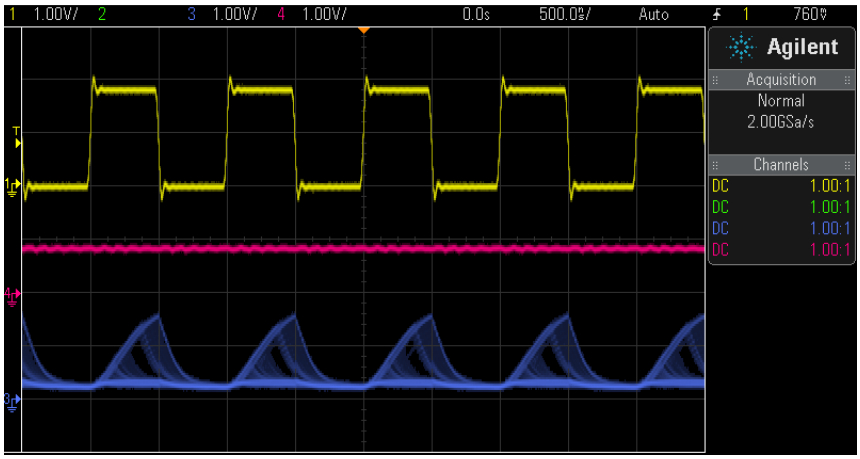


Figure 3.19 The test results of a fault-free circuit without the V_N port.

Furthermore, the test results indicate that the fluctuation range of V_N needs to be determined by further testing, and the window boundary of the comparator needs to be redesigned.

A dynamic comparator is a typically mixed-signal circuit widely used in high-speed and low-power consumption design. However, there are few works on fault diagnosis schemes for dynamic comparators. This work proposed a dynamic comparator scheme for detecting catastrophic faults. In this scheme, a feedback loop was designed using the characteristics of the comparator and monitoring the voltage in the feedback loop to determine the presence of a circuit fault. The proposed BIST scheme was designed and simulated in ROHM 180 nm CMOS technology. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the proposed BIST scheme, one fault-free state and six faults were implemented in the real circuit. The test results show that the scheme is effective. However, the design still falls short. The boundaries of the comparator window require more data to determine.

Reference

[1] Lu, J.M.; Wu, C.W. Cost and benefit models for logic and memory BIST. In Proceedings of the Conference on Design, Automation and Test in Europe, Paris, France, 27–30 March 2000.

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4 A Compact Window Comparator for Extreme Voltage

This chapter proposes a new compact window comparator, which can be used to detect extreme voltage. Extreme voltage means that the voltage is close to the ground or close to the supply voltage. In this window comparator, a source follower is used to translate the extreme voltage to the voltage suitable for detection. The proposed window comparator is realized with transistor level. The simulation results verify the proposed compact window comparator in 180nm CMOS technology.

4.1 Introduction

The window comparator compares the input voltage to the window boundary. The Window boundary is determined by lower limit voltage (V_L) and upper limit voltage (V_H). If the input signal (V_{IN}) is between the lower limit voltage (V_L)and upper limit voltage (V_H), the output signal is logic "1". If the input signal (V_{IN}) is lower the lower limit voltage (V_L) or higher the upper limit voltage (V_H), the output signal is logic "0"

The compact window comparators employ logic circuits are proposed in [1-3]. However, due to the limitation of the threshold voltage, the extreme voltage which close to ground or close to the supply voltage cannot be detected. Subsection is a feasible scheme for detecting extreme voltage [4]. However, this method outputs logic "1" for the entire extreme voltage range. In actual testing or monitoring, a smaller window boundary may be needed. For example, when using the bootstrapped switch circuit, a high voltage which closed to the supply voltage will be achieved. Voltage detection for key node may only require a window

size of tens of millivolts.

This paper presents a compact window comparator for extreme voltage. Section 4.2 previews the conventional window comparator, and the proposed circuit is a modified version of this window comparator. Section 4.3 presents the proposed window comparator. Section 4.4 and 4.5 sets the simulation results and test results. Section 4.6 sets the conclusion.

4.2 Conventional window comparator

The structure of the conventional window comparator [3] is shown in Figure 4.1. This structure employs four inverters to distinguish the input voltage and an XOR gate to determine the output logic.

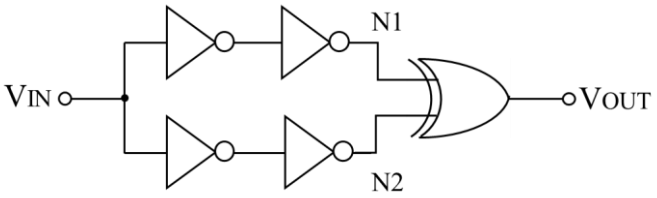

Figure 4.1 The conventional window comparator

The simulation results are seen in Figure 4.2. When $V_L < V_{IN} < V_H$, the Node 1 (N_1) is logic "1", and the Node 2 (N_2) is logic "0". Therefore, the XOR gate output logic "1". When $V_{IN} < V_L$ or $V_H < V_{IN}$, the N_1 and N_2 are both logic "0" or logic "1". Therefore, the XOR gate output logic "0"

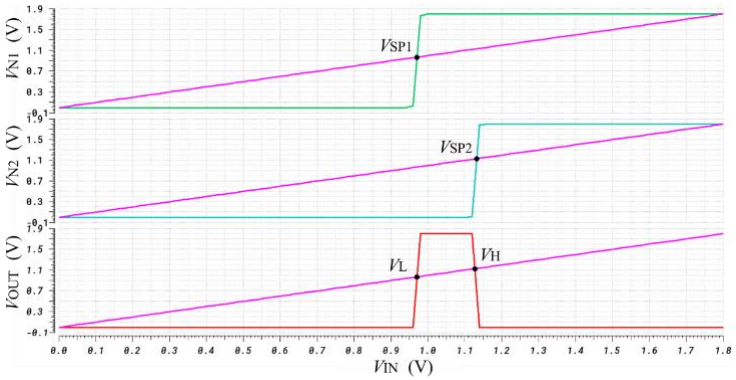

Figure 4.2 The simulation results with the conventional window comparator.

The window boundary voltage V_L and V_H of the window comparator can be designed by adjusting the switching point voltage V_{SP1} and V_{SP2}. Furthermore, the switching point voltage V_{SP1} and V_{SP2} can be adjusted by adjusting the W/L of the four inverters. However, no matter how you adjust the W/L, V_L will not be close to the ground, and V_H will not be close to the supply voltage.

In fact, if $V_{IN} < V_{THN}$ (V_{THN} means the threshold voltage of NMOS) or $|V_{DD} - V_{IN}| < V_{THP}$ (V_{THP} means the threshold voltage of PMOS), the N_1 and N_2 are both logic "0" or logic "1". Therefore, the XOR gate output logic "0". Therefore, the extreme voltage cannot be set to the window boundary. This means the extreme voltages cannot be detected.

4.3 Proposed window comparator

Figure 4.3 shows the proposed compact window comparator. The proposed circuit is a modified version of the circuit of Figure 4.1. The proposed circuit consists of a source follower, four inverters and a XOR gate. A source follower has been added to translate the extreme voltage to the voltage suitable for detection.

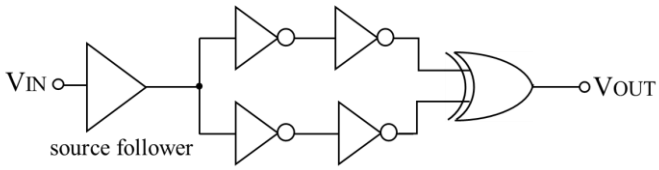

Figure 4.3 The proposed compact window comparator

Figure 4.4 shows the transistor-level schematic of the proposed circuit for an input voltage close to the supply voltage. The source follower is formed by the transistor M_1 and the resistance R_1, four inverters are formed by the transistors $M_{2\text{-}9}$, and the XOR gate is formed by the transistors $M_{10\text{-}21}$.

When input voltage is close to the supply voltage, M_1 turns on in saturation and I_{D1} flows through R_1, the voltage of Node 3 (N_3) will follow the V_{IN} with a difference. Therefore, the voltage close to the supply voltage can be translated to the appropriate voltage, which causes the conventional window comparator to output logic "1". When other voltages are input, the window comparator outputs logic "0"

Similarly, a PMOS source follower can be used to translate when the input voltage is close to the ground, as shown in Figure 4.5.

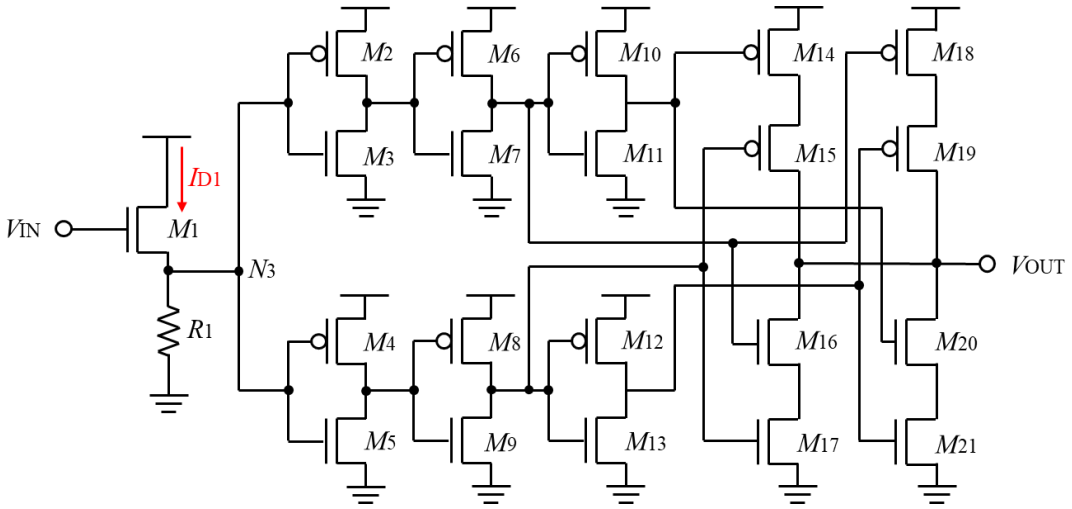

Figure 4.4 The proposed compact window comparator

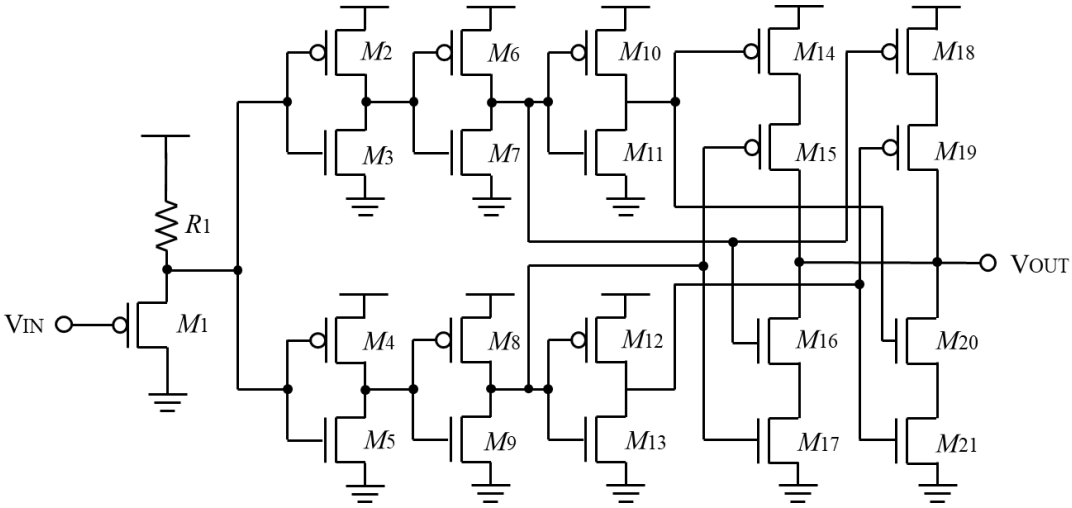

Figure 4.5 The proposed compact window comparator

4.4 Simulation results

The proposed comparator window comparator has been designed in 180nm CMOS technology and simulated by HSPICE. Figure 4.6 shows the simulation results regarding the DC response of the proposed window comparator in Figure 4.4. It is seen that when the input voltage is between 1.74 – 1.8V, the output of the window comparator is logic “1”. This confirming the predicted behavior.

The Monte-Carlo simulation are be used to simulation the process variation and mismatch. Figure 4.7 shows the 200 times Monte-Carlo simulation of the proposed comparator in Figure 4.4. The simulation results verify the proposed compact window comparator can be used to detect extreme voltage.

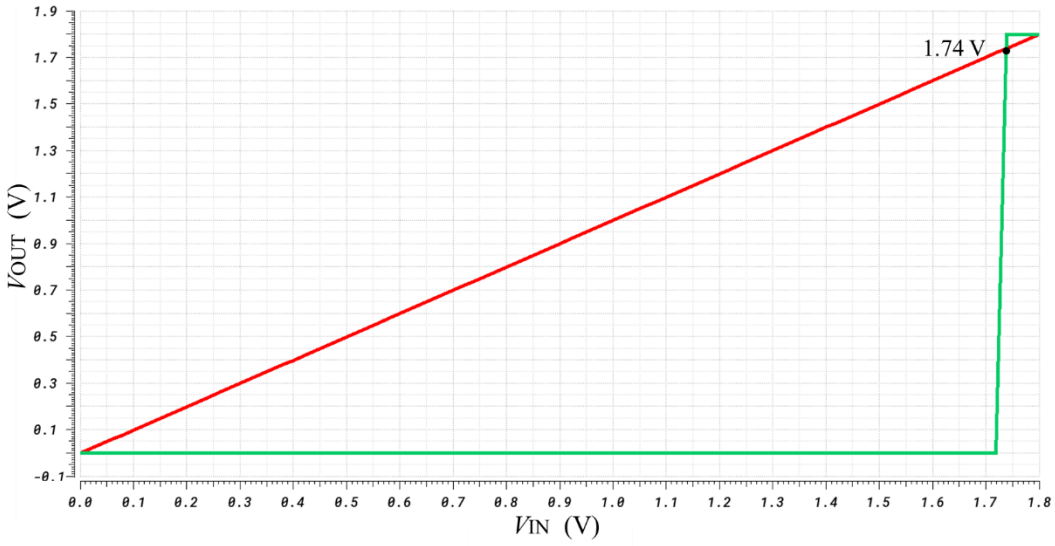

Figure 4.6 The proposed compact window comparator

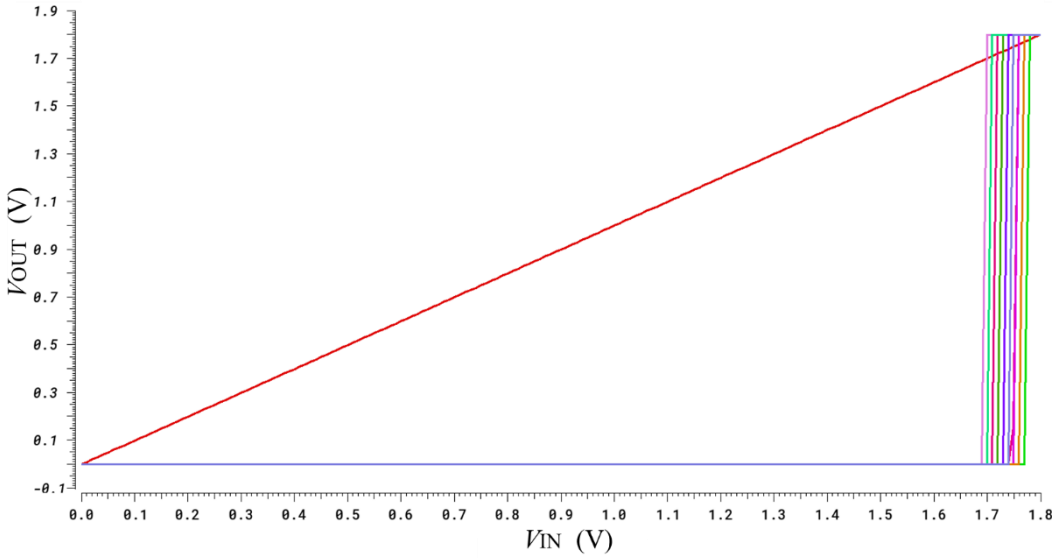

Figure 4.7 The proposed compact window comparator

4.5 Test Result

The proposed compact window comparator has been implemented in ROHM 180nm

CMOS technology. The designed PMOS transistors $M_{2,4,6,8}$ and $M_{10,12,14,15,18,19}$ have 8μ/200n and 4μ/200n, as the W/L, respectively in Figure 4.4. The designed NMOS transistors M_1, $M_{3,7}$, $M_{5,9}$, and $M_{11,13,16,17,20,2}$1 have 4μ/200n, 2μ/2μ, 2μ/400n and 2μ/200n, as the W/L, respectively in Figure 4.4. The designed resistance is 10K Ω.

Figure 4.8 shows the hysteresis measurement of the proposed window comparator for an input voltage close to the supply voltage. The transition voltage were 1.907 V and 1.887 V, resulting in 0.02 V of hysteresis.

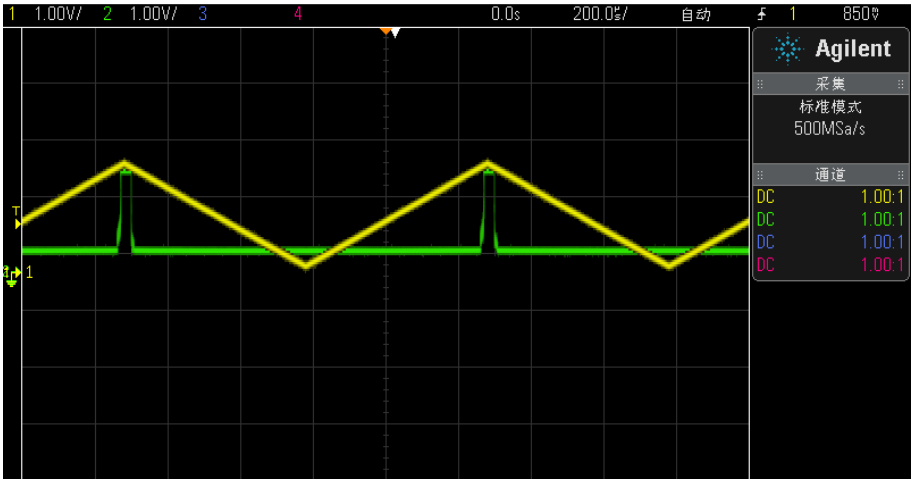

Figure 4.8 The Hysteresis measurement of the proposed window comparator for an input voltage close to the supply voltage.

Figure 4.9 shows the DC response of the proposed window comparator for an input voltage close to the supply voltage. The test results show, that when the input voltage was below 1.9 V, the output voltage was near 0.39 V, which can be recognized as a logic “0”; when the input voltage was 1.9 V to 1.95 V, the output voltage increased rapidly; when the input voltage was 1.96 V to 2 V, the output voltage reaches the maximum value near 1.8 V, which can be recognized as a logic “1”; when the input voltage was greater than 2 V, the output voltage was near 0.39 V, which may due to the protection limitations of ESD circuits.

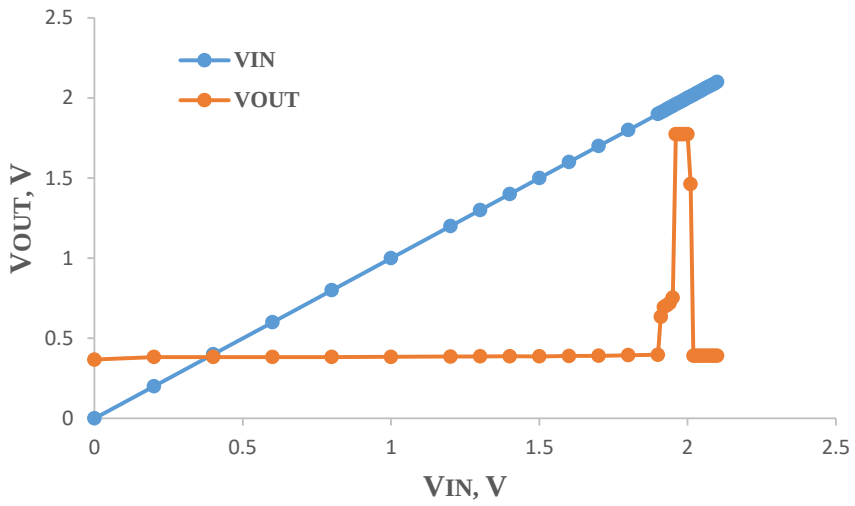

Figure 4.9 The test result of the proposed window comparator for an input voltage close to the ground.

4.6 Conclusion

The conventional window comparator cannot detect extreme voltage. Therefore, this paper proposed a compact window comparator for extreme voltage. The proposed window comparator translates the extreme voltage to the voltage suitable for detection by using a source follower. The test results verify the effectiveness of the proposed window comparator. A feasible embodiment is provided in this paper. The actual window comparator can be designed according to the requirements.

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5 Conclusions

In this dissertation, the built-in self-test schemes are proposed for analog mixed-signal circuits with simple structure but few correlation test circuits for catastrophic faults.

The main research work and innovation of this dissertation are as follows.

(1) This dissertation proposes a BIST scheme for bootstrapped switches. The clock signal and the gate voltage of the sampling MOS transistor are taken as the observation signals in the proposed BIST scheme. Usually, the gate voltage of the sampling MOS transistor is greater than or equal to the supply voltage when the switch is turn on, and such a voltage is not suitable for observation. To solve this problem, a low power supply voltage is provided for the bootstrapped switch to obtain a suitable observation voltage. The proposed BIST scheme and the circuit under test (CUT) are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.9% with 66 test circuits.

(2) This dissertation proposes a BIST scheme for dynamic comparator. In this scheme, a feedback loop is designed using the characteristics of the comparator. By monitoring the voltage in the feedback loop to determine the presence of circuit fault. The pro-posed BIST scheme and the circuit under test are realized with transistor level. The proposed BIST scheme was simulated by HSPICE. The simulated fault coverage is approximately 87.8% with 90 test circuits. To further verify the effectiveness of the propose BIST scheme, six faults were injected into the real circuit. The test results are consistent with the simulation results.

(3) This dissertation proposes a compact window comparator for extreme voltage. Extreme voltage means that the voltage is close to the ground or close to the supply

voltage. In this window comparator, a source follower is used to translate the extreme voltage to the voltage suitable for detection. The proposed window comparator is realized with transistor level. The simulation results verify the proposed compact window comparator in 180nm CMOS technology.

The BIST scheme designed in this dissertation still has the following deficiencies.

(1) The BIST scheme of the bootstrapped bootstrap switch does not tape out. The simulation results are limited and cannot represent the real circuit results.

(2) The BIST scheme of the dynamic comparator has some problems in actual measurement. In layout design, the input and output impedance matching are ignored, resulting in output signal problems.

(3) In the actual circuit injection fault type, a variety of options can be considered for research.

Acknowledgements

The author would like to express his deepest gratitude to his supervisor Prof. Masayoshi TACHIBANA for his support and encouragement. I still remember the first time we talked, Prof. TACHIBANA told me that reading papers is an effective way to see how others do, but there is another way of doing research, which is to find what you want to do and just do it, because when you do it, there will be problems, and just solve those problems.

The author would like to thank Mr. aoki for his help. He provides daily help in the lab. Thank you very much.

List of Publications

[1] X.B. Tang, and M. Tachibana. "A BIST Scheme for Bootstrapped Switches." Electronics 10.14 (2021): 1661.

[2] X.B. Tang, and M. Tachibana. "A BIST Scheme for Dynamic Comparators." Electronics 11.24 (2022): 4169.