ABSTRACT

Thin-film transistors (TFTs) serve as fundamental switching elements in advanced display technologies, including AM-LCD, AMOLED, ultra-high-resolution AR/VR systems, and emerging oxide-based integrated electronics. Conventional platforms, such as hydrogenated amorphous silicon (a-Si:H) and low-temperature polycrystalline silicon (LTPS), face inherent limitations in terms of mobility, scalability, and manufacturing complexity. Although amorphous oxide semiconductors (AOS), such as a-IGZO, enable low-temperature processing and improved uniformity, their amorphous nature fundamentally restricts carrier transport, limiting further enhancement of field-effect mobility (μ_{FE} ~10 $cm^2/V \cdot s$) for next-generation high-frame-rate and high-density applications.

Polycrystalline indium oxide (poly-InO_x) has emerged as a promising alternative channel material owing to its crystalline bixbyite structure, which provides continuous edge-sharing InO_6 octahedra and strong In 5s orbital overlap, enabling intrinsically high mobility. However, the practical implementation of poly-InO_x TFTs faces several critical challenges: (i) excessively high native carrier concentration (~10^{19}–10^{20} cm^{-3}) originating from intrinsic defects, which complicates threshold-voltage (V_{th}) control and enhancement-mode operation; (ii) severe short-channel effects (SCEs), including channel shortening and drain-induced barrier lowering (DIBL), as device dimensions scale below a few micrometers; (iii) high and nonuniform contact resistance; and (iv) instability induced by hydrogen diffusion from conventional dielectric layers during thermal processing.

This dissertation systematically addresses these challenges through integrated material characterization, dielectric engineering, and channel structure optimization. First, the role of hydrogen in poly-InO_x, hydrogen-doped poly-InO_x (poly-InO_x:H) films was investigated using thermal desorption spectroscopy (TDS) and hard X-ray photoelectron spectroscopy (HAXPES) to clarify the hydrogen bonding states, desorption behavior, and their influence on crystallization, grain growth, and carrier transport. These studies established optimized annealing conditions that balance defect passivation and carrier concentration control.

Second, hydrogen-free SiO_2 gate insulators (GI) and interlayer dielectrics (ILD) were developed using $SiCl_4$-based ICP-CVD to eliminate hydrogen incorporation from the dielectric layers. The hydrogen-free dielectric stack significantly suppresses charge trapping, stabilizes the threshold voltage, and enhances the bias-temperature reliability compared with conventional hydrogen-containing SiO_2 processes.

Third, boron (B) implantation was introduced as a precise source/drain (S/D) formation technique to control the carrier concentration and reduce the contact resistance in self-aligned top-gate poly-InO_x TFTs. The impact of implantation-induced lattice defects and subsequent thermal recovery on channel shortening was quantitatively analyzed by extracting ΔV_{th}, channel-shortening length (ΔL), and drain-induced barrier lowering (DIBL). Optimized implantation and annealing conditions effectively mitigated short-channel degradation while maintaining high mobility and stable operation.

Overall, this study establishes a comprehensive materials-to-device framework that integrates hydrogen management, hydrogen-free dielectric processes, and implantation-based channel engineering. The proposed strategies enable high-mobility, thermally stable, and aggressively scalable poly-InO_x TFTs, providing a viable pathway for next-generation display backplanes and oxide electronic applications.

Chapter 1 presents the background and motivation for advancing oxide semiconductor TFTs, particularly in the context of next-generation high-resolution and high-frame-rate display technologies that require high-performance TFTs. This highlights the limitations of amorphous oxide semiconductors, such as a-IGZO, whose structural disorder restricts their mobility and scalability. In contrast, poly-InO_x materials have been introduced as promising channel candidates because of their inherently higher mobilities. This chapter also outlines the key challenges addressed in this study, including TFT structural design, device scaling, SCEs, contact resistance, electrical uniformity, and device reliability.

In Chapter 2, the fundamental material properties of poly-InO_x:H thin films were investigated. Using TDS and HAXPES, we evaluated the H incorporation, bonding configurations, and desorption mechanisms. The analysis clarifies how H influences the phase transition from amorphous to polycrystalline, modifies the crystallization temperature, and promotes the grain growth. These insights provide the basis for selecting

optimized annealing conditions and understanding the impact of H on the electrical properties, including Hall mobility and TFT operation.

In Chapter 3, a fully H-free SiO_2 dielectric formation method is introduced and demonstrated to prevent unintended hydrogen diffusion into the poly-InO_x active layer during the fabrication process. The H-free SiO_2 formed by the optimized processing exhibited superior interface quality, reduced charge trapping, and significantly improved device reliability. This chapter further compares conventional TEOS and SiH_4 based SiO_2 deposition methods for GI and ILD, evaluating their influence on electrical stability using TDS and secondary-ion mass spectrometry (SIMS) analyses. The extracted parameters confirmed that the H-free dielectrics enhanced the device uniformity, suppressed degradation, and supported reliable TFT performance.

Chapter 4 examines the effectiveness of B-implantation in mitigating channel-shortening and improving the performance of short-channel TFT. It also quantifies the influence of thermal budget at different temperatures and durations on the lateral reduction of the active channel region. This chapter explains how B-induced defects modify the lattice structure and generate the carrier concentration. The subsequent lattice recovery during annealing governed the degree of channel-shortening in the films. Electrical analyses, including channel shortening length (ΔL), width-normalized source-drain contact resistance ($R_{SD}W$), and DIBL, demonstrated that the optimized B-implantation enhanced gate controllability and enabled aggressive channel-length scaling.

Chapter 5: Conclusions

The results of the research are summarized, and the steps for further research are listed in this chapter.