# DEVELOPMENTS OF BUILT-IN SELF TEST AND CALIBRATION OF ANALOG MIXED-SIGNAL LSI FOR CATASTROPHIC FAILURES AND PARAMENTRIC VARIATIONS

**Wimol San-Um**

**A dissertation submitted to**
**Kochi University of Technology**
**in partial fulfillment of the requirements**
**for the degree of**

**Doctor of Philosophy**

**Graduate School of Engineering**
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# Abstract

The modern system-on-chip technology has led to a continuous increase in quantity and diversity of integrated circuits. Testing and calibrating for catastrophic and parametric faults in both product development and mass-production phases have subsequently become more challenging, and now constitute a major portion of overall cost. Although the testing process has been commercialized by means of off-chip automatic testing equipment, this process is expensive and time-consuming. Recent research efforts for on-chip testing in analog mixed-signal circuits have therefore been of much attractive, focusing on Built-In Self Test (BIST) techniques in which test stimuli and response analysis are accomplished entirely on-chip through built-in hardware. Neither external test stimulus generator nor external digital signal-processing unit is required, resulting in low cost and low testing time.

This dissertation aims to design new BIST techniques and to develop corresponding BIST circuits and systems for catastrophic fault detection and parametric fault calibration in analog mixed-signal LSI. Such BIST techniques are expected to be versatile and capable of yielding high fault coverage, whilst BIST circuits and systems are expected to possess low area overhead, low power consumption, and low performance degradation. The design strategy is the development of specific BIST approaches for each particular analog mixed-signal Circuit-Under-Test (CUT) blocks. The scope of CUT in this dissertation has emphasized on common circuits encountered in LSI systems, ranging from simple analog building blocks, which comprise only CMOS transistors, to complicated mixed-signal circuits composed by various analog and digital building blocks. Contributions of this dissertation involve five new BIST techniques classified in two approaches. The first approach involves three BIST-only techniques for catastrophic and parametric fault detection in three targeted circuits. Reasons for investigating only BIST without calibration is due to the need for BIST for analog circuit with performance degradation awareness and also the reasonable cost for extra chip area, especially in small circuit size. Three targeted CUT involve a compact CMOS-only analog circuit such as amplifiers and low-order filters, a RC-based Linear-Time-Invariant (LTI) analog circuit such as higher-order filters, and an embedded analog circuit in mixed-signal LSI through IEEE1149.4 standard analog-digital boundary scans. The second approach involves two BIST with calibration approaches, which detect catastrophic faults as well as accommodate parametric faults, in frequency-based analog mixed-signal circuits. Both test and calibration circuits are

investigated due to the possibility of frequency calibration. Since these circuit types are relatively complicated, comprising vast number of transistors, calibration foster a cost reduction in the case where parametric faults exist. Two targeted CUTs involve a self-oscillating circuit such as linear oscillators, and a Charge Pump Phase-Locked Loop (CP-PLL) that comprises complex analog and digital mixed-signal circuits.

In this dissertation, the first proposed BIST technique is a two-step AC and DC testing scheme for detecting catastrophic faults in the pre-screening of defective small analog building blocks. This technique simplifies the design of fault-sensing circuits, and provides a single test outputs in digital form, which is applicable in LSI test systems. Demonstrations of the BIST system for a two-stage CMOS differential amplifier show the fault coverage percentage and area overhead of 95.45% and 15%, respectively. The second proposed BIST technique is a pulse input stimulus and a single voltage sample obtained on pulse responses. This BIST technique employs a new pulse generator, which simultaneously provides two short pulses for stimulating a CUT and controlling the sampling process. A single effective voltage on a transient pulse response is initially sampled using a sampled-and-hold circuit and lately employed for fault detection using window comparators. Demonstrations of BIST system for Sallen-Key low-pass filter with a cut-off frequency of 500kHz, containing the total number of 67 faults, show high percentage of fault coverage at 95.5%. Experimental results show an area overhead of approximately 12% with low performance degradation on existing CUT performances.

The third proposed BIST technique is a fault signature characterization and the extension of IEEE 1149.4 standard. The testing technique is a sinusoidal fault signature characterization by means of two level crossing voltages. The test system is an extension of the IEEE 1149.4 standard through the modification of an analog boundary module, affording functionalities for both on-chip testing capability and accessibility to internal components for off-chip testing purposes. Demonstrations of the BIST system for a $4^{th}$-order $G_m$-$C$ low-pass filter show that both catastrophic and parametric faults are potentially detectable at the minimum parameter variation of 0.5%. The fault coverage associated with CMOS transconductance operational amplifiers and capacitors is approximately 94% and 100%, respectively. The fourth proposed BIST and calibration technique is a regulated supply tuning current-starved voltage-controlled ring oscillator with built-in self test and calibration. A low-dropout regulator with an integrated low-pass filter operates as a frequency-tuning element with inherent noise suppression. Frequency calibration employs a bias current tuning in three frequency ranges for adjusting an oscillation frequency shift caused by parametric faults. The Built-In Voltage and Current Sensor (BIVCS) facilitates on-chip accessibility and

testability for catastrophic faults. Simulation results reveal low jitter performance of less than 14.32ps at the oscillation frequency of 200MHz. High and low frequency ranges can be calibrated with the offset frequencies of 22MHz and 20MHz, respectively, through two-bit control signals. Tests for shorts and opens show total fault coverage of 83.68%. The fifth proposed BIST and calibration technique is a supply-regulated charge pump phase-locked loop. This technique employs two independent regulators that provide low-sensitivity supply voltages with inherent noise suppression for analog blocks, and afford multiple reference voltages for test and calibration process. The BIST and calibration system based on the deviation of a control voltage during locking state facilitates on-chip accessibility and observability. Demonstrations through simulations and experiments of a 200-MHz CP-PLL demonstrate low-jitter and low supply sensitivity performances with test and calibration functionality.

All proposed BIST techniques have demonstrated a compact test system implementation using a few number of compact components while maintaining high average fault coverage of greater than 80%, which is sufficient for cost-effective fault pre-screening process on-chip. Unlike other BIST approaches in which the CUT has to be modified in order to facilitate test features, these proposed BIST techniques do not modify the existing CUT configurations since particular types of input stimulus and output response characterization were employed for specific types of CUT, resulting in low performance degradation. Moreover, all proposed BIST circuits are designed as switchable circuitries, i.e. normal operation and test modes are selectable, in order to avoid loading effects and reduce extra power consumption in normal operation mode. These five techniques proposed in this dissertation have a potential of being further improved to meet the future demands in both academia and industries.

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# Chapter 1

## Introduction

The emergence of modern system-on-chip technology has led to a continuous increase in quantity and diversity of integrated circuits. As the complexity has grown, testing and calibrating for catastrophic and parametric faults in both product development and mass-production phases have become more challenging, and now constitute a major portion of overall cost. Although the off-chip testing process has been commercialized by means of Automatic Testing Equipment (ATE), this process is expensive and time-consuming. Recent research efforts for on-chip testing in analog mixed-signal circuits have therefore been of much interest, particularly focusing on Built-In Self Test (BIST) techniques in which test stimuli and response analysis are accomplished entirely on-chip through built-in hardware. Neither external test stimulus generator nor external digital signal-processing unit is required, resulting in low cost and low testing time. This chapter presents the background and viewpoint of BIST techniques that motivate the studies in this dissertation. The chapter initially introduces defects in integrated circuits that cause circuit operation failures and output variations. Perspective reviews and comparisons of on-chip testing are subsequently summarized. Existing BIST techniques in three classifications are also reviewed. The objectives and strategy of this dissertation are included. Thesis organization is finally summarized.

### 1.1 Faults in Integrated Circuits

Failures in electronic components are generally the effects of chemical and physical processes. Failures caused by chemical effects lead to continuous production of defective components over whole production lines. Failures caused by physical effects, however, result in defects in individual components, involving component shorts and breaks, and packaging. Consequently, faults in integrated circuits are typically modeled based on physical failures, and generally classified into two categories, i.e. parametric and catastrophic faults. The catastrophic faults are caused by random defects, for example dust particles, resulting in short and open circuits or large-scale deviation of design parameters.

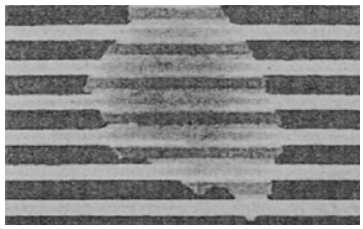
The parametric faults are representing the parameter variations of the nominal value, which exceeds the attributed tolerance band. Such parametric faults are caused by fluctuation in the manufacturing process. Comparing catastrophic and parametric faults, most electrical failures are catastrophic faults at a percentage of 83.5% (*Rajsuman*, 2000).

### 1.1.1 Catastrophic Faults

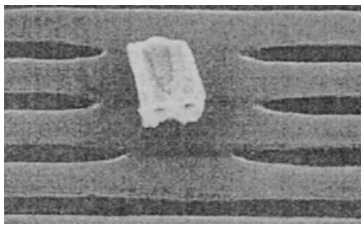
Catastrophic faults are commonly referred to as potential shorts and opens. In the case of shorts, two possible short circuits are bridging defects and Gate-Oxide Short (GOS). The bridging defects appear when two or more metal lines are electrically connected in an integrated circuit. Fig. 1.1 shows examples of bridging and GOS defects in CMOS technology presented by *Ohletz* (1996). As shown in Fig.1.1 (a), six examples of short circuits include the shorting of metal lines caused by unexposed photoresist, a solid-state particle on the metal mask, a scratch in the photoresist, metallization defects, and inter-layer shorts. Bridging resistance is important in defect detection since the majority of bridging defects show low resistance while many high resistance-bridging defects do not result in failure. Therefore, a resistance connecting the two bridges nodes can simply be modeled in simulation process. Fig. 1.1 (b) shows GOS defects in CMOS technology. These GOS defects are short circuits between the gate electrode and the active zone through the $SiO_2$ oxide of the device. In the majority of cases, gate-oxide defects cause reliability degradation such as changes in transistor threshold voltage and the increase in switching delay. Fig. 1.2 shows examples of open circuits presented by *Ohletz* (1996), involving a foreign particle causing a line open and a line thinning, and a contaminating particle causing 7-line opens. These open circuits are unconnected or floating inputs that usually high impedance or floating.

### 1.1.2 Parametric Faults

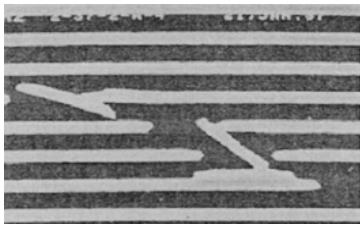
Parametric faults are generally referred to as the variation in components and interconnect dimensions. The physical component dimension is relatively susceptible to process variation, such as a Gate-length ($L$) and a threshold voltage ($V_T$) in CMOS transistors. The critical variations in interconnect dimensions of line-spacing and metal thickness result in different metal properties of the interconnect wires, such as their parasitic resistance, capacitance, and inductance values. As parametric faults typically depend on parameter tolerance band acceptability, modeling of parametric faults is relatively complicated at the physical design level. In order to overcome such impasses of parametric fault modeling, analysis method realizes an acceptable circuit instances based



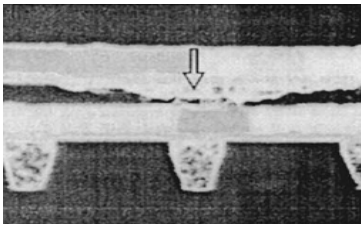
Metal short



Small solid particle

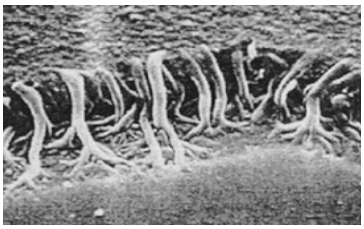


Line scratch

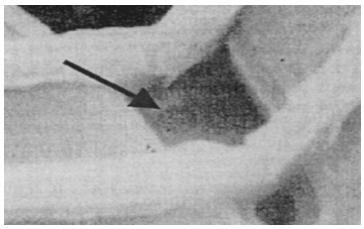


Inter layer short

(a) Examples of bridging defects in CMOS Technology



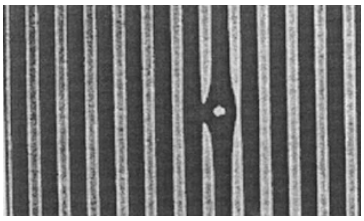
Metal Gate-Oxide short



Gate-Oxide short

(b) Examples of Gate-Oxide shorts in CMOS Technology

**Fig 1.1.** Examples of bridging defects and Gate-Oxide Shorts.



Foreign Particle

Contaminating Particles

**Fig 1.2.** Examples of opens caused by foreign and contaminating particles.

on tolerance specifications (*Chang and Lee*, 2002). In other words, the variation of parameters is initially injected randomly from ±5% to ±15% deviations from the nominal values, and the distribution of output variable values is subsequently analyzed for region of acceptability. The distribution of output variable is generally a normal distribution. In order to distinguish between acceptable and unacceptable instances, the region of acceptability is on the order of ±5% for the 99% confidential interval (*Spink and et al.*, 2004). Large variations in circuit parameters such as ±10% variations (*Seshadri and Abraham*, 2001)

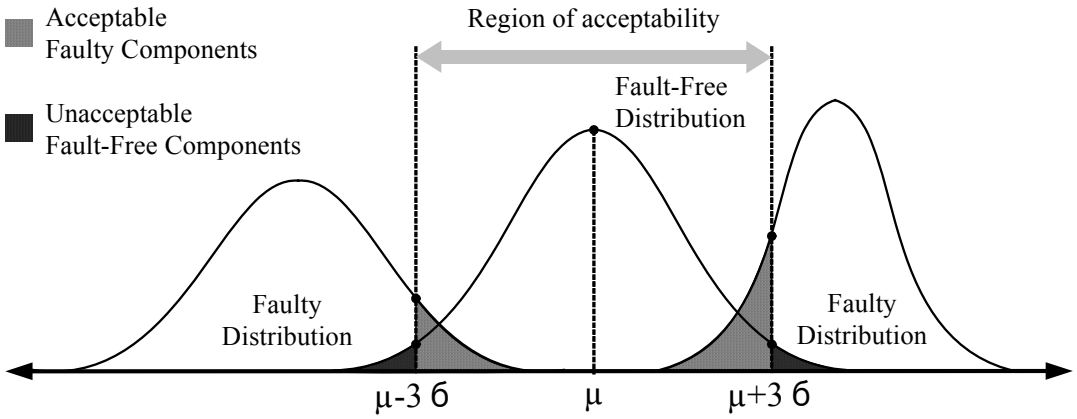



**Fig. 1.3.** Probability of faulty and fault-free distributions by parameter variations.

in resistor and capacitor values have been considered as unacceptable, and therefore the Circuit-Under-Test (CUT) is classified as defective component instantly. However, some large variations in circuit parameters may not result in specification violation while some small variation may not cause tremendous specification violation. Fig. 1.3 shows the probability of faulty and fault-free distributions. In order to ensure that all acceptable devices are distinguished with high yield coverage, the decision for acceptable components is based on specification violation, i.e. within the acceptability region of ±3σ, rather than the variation percentage of injected parametric faults (*Yoon et al.*, 1999).

## 1.2 Perspectives Reviews on On-Chip Testing Techniques

### 1.2.1 Reasons for On-Chip Testing Compared with Off-chip Testing

Two major reasons for on-chip testing of catastrophic and parametric faults are (1) the need of fully analog-digital test instruments and (2) high cost of off-chip testing through ATE. First, the advancement of deep sub-micron technology drives test equipments towards a single platform solution that can test both digital and analog structures on a single chip (*Stound*, 2006). Whereas test equipments for digital circuits are similar to purely digital chips, preferable analog mixed-signal test equipment is expected to be feasible. Consequently, test equipments are transversely changing from digital-only to the full integration of high performance instruments. Second, the ATE cost is the one of the most expensive cost in overall manufacturing process cost even though the combinations of equipment cost and reduction in equipment capability requirements have been suggested. Expensive analog test instruments and long testing time remain a difficulty. Moreover, test cost does not directly scale with transistor count, die size, device pin count and process technology.

### 1.2.2 Comparisons between Digital and Analog On-Chip Testing

Several early on-chip testing techniques have been applied successfully in digital circuits in which each level of abstractions is verified against the immediate preceding levels (*Stound*, 2006). Digital testing on-chip is supported by rigorous mathematical expression such as Boolean expressions, high-level programming language constructs, and single stuck-fault models. Therefore, test pattern algorithms and output response analysis in digital domains have been developed broadly with acceptable fault coverage. As opposed to testing in digital integrated circuits, testing in analog mixed-signal circuits is relatively complicated owing to not only instantaneous continuous-time analog response of signal values, but also non-linear characteristics and broad variations in circuit parameters (*Milor*, 1998). Test accuracy of analog mixed-signal systems also depends upon the test equipment resolution as well as the accuracy of input testing stimuli. Besides, both analog and digital circuits are recently developed on the same substrate and disturbances, i.e. noises from digital sections may produce influences on the function of the analog parts. These characteristics lead to difficulties in testing analog circuits, including vulnerability to performance degradation and indecipherable standard fault models (*Garcia et al*., 2001).

### 1.2.3 Comparisons between DFT and BIST Techniques

Two commonly known on-chip testing techniques are Design-for-Test (DFT) and Built-In Self Test. The DFT is a technique to reduce difficulty of testing by adding or modifying some hardware on chip. The scan DFT methodology (*Wei et al*, 1997), in which the sequential storage elements allow normal operation and test modes, has been a standard DFT practice followed by industry. In normal mode, the storage elements take their stimulus from a combinational logic and the response feeds into a combinational logic. In test mode, the storage elements are reconfigured as one or more shift registers, and each such configuration is known as a scan chain. The stimulus vector can be shifted serially into this scan chain. The chip is consequently allowed to function in normal mode and the responses for a test vector are captured in the storage elements. The response can be shifted out and compared with reference responses in order to test the chip for functional correctness. The use of DFT scan design has two major penalties, i.e. an area overhead due to the additional scan flip-flops and the performance overhead caused by on-path multiplexors in the scan flip-flops. Besides, this scan also has the disadvantage of greater power dissipation as there is generally more switching operation during scan mode than normal operation. Thus, a slow clock is commonly used for scan operation in order to reduce average power dissipation.

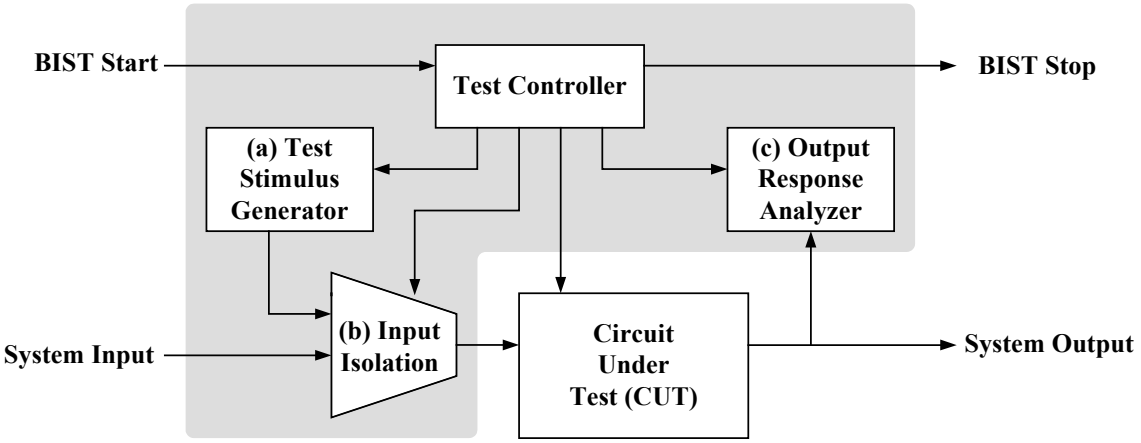



**Fig.1.4**. A generalized block diagram of BIST architecture.

The BIST refers to as techniques and circuit configurations that enable a chip to test internally and automatically (*Cluskey*, 1985; *Yamani and McCluskey* , 2003). In this BIST technique, test patterns are generated and test responses are analyzed completely on chip. Pattern generator logic reduces test data volume through shifting process of the easily detectable faults. The BIST technique offers various advantages over DFT testing techniques and ATE. First, test circuitry is incorporated on chip and no external tester is required. Second, test operations can be performed at normal clock rate. Third, the test operation can be performed after the chip has been incorporated in the system. However, two difficulties encountered in BIST techniques are area overhead and performance degradation. Incorporation of the self-testing capability requires addition of hardware on-chip, which may increase the silicon area and manufacturing costs.

Applying BIST techniques for analog mixed-signal circuits can be primarily considered in two approaches, i.e. functional and structural tests. Functional BIST evaluates circuit functionality and compares to a set of functional specifications. This functional BIST requires analog stimulus and measurement of analog outputs. Therefore, the quality of applied input and the precision of measured outputs are relatively important factors, highly depending on the test setup and equipment. On the other hand, structural BIST is based on physical information of the manufactured device. Therefore, the applied test patterns can be optimally chosen and fault coverage can be evaluated based on fault models.

## 1.3 Existing BIST Techniques for Analog Mixed-Signal LSI

Fig.1.4 shows the generalized block diagram of BIST architecture. This BIST architecture includes two essential functions, i.e. test stimulus generator and output response analysis, and two additional functions that are necessary to facilitate execution of

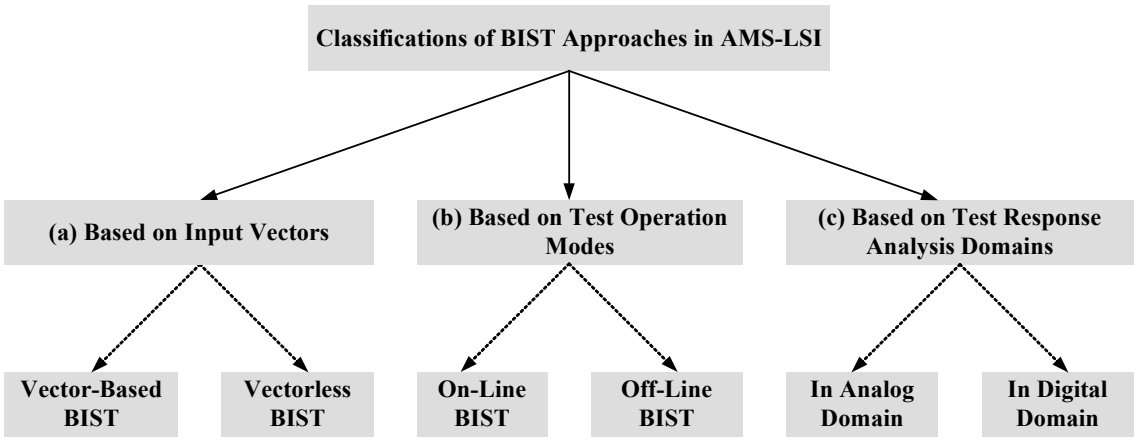



**Fig.1.5**. Classification diagram of BIST techniques.

self-testing feature, i.e. test controller and input isolation. Based on this generalized block diagram, several BIST techniques have recently been proposed to address the need for analog mixed-signal testing. Fig.1.5 therefore shows the classification diagram of BIST techniques. The BIST techniques can be classified into three main categories based on the use of input vectors, test operation modes, and test response analysis domain. Existing BIST techniques based on Figs.1.4 and 1.5 are reviewed in this section.

### 1.3.1 BIST Techniques Based on Input Vectors

As depicted in Fig. 1.5 (a), the BIST techniques based on input vectors are considered regarding the input stimulus generator in Fig.1.4 (a), and can be classified as vector-based and vectorless techniques. The vector-based BIST techniques are referred to as the testing techniques that require the output signals for fault information processing by means of applying test input stimuli such as DC input stimulus, sinusoidal input stimulus, and other non-sinusoidal signal. For DC input stimuli, the measurement of DC input signal through the use of a comparator (*Venuto*, 1995) yields low cost and low area overhead. A multiple DC measurement (*Sasho*, 1998) was also suggested in order to increase the fault coverage. Although these DC testing schemes are relatively simple and sufficient for some cases in the pre-screening process, the percentage of fault coverage is not high since some of hard-to-detect faults do not produce fault signatures through DC characteristics. The sinusoidal signals have also been used as an input vector (*Current and Chu*, 2001; *Marcia*, 2005), in which AC characteristics can be verified for the circuit functionality. The use of sinusoidal input vector offers a high fault coverage and multiple-frequency test can be achieved for a functional analysis in high-precision testing. However, the implementation

of high-precision sinusoidal signal generation on-chip is relative complex, requiring a large chip area. In addition, long test time for AC analysis is need in order to correctly characterize the circuit. Non-sinusoidal input stimuli such as pulse stimulus (*Singh at al*., 2004) and pseudo-random input stimulus (*Marzocca and Corsi*, 2002) have also been presented for some analog LTI circuits in LSI systems.

On the other hand, the vectorless BIST techniques are referred to as the testing that reconfigures CUT in order to generate output signals automatically with no input stimuli applied. Oscillation-Based Test (OBT) has proposed for testing different classes of analog and mixed-signal circuits (*Arabi and Kaminska*, 1996; *Zarnik*, 2000; *Harzon and Sun*, 2006). During test mode, the circuit is transformed into an oscillator and the frequency of oscillation is measured. Fault detection is based on the comparison of the measured oscillation frequency of the CUT with a reference value obtained from a fault-free circuit, operating under the same test conditions. This OBT test method is suitable for switching circuits such as the switched-capacitor technique that can easily be transformed through switching mechanisms. Another vectorless BIST techniques is the current testing approach which employs the current sensors to detect the magnitude of the DC quiescent current ($I_{DDQ}$) through a resistor, connecting between the CUT and the supply voltage (*Rajsuman*, 2000). The detected $I_{DDQ}$ will subsequently be compared with reference currents. Although this current testing approach has successfully been applied to digital circuits and can potentially enhance fault coverage, $I_{DDQ}$ testing suffers from power supply variation and ground shift.

### 1.3.2 BIST Techniques Based on Test Operation Modes

As depicted in Fig.1.5 (b), the BIST techniques based on test operation modes are considered regarding the input isolation circuitry in Fig.1.4 (b), and can be classified as off-line and on-line test methods. In off-line BIST test methods, the CUT suspends normal operations, and enters a test mode when the appropriate test method is applied. The off-line test operation can generally be executed either through ATE or through the use of BIST circuitry. This off-line test has been realized widely in most analog mixed-signal testing. For instance, all of those BIST techniques summarized in Section 1.3.1 obey off-line test methods. In on-line BIST test methods, the outputs from CUT are tested during normal operation. This on-line test operation can be achieved by coding scheme that has been embedded in the circuit design. For linear analog filters, continuous checksums have been proposed by (*Chatterjee*, 1993) through a cascade of analog integrators, which generate a non-zero signal in the case of an error in the transfer function of the circuit. An analog checker employs the on-line test method, which verifies an operational amplifier by means

of normal input and output signals (*Velasco*, 1998). An on-line BIST test method for analog biquad filter based on system identification (*Cota and et al.*, 1999) was studied by comparing the observed and expected outputs concurrently through adaptive filter in digital domain. Nonetheless, most BIST techniques are not suitable for on-line test since the circuit has its topology modified during the test or its input signal is being controlled by test mechanism. Therefore, the on-line test method requires the development of test strategies that continuously evaluate the operation of the circuit during normal operation. This problem of on-line monitoring becomes more important due to the use of sub-micron technologies, which are more sensitive to noise and radiation effects.

### 1.3.3 BIST Techniques Based on Domains of Fault Analysis

As depicted in Fig.1.5 (c), the BIST techniques based on domains of fault analysis are considered regarding the output response analyzer in Fig.1.4 (c), and can be classified as either in digital or analog domains. In digital domain, the output characterization process initially converts analog fault signatures into digital signals using a sigma-delta A/D converter (*Dufaza and His*, 1996) or a voltage comparator (*Czaja*, 2006). Such digital signals will subsequently be employed for fault detection by means of a digital comparator (*Roh and Abraham*, 2000) or a digital counter (*Cassol et al*., 2003), incorporating stored fault-free bit streams. Despite the fact that the characterization in digital domain offers expedience in comparison and storage of digital fault signatures, the implementation of A/D converters and digital counters is relatively complicated, resulting in hardware overhead and ultimately necessitating fault testing. On the other hand, the output characterization process in analog domain generally captures fault signatures by means of sampling process, and detects faults through voltage comparison in allowable tolerance margins (*Yu et al.*, 2004; *Stround*, 2006). Characterizing output response in analog domain has been realized extensively in most cost-effective BIST systems, as both catastrophic and parametric faults can be detected instantaneously with low area overhead.

## 1.4 Dissertation Developments

### 1.4.1 Motivations

With references to previously developed BIST techniques described in Sections 1.2 and 1.3, there are three major motivations that have led to the research and development of this dissertation. Firstly, there is a constant demand for new BIST techniques, especially for recent advanced analog mixed-signal LTI systems with low-cost,

low testing time, and low performance degradation. This demand for new BIST techniques has continuously been attractive for research activities since BIST is newly introduced to real chip manufacturing industry, and only a few number of BIST techniques have been implemented. Unlike scan DFT that has been integrated in digital circuits, not many BIST techniques have been integrated in the manufacturing industry yet.

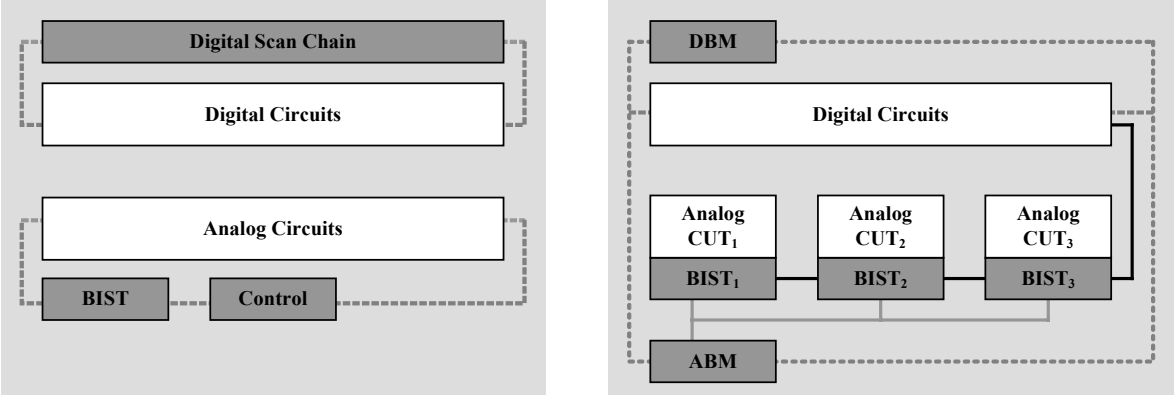
Secondly, there is the need for simple and compact BIST techniques for particular analog mixed-signal systems. Although a number of existing BIST techniques have demonstrated high fault coverage, the extra BIST circuitry is even more complicated than the exiting CUT itself, i.e. difficult operations and the requirement for extra external hardware. Those exiting complex BIST system may not suitable for on-chip integration and therefore simple BIST circuits and operations are still preferable, especially for the case of compact analog mixed-signal CUTs such as small amplifiers or filters. Lastly, there is a lack of studies in BIST circuits with calibration for some sensitive and complicated analog mixed-signal circuits such as oscillators and phase-locked loops. Since extra BIST circuits may introduce some penalties to the CUTs, applying BIST techniques to these circuit types remains a difficulty due to awareness of performance degradation. In addition to the three motivations, the improvement of previously proposed BIST techniques is also important in order to extend better BIST performances and functionalities.

### 1.4.2 Research Objectives

The objective of this dissertation is to develop new BIST techniques and implementations for catastrophic fault detection and parametric fault calibration. The BIST techniques are expected to be versatile for each specific type of analog and mixed-signal circuits, and capable of yielding high fault coverage. In addition, this dissertation also aims to design and implement corresponding BIST systems in CMOS technology, which yield low area overhead, low power consumption, and low performance degradation.

### 1.4.3 A Strategy for BIST Architecture

Generally, BIST strategy for analog mixed-signal can be considered in two architectures. Fig. 1.6 shows the block diagram of classical and recent BIST test strategies. As shown in Fig.1.6 (a), the classical test strategy exploits a common BIST for all analog sections, which can be considered as functional testing. The input signal stimuli are applied for all analog section and the expected single output is solely employed for fault signature analysis. The BIST circuit uses its own control system and those digital sections are scanned independently from analog sections. Although this classical strategy can simply be implemented, the fault coverage and testability is relatively low since different analog




**(a) Classical BIST Test Strategy** **(b) Recent BIST Test Strategy**

**Fig. 1.6.** Architectures of classical and recent BIST test strategies.

blocks exhibit different characteristics and functionalities. In addition, accessibility for fault localization cannot be achieved since test operation has to be done throughout analog sections. This dissertation therefore realizes a recent BIST test strategy as shown in Fig.1.6 (b) in which each analog mixed-signal functional block is tested independently through different test techniques. These independent tests yield not only higher fault coverage as each specific circuit is tested based on its functions, but also offer accessibility capability to each individual circuit. As new mixed-signal system has been advanced, test control operation can be achieved from the digital section. In addition, the compliance between analog and digital boundary scan modules has been researched intensely and therefore corporation test between digital and analog sections is possible.

### 1.4.4 Scopes of Research and Contributions

In order to discover new BIST techniques based on the motivations and objectives in the previous section, the scope of developed BIST techniques in this dissertation emphasizes on common CUT types encountered in LSI systems. Such CUTs are ranged from a simple analog building block, which comprises only CMOS transistors, to more complicated mixed-signal circuits composed by various analog and digital building blocks. For a better understanding in overall figure, Fig. 1.7 summarizes scopes and contributions of this dissertation through a flow diagram. This diagram describes two clusters of BIST circuit and system designs, ranging from low to high circuit complexity and conducting through five research phases. As shown in Fig.1.7 (a), the early three research phases in cluster 1 focus on BIST techniques for small and medium analog integrated circuits. Reasons for investigating only BIST without calibration are due to the need for BIST for analog circuit with performance degradation awareness and also the reasonable cost for

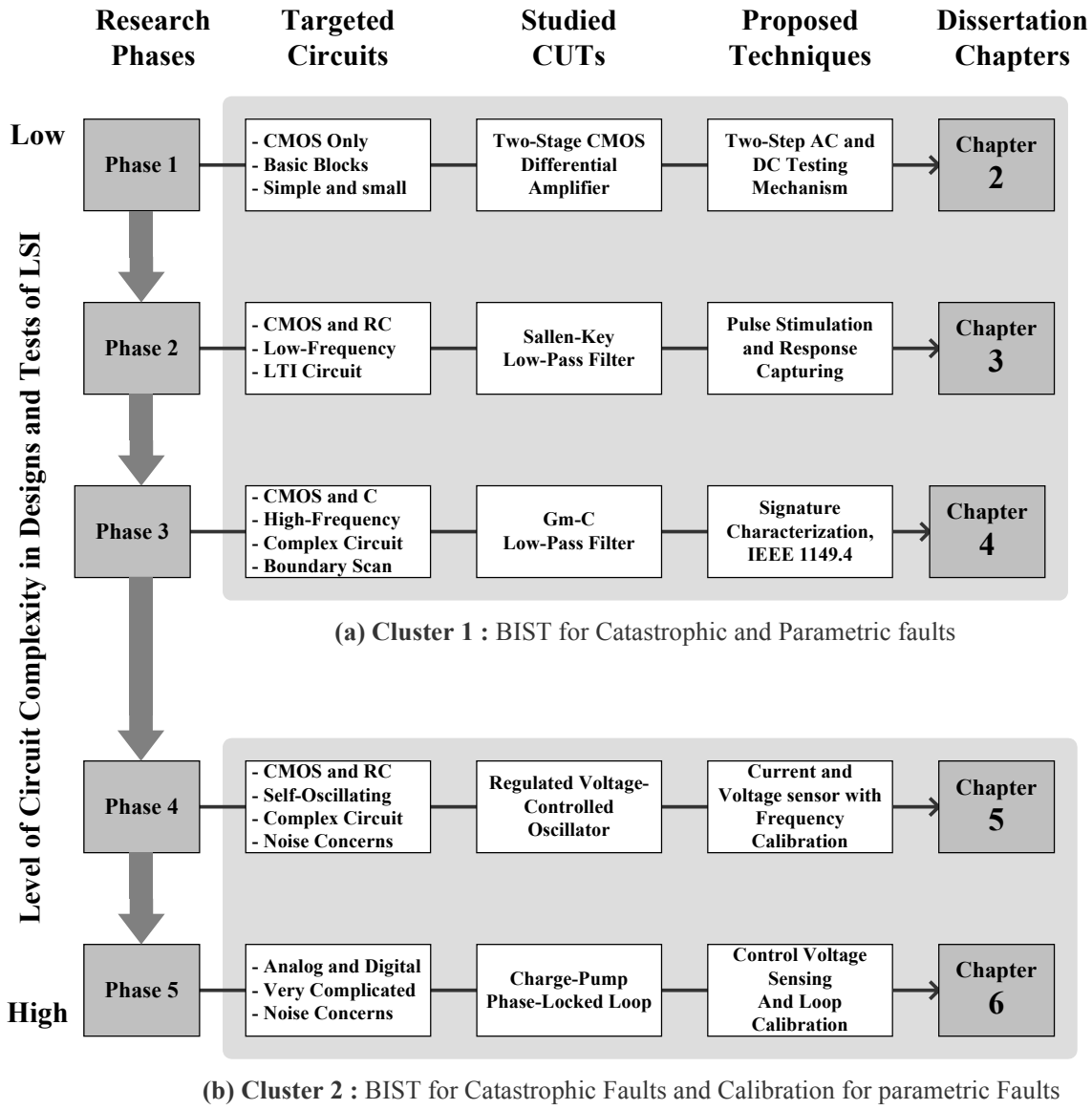



**Fig. 1.7.** Block diagram of scopes and contributions of this dissertation.

extra chip area, especially in small circuit size. Details of the three research phases are described as follows. Phase 1 particularly investigates a compact CMOS-only analog circuit as a simple building block in most LSI systems. A two-stage differential amplifier is chosen as a CUT and the contribution to a new BIST technique is a two-step DC and AC testing mechanism. Phase 2 focuses on a medium size Linear-Time-Invariant (LTI) analog circuit composed by CMOS transistors, resistors and capacitors. The Sallen-Key $2^{nd}$-order low-pass filter, which is commonly used for test demonstrations, is selected as a CUT, and the contribution is new pulse stimulation and response capturing. Phase 3 alternatively considers both a complicated analog circuit and a system implementation compliant to analog and digital boundary scan. The $G_m$-C low-pass filter is chosen as a CUT. The

contributions include a new fault signature characterization technique and the extension of IEEE1149.4 standard analog boundary scans.

As shown in Fig.1.7 (b), the latter two research phases in cluster 2 focuse on BIST and calibration techniques for frequency-based complicated analog mixed-signal circuits. Both test and calibration circuits are suggested to this cluster due to the possibility of frequency calibration. Since these circuit types are relatively complicated, comprising vast number of transistors, and calibrations foster a cost reduction in the case where parametric faults exist. Details of two research phases are described as follows. Phase 4 considers a self-oscillating circuit, and the voltage-controlled oscillator is selected as a CUT. The contribution is a new BIST technique based on a current and voltage sensor in power supply regulation system. Phase 5 particularly studies the most complex analog mixed-signal circuit, which is a Phase-Locked Loop, comprising both analog and digital mixed-signal circuits. The contribution is a new voltage control sensing and PLL with frequency calibration.

## 1.5 Thesis Organizations

This thesis is organized into seven chapters. The following chapter 2 presents the first proposed BIST technique based on two-step AC and DC testing mechanisms, which detect faults by monitoring and analyzing the fault signatures through amplitude and offset of sinusoidal voltage signals. This technique simplifies the design of fault-sensing circuits, and provides a single test outputs in digital form, which is applicable in LSI test systems. Details of BIST circuit design and implementation through the use of 0.18-μm CMOS technology are included. Demonstrations of a two-stage CMOS differential amplifier show the percentage of fault coverage and area overhead of 95.45% and 15%, respectively.

Chapter 3 presents the BIST technique that employs a new simultaneous pulse generator and a single effective voltage on a transient pulse response for fault detection. Demonstrations of BIST system for Sallen-Key low-pass filter with a cut-off frequency of 500kHz, containing the total number of 67 faults, show high percentage of fault coverage at 95.5%. Experimental results show an area overhead of approximately 12% and low degradation on existing CUT performances. On-chip BIST of four CUT examples and comparisons of other related techniques are also included.

Chapter 4 presents the BIST technique that is a fault signature characterization for embedded analog circuits in mixed-signal LSI compliant with IEEE1149.4 boundary scan standard. Demonstrations have been performed for a $4^{th}$-order Gm-C low-pass filter. Both catastrophic and parametric faults are potentially detectable at the minimum parameter variation of 0.5%. The fault coverage associated with CMOS transconductance operational amplifiers and capacitors is at 94.16% and 100%, respectively. Low performance

degradation has been verified through low deviation of the DC gain and the linearity of values 0.0025% and 0.895%, respectively.

Chapter 5 presents the BIST technique, which is a regulated supply tuning voltage-controlled oscillator with built-in test and calibration. Circuit implementation demonstrates low jitter performance of less than 14.32ps at the oscillation frequency of 200MHz. High and low frequency ranges can be calibrated with the offset frequencies of 22MHz and 20MHz, respectively, through two-bit control signals. Tests for potential shorts and opens show the detected faults of 159 from all 190 faults, resulting in a high percentage of fault coverage at 83.68%.

Chapter 6 presents the BIST technique that has particularly focused on a charge pump phase-locked loop (PLL), which is a significant mixed-signal circuit in a variety of applications. This technique is the integration of power supply regulation system in a charge pump PLL that offers power supply noise suppression and facilitates built-in test and calibration system. Demonstrations were performed for a 200-MHz charge pump PLL. Stable reference voltages against changes in the supply voltage were therefore readily obtainable at 1.2V with high PSR performances of –78dB. This supply regulated PLL consequently produces smaller RMS jitters of approximately 12ps for all cases, indicating the capability of supply noise suppression. The expected center frequency was 200MHz at the input control voltage of 0.65V, and three frequency ranges are adjustable with frequency offset of 20MHz, i.e. ranging from 180MHz to 220 MHz. Potential shorts and opens were detectable and test output correctly reports failure status for all cases.

Chapter 7 finally draws a conclusion of all five techniques, which have demonstrated a compact implementation using a few number of compact components while maintaining high average fault coverage of greater than 80%, which is sufficient for cost-effective on-chip prescreening process.

# Chapter 2

## BIST Technique using Two-Step Measurement of AC and DC Output Signal Characteristics

### 2.1 Introduction

This chapter presents the compact on-chip testing scheme for detecting catastrophic faults in the pre-screening of defective small analog building blocks. This chapter commences by the reviews on four examples of related AC and DC testing techniques. Subsequently, the BIST technique based on two-step AC and DC testing mechanisms, which detect faults by monitoring and analyzing the fault signatures through amplitude and offset of sinusoidal voltage signals is presented. This technique simplifies the design of fault-sensing circuits, and provides a single test output in digital form, which is applicable in LSI systems. Details of BIST circuit design and implementation through the use of 0.18-μm CMOS technology are included. Demonstrations of a two-stage CMOS differential amplifier show the percentage of fault coverage and area overhead of 95.45% and 15%, respectively.

### 2.2 Reviews on Related AC and DC Signal-Based BIST Techniques

Table 2.1 summarizes existing BIST techniques based on the monitoring of DC and AC signals, which are initially reviewed as related BIST techniques to the first proposed BIST technique in this chapter. Four particularly related BIST techniques for operational amplifiers have previously been proposed by *Dufaza and His* (1996), Harjarni and *Vinnakota* (1997), *Current and Chu* (2001), and *Font et al.* (2003). As summarized in Table 2.1 (a), *Dufaza and His* (1996) firstly presented an investigation on an operational amplifier with an evaluation technique for optimizing the tolerance band, and discussing a DC pattern with minimal number of test points for the detection of catastrophic defects. Fig.2.1 (a) and (b) show the operational amplifier with two diction nodes ($V_1$ and $V_2$), and the Built-In Voltage Sensor (BIVS), respectively. The CUT is an amplifier and consists of transistors $M_1$ to $M_{10}$. In test mode, the amplifier is configured as buffer. This technique is

**Table 2.1.** Summary of four particularly related BIST techniques.

| Authors | Years | CUTs | BIST Techniques |
|---|---|---|---|
| (a) *Dufaza and His* | 1996 | CMOS Op-Amp | Built-in DC Voltage Sensor |
| (b) *Harjarni and Vinnakota* | 1997 | CMOS Op-Amp | AC-based Analog Observer |
| (c) *Current and Chu* | 2001 | CMOS Op-Amp | AC-based Input/Output Detector |
| (d) *Font and et al.* | 2003 | CMOS Op-Amp | Built-in AC Current Sensor |

the detection of two voltages $V_1$ and $V_2$. It was concluded that the voltage $V_1$ could potentially detect open faults, while the voltage $V_2$ could detect short faults. Therefore, it can be deduced that the combination of $V_1$ and $V_2$ delectability allows detecting the maximal number of considered defects. Based on the tolerance band ($V_{min}$, $V_{max}$) set by the inverter switching voltage, Fig.2.1 (b) shows the BIVS composed by an inverter (INV), a buffer (BUFF) and a NAND gate. This buffer is designed with two serial invertors. The lower limit $V_{min}$ of the tolerance band corresponds to the intersection point between BUFF low to high and NAND high to low voltage responses. The upper limit $V_{max}$ of the tolerance band corresponds to the intersection point between INV high to low and NAND low to high voltage responses. Fault simulations performed on a two-stage amplifier have proved that 100% of catastrophic fault lists totally covered by the observation of only two voltage test points.

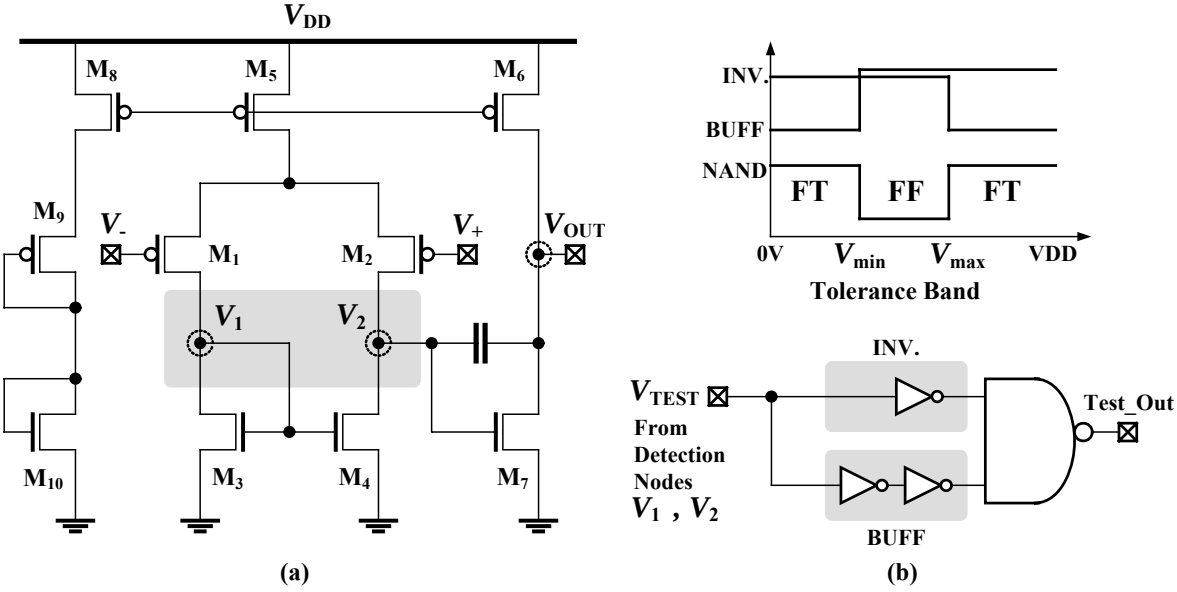



**Fig. 2.1.** The operational amplifier with two diction nodes and the built-in voltage sensor with the description of tolerance band (*Dufaza and His*, 1996).

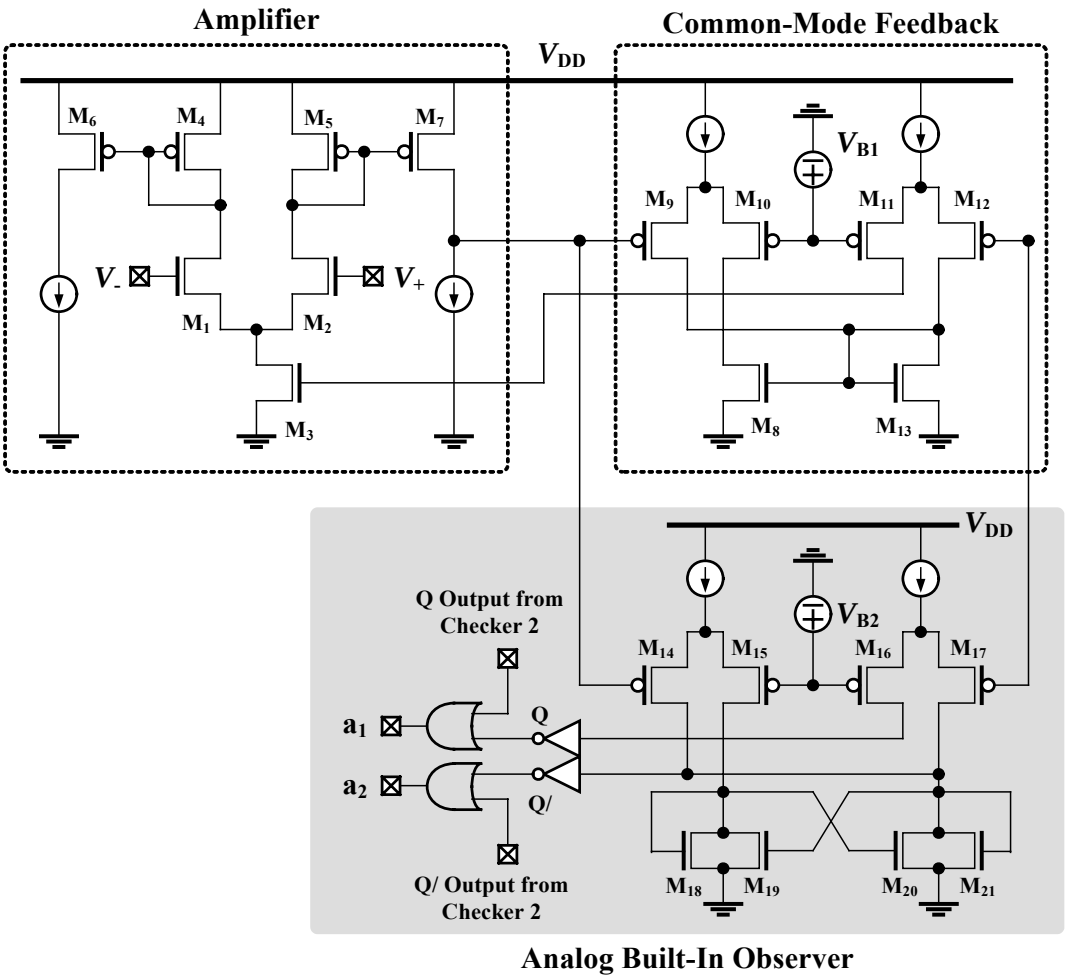



**Fig.2.2.** The amplifier-under-test and built-in observer (*Harjarni and Vinnakota*, 1997).

As summarized in Table 2.1 (b), *Harjarni and Vinnakota* (1997) introduced an analog circuit observer (ACOB) for analog and mixed-signal circuits. The ACOB is a structure designed to reduce the need for precision in measuring analog signals during test operations. Fig.2.2 shows the amplifier-under-test and the built-in analog observer. The circuit consists of a differential amplifier, a common-mode feedback, and the analog circuit observer. First, the fully differential amplifier consists of transistors $M_1$ to $M_7$. Second, the common-mode feedback circuit, consisting of transistors $M_8$ to $M_{13}$, measures the difference between the common-mode voltages and the bias voltage $V_{B1}$. This voltage difference is then amplified and used to set the quiescent common-mode voltage of the output terminals. Last, the analog circuit observer formed by $M_{14}$ to $M_{21}$ with some digital logics is designed to detect a shift in the common-mode voltage of the output. Two checkers are employed, i.e. one to detect a positive shift and another to detect a negative shift. During normal operation, the common-mode voltage of the operational amplifier is vary due to a number of reasons including finite CMRR, limited common-mode feedback bandwidth, switching noise, and nominal process variations. The latch provides a steady

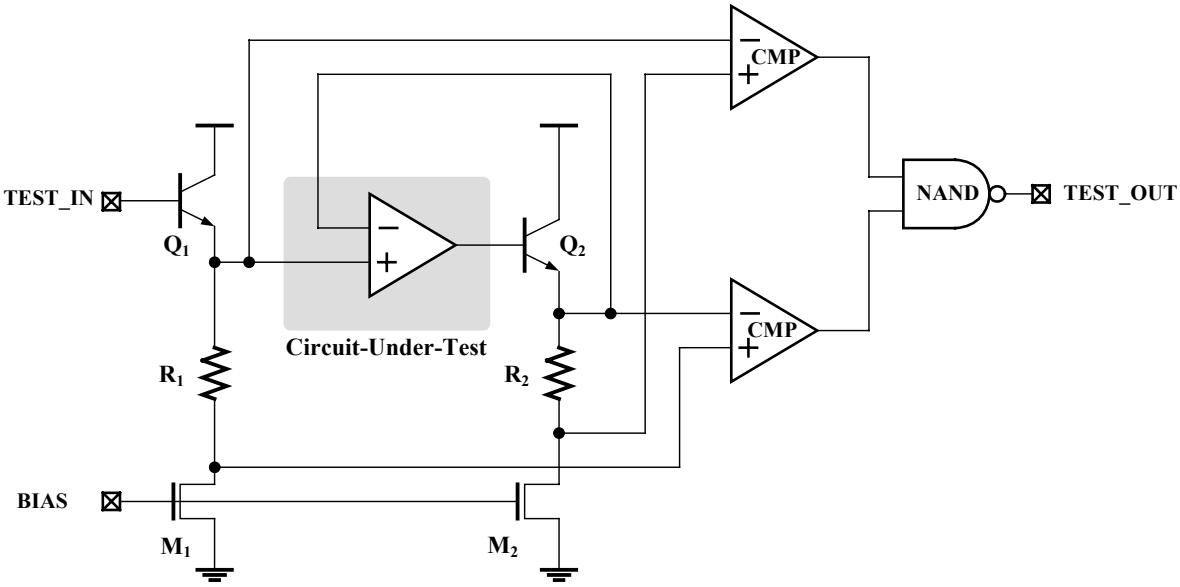



**Fig.2.3.** The operational amplifier with self testing scheme (*Current and Shu*, 2001).

fault detection signal. Latched signals from several checkers can be combined to form a scan chain. It is also necessary to include some hysteresis in the checkers. The ACOB potentially offers a number of advantages over off-chip test techniques such as reduced tester complexity, smaller measurement induced errors, and increased observability.

As summarized in Table 2.1 (c), *Current and Chu* (2001) has proposed a simple and straightforward test technique through AC input and output signal comparisons. Fig.2.3 shows the operational amplifier with self-test scheme. Additional circuits required for the op amp testing include one source follower, two comparators, two current sources, two downshift resistors, and two additional switches per functional block. The op amp under test is connected as a voltage follower driven by a self-test signal through BJT transistor $Q_1$, and the output is given at BJT transistor $Q_2$. The resultant output is then compared to the test input meanwhile the output is also compared to the original input. The range covered by the input signal is used to verify the input common-mode range. The comparison results are employed to verify that the output signal appropriately follows the input signal within an acceptable tolerance set by voltage shifts. The required test input can be generated on-chip by charging a capacitor through high impedance voltage dividers and buffering the ramp signals using source or emitter followers. The shifted copies of signals are generated by connecting current sources to input and output terminals through resistors $R_1$ and $R_2$. It should be noted that precise input common-mode range cannot be checked, but a nominal range can be verified. The output tolerances will not be highly accurate. However, tolerance error can be minimized by biasing the downshift current sources with resistors matched to those of the downshifting circuits.

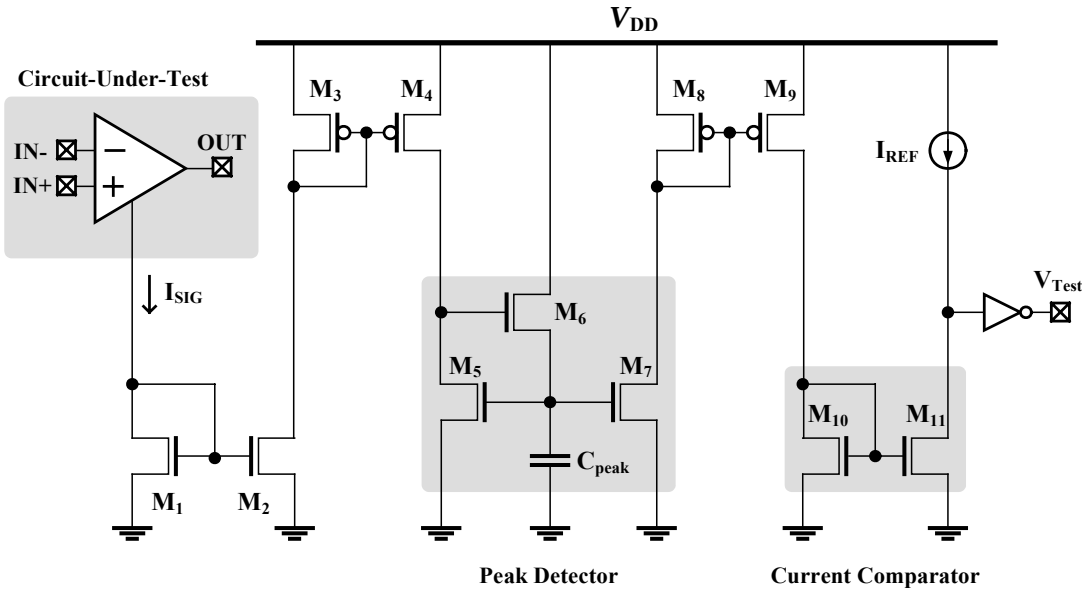



**Fig.2.4.** The built-in current sensor proposed by *Font and et al.* (2003).

As summarized in Table 2.1 (d), *Font and et al.* (2003) has presented a Built-In Current Sensor (BICS) based on the monitoring of a signature of the supply current peak of CMOS operational amplifier using the Oscillation-Based Test (OBT) strategy, i.e. the amplifier is configured as an oscillator under the test mode. Fig.2.4 shows the circuit configuration of the BICS. This BICS takes a sample of the current through current mirrors formed by transistors $M_1$ to $M_4$, and monitors a current signature $I_{SIG}$ of the peak value under oscillation. The peak detector, formed by transistors $M_5$ to $M_7$ and a capacitor $C_{peak}$, provides a DC level of the oscillated supply current. This DC level is subsequently conveyed to the current comparator and some digital circuitry are used to provide a pass/fail flag. Simulation results in 0.35-μm N-well CMOS technology show fault coverage of 97% (39 faults defected out of 40). The area overhead due to the current sensor is about 17%. Although this BICS implementation presents very good fault coverage and negligible impact on the performance characteristics of the amplifier, the area overhead is relatively high. The mismatch in current mirrors may result in low precision of current measurements

## 2.3 Proposed BIST Technique using Two-Step Measurement of AC and DC Signal Characteristics

The proposed BIST technique is a two-step AC and DC testing technique, which checks the defective CUT by monitoring the fault signatures through output voltage signal characteristics. Typically, the characteristics of output voltage signals can be described in the form of a sinusoid equation, i.e.

**Table 2.2.** Summary of fault signature characteristics, and symbolized codes.

| Fault Signatures | | Codes |
|---|---|---|
| (a) Change in magnitude of peak-to-peak $V_m$ | | $F_{00}$ |
| (b) Change in offset voltage $V_{DC}$ | Magnitude change | $F_{01}$ |
| | Stuck-at-$V_{DD}$ | $F_{10}$ |
| | Stuck-at-$G_{ND}$ | $F_{11}$ |

$$v(t) = V_{DC} + V_m \sin(\omega t + \Phi) \tag{2.1}$$

where $V_{DC}$ is the offset voltage, $V_m$ is the signal amplitude, ω is the frequency in radians, and Φ is a phase shift in degrees. Based on this equation, the catastrophic faults can cause changes in all parameters in which fault signatures can be detected. However, fault signatures, which are monitored through the parameters ω and Φ, generally require complicated measuring devices such as spectrum analyzers and phase detectors. In this work, the AC testing is defined as detection of the changes in $V_m$ while the DC testing is defined as detection of the changes in $V_{DC}$ of the sinusoidal output signals. The testing procedure is performed in two steps, i.e. testing $V_m$ and $V_{DC}$ consecutively, and hence called a two-step AC and DC testing technique. This strategy aims to achieve the on-chip testing feature for the testing in the pre-screening of defective chips before high precision testing. Table 2.2 summarizes the characteristics of fault signatures and the correspondingly symbolized codes. The change in $V_m$ is the decrease or the increase in magnitude of peak-to-peak amplitude represented by the code $F_{00}$. In addition, the change in $V_{DC}$ is the decrease or the increase in magnitude of the DC offset represented by the code $F_{01}$. However, the stuck-at-$V_{DD}$ and stuck-at-$G_{ND}$ levels are distinct, coded as $F_{10}$ and $F_{11}$. This strategy is a non-intrusive testing approach, which does not require the CUT configuration changes, and offers a digital-oriented test output in which the Pass/Fail test output is reported in the form of digital logic values.

Fig. 2.5 shows a flow diagram of the test procedure, designing by means of characteristics of the four fault signatures shown in Table 2.2. Starting with AC testing, a sinusoidal input signal is applied to the CUT and the expected output is also a sinusoid. If the test output is steady at $V_{DD}$ (High) or ground (Low) states, the faults $F_{10}$ and $F_{11}$ will be detected. Additionally, the fault $F_{00}$ will also be detected in cases where the amplitude is not sufficient to switch periodically between High and Low states. If the output is a sinusoid, the flow will continue to the DC testing process where the sinusoidal input signal is removed, and the input is connected to an external DC reference voltage for comparison. If the test output is High, fault $F_{01}$ will be detected. Finally, the flow ends when the test output is Low. Fig.2.6 shows design and test methodology in three processes. First, the

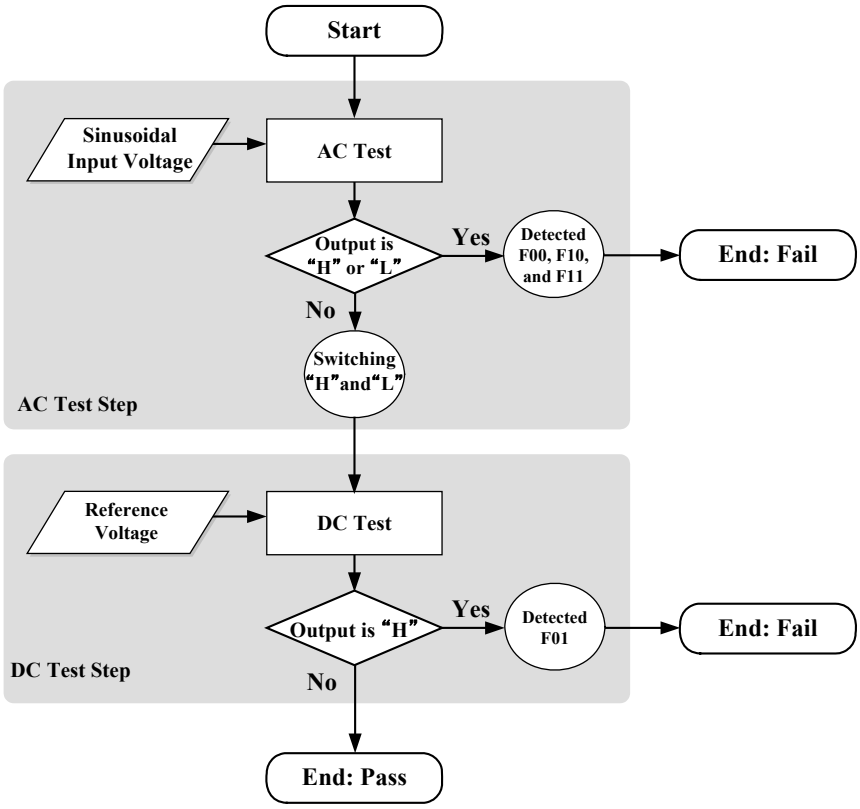



**Fig. 2.5.** Flow diagram of test procedures of the two-step AC and DC test technique.

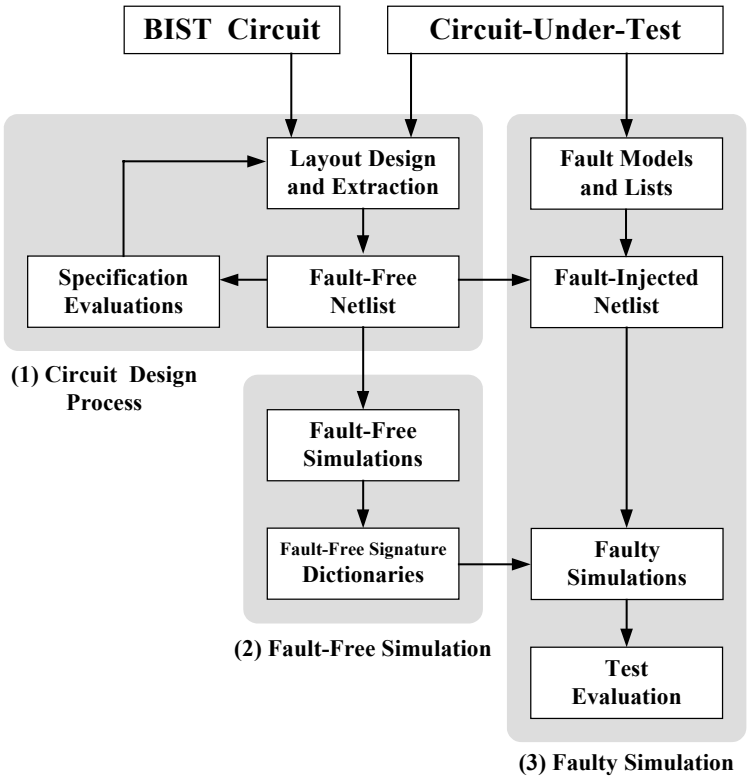



**Fig. 2.6:** Block diagram of design and test method with three test processes.

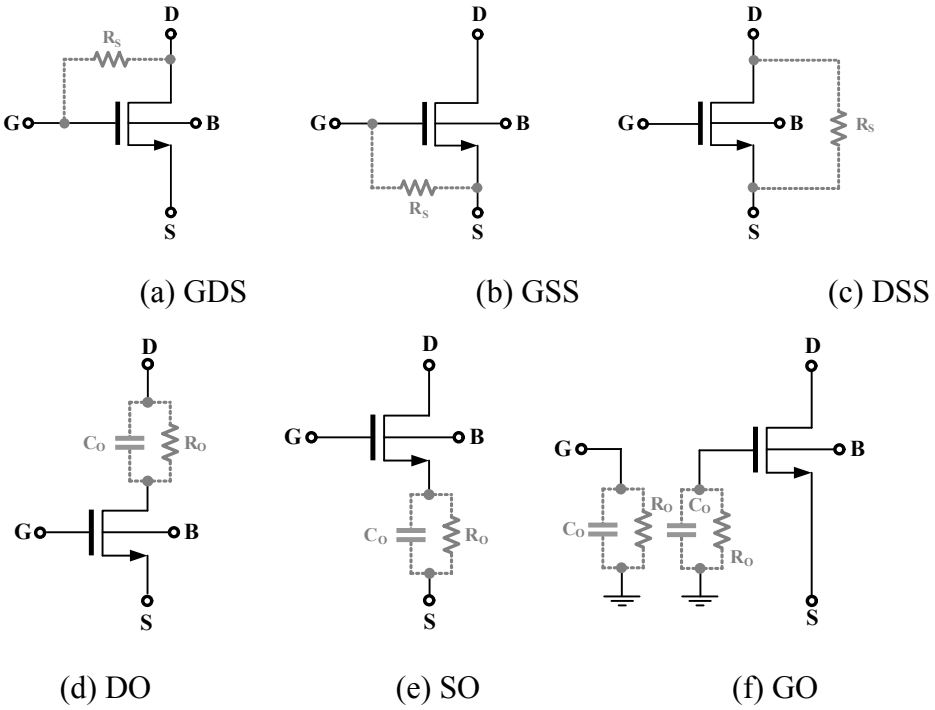



**Fig. 2.7.** Fault models; (a) GDS, (b) GSS, (c) DSS, (d) DO, (e) SO, and (f) GO.

layout is designed and extracted. The netlist obtained from layout extraction is primarily used in the simulation for evaluating CUT specification. Second, fault-free simulation is performed after the CUT specification has been achieved. This fault-free simulation provides data on the magnitude of $V_{DC}$ and $V_m$ of the output voltage. This data will be stored as fault dictionaries for later references. Finally, the fault list, which covers all possible catastrophic faults, is defined. Each fault in this list is injected into the fault-free netlist independently and the faulty simulation is performed at a single time.

As a number of standard digital fault models are in existence, fault simulations in digital CMOS integrated circuits can be realized at all levels of abstraction, ranging from behavioral to layout. However, there is no standard fault model for analog integrated circuits. Therefore, fault simulations are realized mostly at the transistor level by inserting resistors into the CUT. Insertion of transistors provides a sufficient simulation of the electrical behavior of shorts and opens, and offers low complexity fault modeling suitable for most types of CUT. Fig.2.7 shows circuit diagrams of possible catastrophic fault models in an nMOS transistor. Shorts are modeled by connecting a small resistor ($R_S$) between each pair of terminals, including (a) Gate-Drain Short (GDS), (b) Gate-Source Short (GSS), and (c) Drain-Source Short (DSS). Additionally, opens are modeled by inserting a parallel combination of a large resistor ($R_O$) and a small capacitor ($C_O$) in series into each terminal, including (d) Drain Open (DO) and (e) Source Open (SO). However,

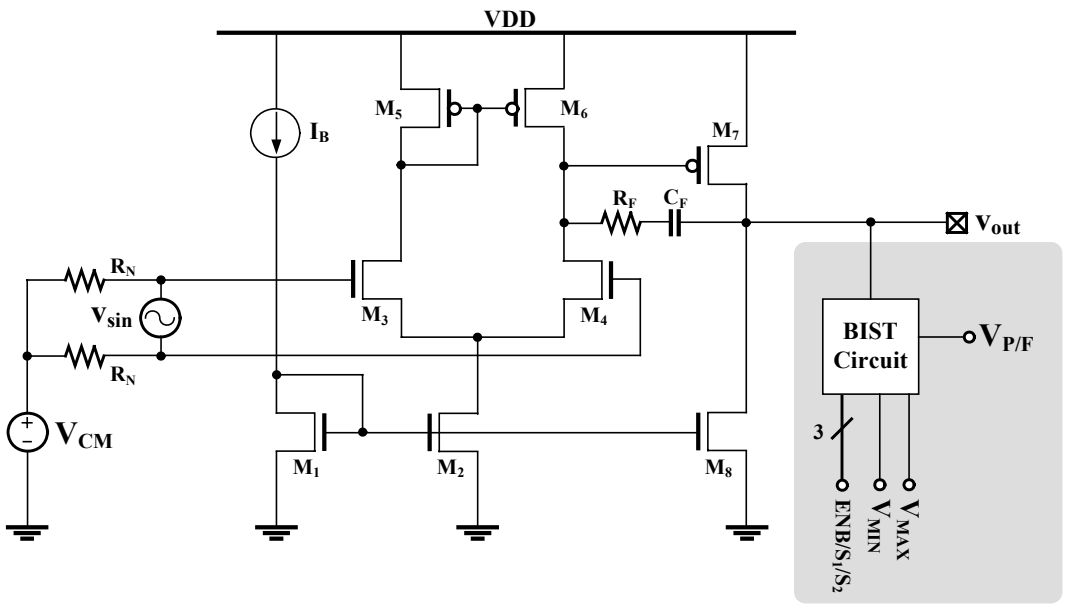



**Fig. 2.8.** A two-stage differential amplifier with BIST Circuit.

the Gate Open (GO) is not easily modeled and thus generally excluded from the fault list in many works. As direct insertion of $R_O$ at the gate terminal is not effective for simulating real behavior of GO, this work therefore realizes GO by means of grounded $R_O$ and $C_O$ at the two disconnecting terminals as illustrated in Fig.2.7 (f), in order to eliminate the voltage discontinuity in simulation process.

## 2.4 Circuit Designs and System Implementations

### 2.4.1 Design of a Two-Stage Differential Amplifier as a CUT

Fig. 2.8 shows the circuit diagram of the CUT, which is a CMOS differential amplifier, and the BIST circuit. The CUT comprises four major components, i.e. an nMOS current-mirror bank formed by transistors $M_1$, $M_2$ and $M_8$, an nMOS differential pair formed by transistors $M_3$ and $M_4$, a pMOS current mirror formed by transistors $M_5$ and $M_6$, and a pMOS amplifying transistor $M_7$. This CUT is biased by a single power supply voltage $V_{DD}$ and a bias current source $I_B$. The small signal input voltage $v_{sin}$ and the common-mode voltage $V_{CM}$ are connected through the large resistors $R_N$. As for testing output signals, an open-loop gain of the CUT is exploited for input signal amplification. Fig.2.9 shows the small-signal analysis diagram of the two-stage amplifier. The low-frequency open-loop gain of the op-amp is calculated as the product of each gain stage, and is given by

$$A_{OP} = \left(g_{mN}\left(r_{oN} \,//\, r_{oP}\right)\right)\left(g_{mP} r_{oP}\right) \tag{2.2}$$

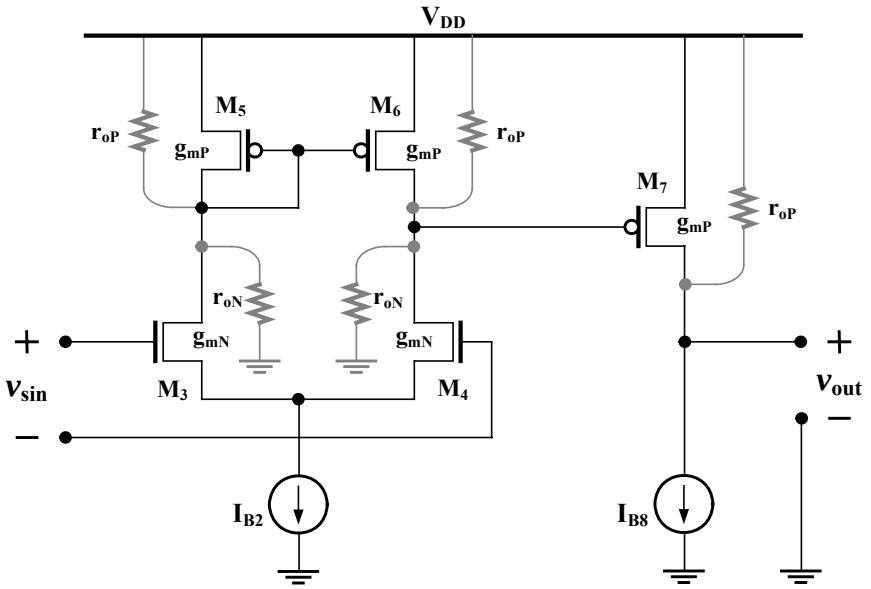



**Fig. 2.9.** Small-signal analysis diagram of the two-stage differential amplifier.

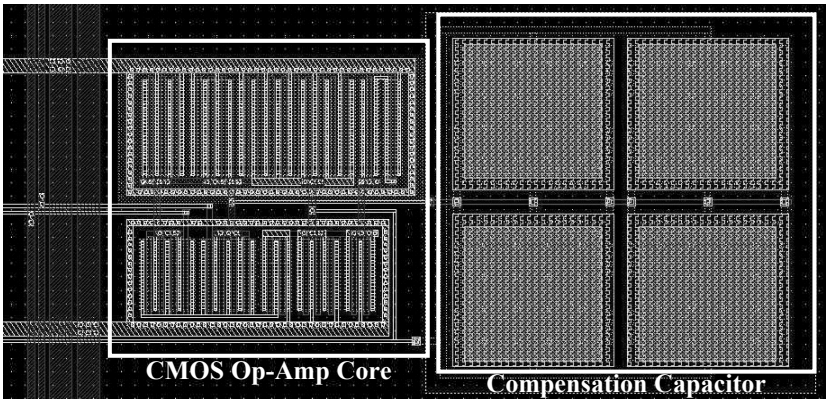



**Fig. 2.10.** Layout design of a differential amplifier with BIST Circuit.

where $g_{mN}=g_{m3}=g_{m4}$ is a transconductance of the nMOS transistor, and $g_{mP}=g_{m7}$ is a transconductance of the pMOS transistor. The parameter $r_{oN}=r_{o3}=r_{o4}$ is an output resistance of the nMOS transistor, and $r_{oP} = r_{o7}$ is an output resistance of the pMOS transistor. It should be noted that transistors $M_3$ and $M_4$ are identical and $M_5$ and $M_6$ are also identical in order to reduce the input offset voltage. The DC power dissipation can be calculated as

$$P_{DC} = V_{DD}\left(I_B + I_{B2} + I_{B8}\right) \tag{2.3}$$

Additional $C_F$ and $R_F$ are a frequency compensation component where this $C_F$ introduces the dominant pole. For unity feedback stability, the phase shift from the other poles and zeros at the unity gain bandwidth cannot exceed $90^o$ minus the required phase margin. In

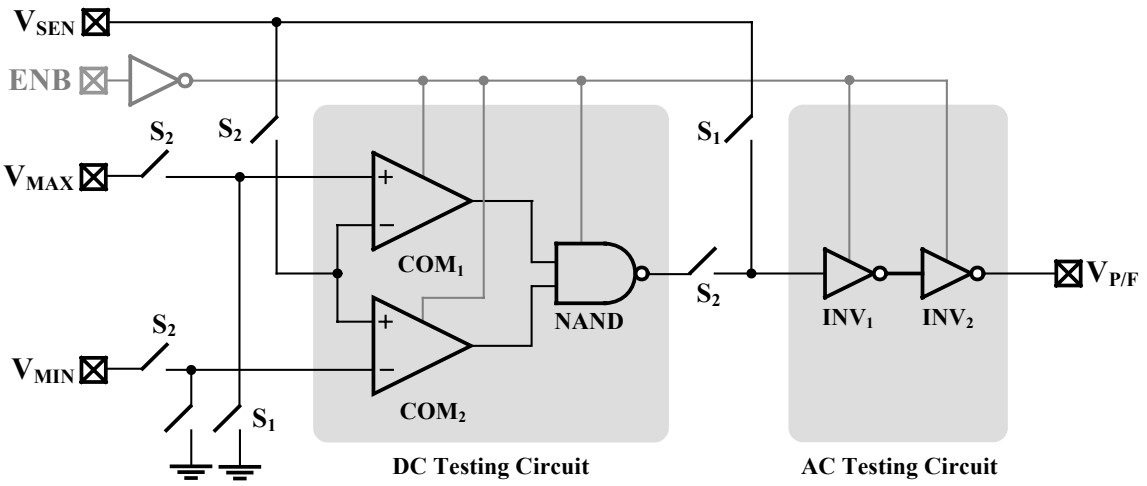



**Fig. 2.11.** Circuit diagram of the proposed BIST circuit based on two-step AC and DC testing technique.

the case of a dominant pole with the resistor $R_F$ and the capacitor $C_F$, the unity gain bandwidth is approximately given by

$$\omega_C = \frac{g_{mN}}{C_F} \tag{2.4}$$

In this design, the use of the open-loop gain offers a wide range of test frequency prior to a unity-gain bandwidth and simplifies the need for re-connecting the CUT as a buffer, especially for later cascaded connection with other amplifiers. With reference to the fault models shown in Fig. 2.7, a total of 44 faults existed in the CUT, of which 18 were shorts and 26 were opens. Fig.2.10 shows the corresponding layout of the differential amplifier.

### 2.4.2 Design of the BIST circuit and Operations

Based on the proposed technique shown in Fig. 2.5, the corresponding BIST circuit is designed using simple analog and digital circuits with switching mechanisms. Fig. 2.11 show circuit diagram of the proposed BIST circuit, respectively. As shown in Fig. 2.11, the DC testing circuit was designed based on comparison of DC voltages. This DC testing circuit consists of two comparators ($COM_1$ and $COM_2$), and a single NAND gate. The two comparators compare the DC input voltage values, where minimum and maximum points are determined by the external voltages $V_{MIN}$ and $V_{MAX}$, respectively. Comparison results are finally processed by NAND gate in order to provide a single logical test output. In this DC testing circuit, the faults $F_{00}$ and $F_{01}$ can be detected, excluding hard-to-detect faults, which produce no fault signatures.

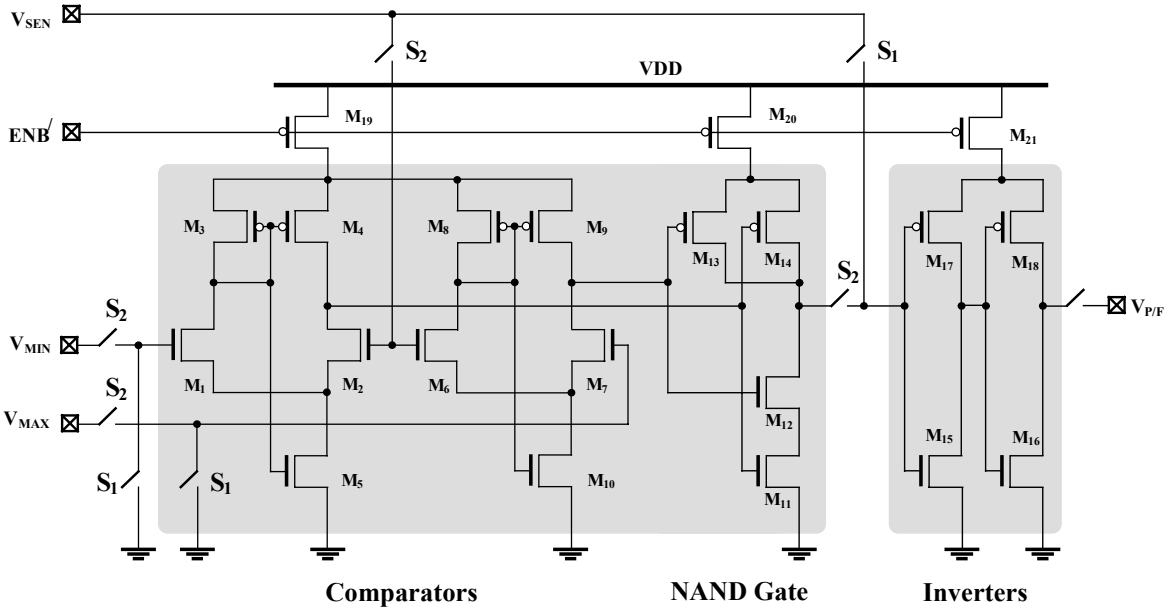



**Fig. 2.12.** Circuit configuration of the proposed BIST circuit based on two-step AC and DC testing technique.

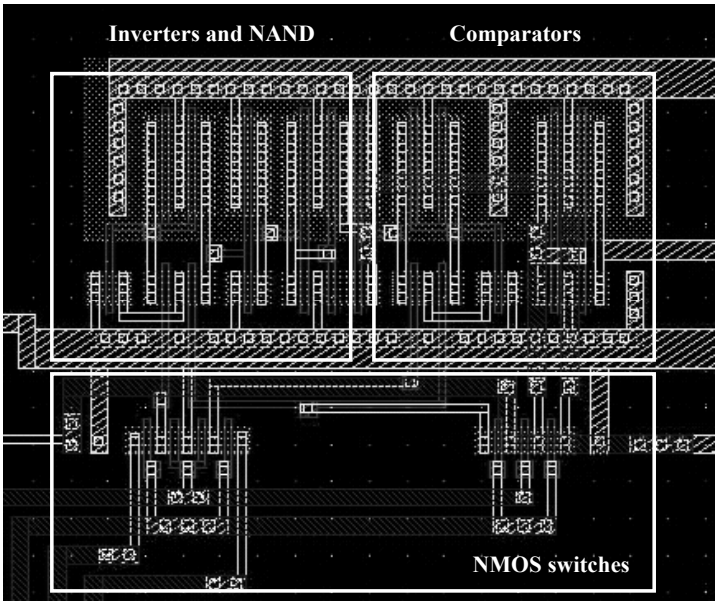



**Fig. 2.13.** Layout diagram of the BIST circuit based on two-step AC and DC testing technique.

The AC testing circuit was designed based on the switching characteristics of two identical inverters ($INV_1$ and $INV_2$), which are connected in series and designed for equal values of the switching voltage point ($V_{SP}$). In this AC testing circuit, faults $F_{10}$ and $F_{11}$ can be detected instantly as there is no signal alternation over $V_{SP}$. Additionally, faults $F_{00}$ and $F_{01}$ can also be detected in cases where the maximum of positive peak and the minimum of

**Table 2.3.** Circuit operations of the two-step AC and DC testing technique;
√ = Connected, × = Removed, H = 1.8V, L=0V, SW = Switching.

| Modes | Control Signals | | | Inputs/ Outputs Signals | | | | | Test Results |
|---|---|---|---|---|---|---|---|---|---|
| | **ENB** | $S_1$ | $S_2$ | $v_{sin}$ | $V_{CM}$ | $V_{MIN}$ | $V_{MAX}$ | $V_{PF}$ | |
| Normal | L | H | L | √ | √ | × | × | - | - |
| Step 1 | H | H | L | √ | √ | × | × | H | Faulty |
| | | | | | | | | L | Faulty |
| | | | | | | | | SW | Next Step |
| Step 2 | H | L | H | × | √ | √ | √ | H | Faulty |
| | | | | | | | | L | Fault-Free |

negative peak are lower and higher than $V_{SP}$, respectively. In addition to AC and DC testing circuits, switches $S_1$ and $S_2$ were included for controlling the two-step switching mechanisms. The active-high enable signal (ENB) was also included for disconnecting testing circuits during normal operation to eliminate extra power consumption. Fig. 2.12 shows the circuit configuration of the proposed BIST circuit based on two-step AC and DC testing technique. As shown in Fig. 2.12, two comparators $COM_1$ and $COM_2$ consist of $M_1$ to $M_5$, and $M_6$ to $M_{10}$, respectively. These two comparators were designed using a self-biased differential amplifier in which no external bias voltage is required for setting the operating currents. The NAND gate, consist of $M_{11}$ to $M_{14}$, is realized by a typical 4-transistor digital logic gate. The inverters, consisting of $M_{15}$ to $M_{18}$, were realized by typical digital inverter configuration. Three transistors $M_{19}$, $M_{20}$ and $M_{21}$ operate as enabling switches in order to allow $V_{DD}$ to be connected to the test circuits. Fig.2.13 shows the layout diagram of the BIST circuit based on two-step AC and DC testing technique.

Table 2.3 describes the operations of the testing circuit. In normal mode, the sinusoidal signal, i.e. $V_x = v_{sin} + V_{CM}$ where $v_{sin}$ and $V_{CM}$ are a small-signal voltage and a common-mode voltage, respectively, is applied to the CUT. Additionally, the testing circuit is disconnected from the CUT. In testing modes, the AC testing is performed with the presence of $v_{sin}$ and $V_{CM}$ as the first step. Initially, the control signals ENB, $S_1$ and $S_2$ were set to High, High and Low, respectively. After setting, the output voltage from the CUT is applied to the AC testing circuit. The fault is detected if the test output $V_{PF}$ is steadily at either High or Low. If $V_{PF}$ is periodically switching between High and Low, the test will continue to the second step. The second step is DC testing where the control signals ENB, $S_1$ and $S_2$ are now set to High, Low and High, respectively. After setting, the output signal of the CUT is still applied to the DC testing circuit, and the AC testing circuit is connected to the output of the DC testing circuit in order to operate as a buffer. In this second step, $v_{sin}$

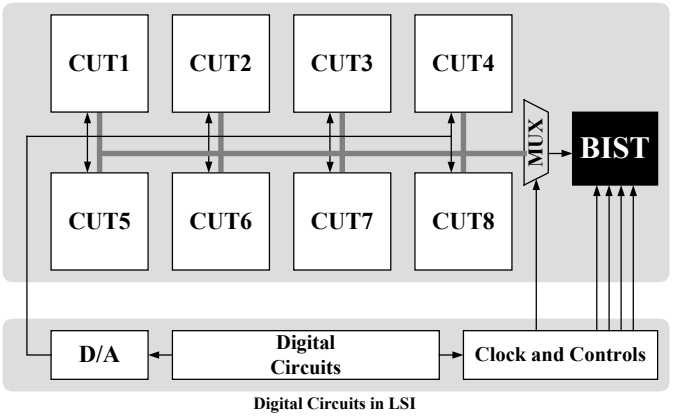



**Fig. 2.14**. Block diagram of the BIST system based on two-step AC and DC testing technique, containing 8 examples.

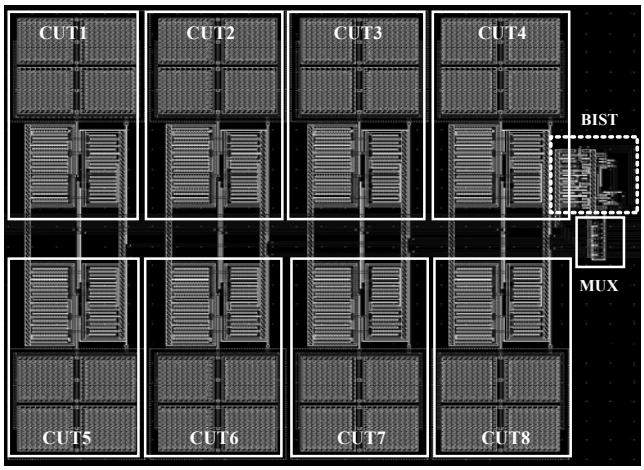



**Fig. 2.15**. Layout diagram of the overall designed BIST system based on two-step AC and DC testing technique.

is removed leaving only $V_{CM}$ as the input signals for the CUT. The fault is detected if the output is Low. If the output is High, the circuit can be considered as either fault-free or as having some hard-to-detect faults. Fig.2.14 depicts the system architecture of the proposed testing scheme. Different types of analog circuits can be checked through the multiplexer corresponding to the fault-free dictionaries. The control signals and clocks are assumed to be provided sufficiently from the control system of digital circuitry in LSI. It can be seen from Fig.2.14 that eight particular CUT examples were designed. The $CUT_1$ and $CUT_2$ are fault-free operational amplifier and its redundant one as a reference, respectively. The $CUT_3$ to $CUT_8$ were included for demonstrating different fault types. With reference to Fig. 2.8, the faulty $CUT_3$ has a GDS at $M_3$. The faulty $CUT_4$ has a GO at $M_7$. The faulty $CUT_5$ has a DSS at $M_5$. The faulty $CUT_6$ has a SO at $M_4$. The faulty $CUT_7$ has a GO at $M_1$. The faulty $CUT_8$ has a short at $R_F$. Fig. 2.15 shows the layout diagram of the overall designed BIST system based on two-step AC and DC testing technique.

**Table 2.4.** Comparison of simulated performances between the CUT with and without BIST circuit.

| Performances | Simulated Values | | |
|---|---|---|---|
| | **Original CUT** | **CUT With BIST** | **Units** |
| Offset voltage | 57 | 57 | μV |
| DC gain | 73.5 | 73.5 | dB |
| UGBW | 56 | 56 | MHz |
| PM | 67 | 67 | Degree |
| Slew rate | +56 /-44 | +53/-44 | μV/S |
| ICMR | 0.55 - 1.76 | 0.55 - 1.75 | V |
| PSRR | 98.81 dB | 98.81 dB | dB |
| Power | 198 | 198 | μW |

**Table 2.5.** Summary of characteristics of the BIST circuit.

| **Performances** | | **Values** | **Units** |
|---|---|---|---|
| DC test circuit | Operating range $V_{MAX}$ | 1.36 | V |
| | Operating range $V_{MIN}$ | 0.04 | V |
| | Fault-free region | 0.80-0.88 | V |
| | Offset Error | <0.12 | % |
| AC test circuit | $V_{SP}$ | 0.87 | V |

## 2.5 Results and Discussions

### 2.5.1 Simulation Results

Initially, the overall BIST system was designed using Cadence and simulated through Hspice. The technology is a 0.18-μm standard CMOS Technology. Table 2.4 shows the comparison of simulated performances between the original CUT and the CUT with BIST circuit where the values of $V_{DD}$ and $I_B$ were set at 1.8V and 30μA, respectively. Primarily, the CUT was designed for a DC gain of greater than 70dB, a phase margin (PM) of $67^o$, and a unity gain bandwidth (UGBW) at 56MHz. These specifications were compensated using $R_F$ and $C_F$ of values 2.5 kΩ and 0.4pF, respectively. It is seen in Table 2.4 that inclusion of the BIST circuit does not cause performance degradation in normal operation. This is because the nMOS switches operate as large resistances, disconnecting the BIST circuit from the CUT, and no significant loading effects is apparent.

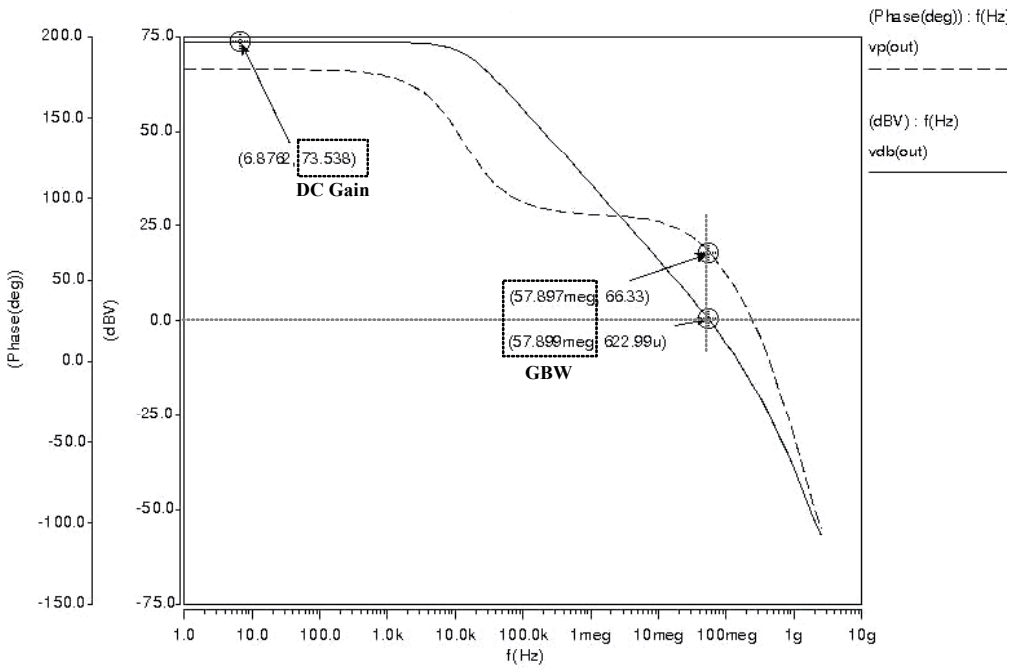



**Fig.2.16**. Simulated Bode plot characteristics of the operational amplifier.

In high-frequency operations, parasitic capacitances of these two switches may have a loading effect on settling time. However, this effect is not significant as stray capacitances are relatively small compared to gate capacitances of input transistors in the next stage or load capacitances.

Table 2.5 summarizes the characteristics of the BIST circuit. As can be seen from Table 2.5, the operating range of $V_{MIN}$ and $V_{MAX}$ is tunable in the region of 0.04V to 1.36V. The offset error over the entire operating range is less than 0.12%. In addition, the switching point of the AC circuit is 0.78V. These values can be adjusted for different types of circuits based on the acceptable band. Subsequently, fault simulations were performed based on the fault models depicted in Fig.2.8 where $R_S$ and $R_O$ are 1Ω and 10MΩ, respectively. The capacitor $C_O$ in all the opens was 1fF. The amplitude and frequency of $v_{sin}$ were 0.1V and 1KHz, respectively. The resulting fault-free investigation output voltage had peak-to-peak amplitude and offset of 0.9V and 0.85V, respectively. As for testing catastrophic faults, the acceptable band was setting to ±5% deviation of the fault-free output voltage. Fig.2.16 shows the simulated Bode plot characteristics of the operational amplifier. It can be seen that the DC gain and GBW are approximately 73.5dB and 57 MHz, respectively. Fig.2.17 illustrates the testing waveforms and control signals of the fault $F_{10}$ where the input and output signals are a stuck-at-$V_{DD}$ (1.8V) and High state logic signal, respectively. Fig.2.18 illustrates the testing waveforms of the fault $F_{00}$ where the input and output signals are a gain-reduced sinusoid and a periodically switching state logic signal, respectively. Fig.2.19 illustrates the testing waveforms of the fault $F_{01}$ where the input and output signals are a

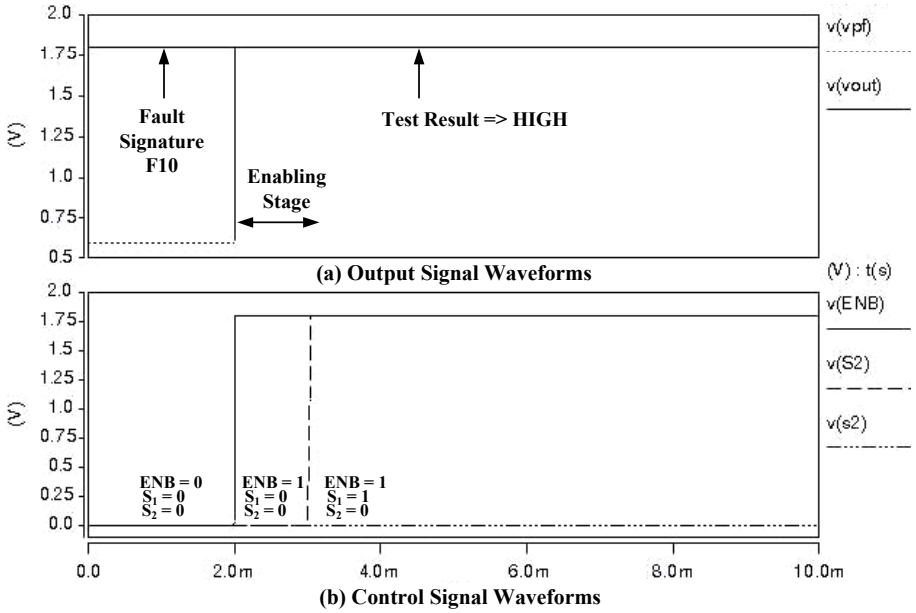



**Fig.2.17.** The waveforms of input, output, and control signals of the fault $F_{10}$.

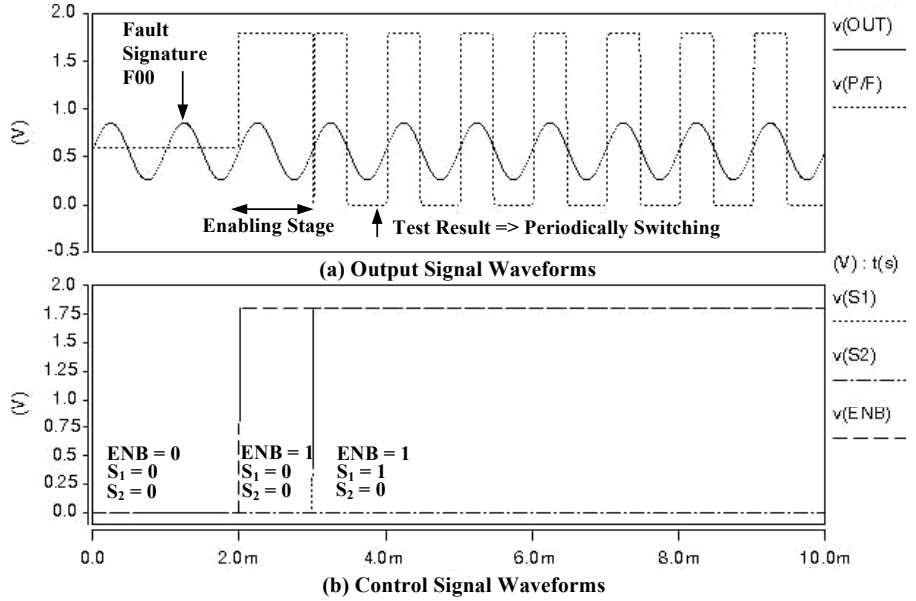



**Fig.2.18.** The waveforms of input, output, and control signals of the fault $F_{00}$.

stuck-at-$G_{nd}$ (0V) and High state logic signal, respectively. Table 2.6 summarizes the simulated results of injected and detected faults with fault coverage. The total number of injected faults was 44 and the number of detected faults was 42, yielding the percentage of fault coverage of 95.45%. It can be seen from Table 2.6 that those catastrophic faults DGS, DSS, GSS, DO, and SO in MOS transistors were completely detected. This is because the CUTs failed to operate correctly, i.e. the test outputs mostly exhibited stuck-at-$V_{DD}$ and stuck-at-Gnd. Short and open in the compensation capacitor were also detectable. However, the open at the Gate terminals of the transistor $M_1$ in Fig. 2.8 was not detected. It is assumed that the gate voltage of transistors $M_1$ and $M_2$ was sustained at the same value,

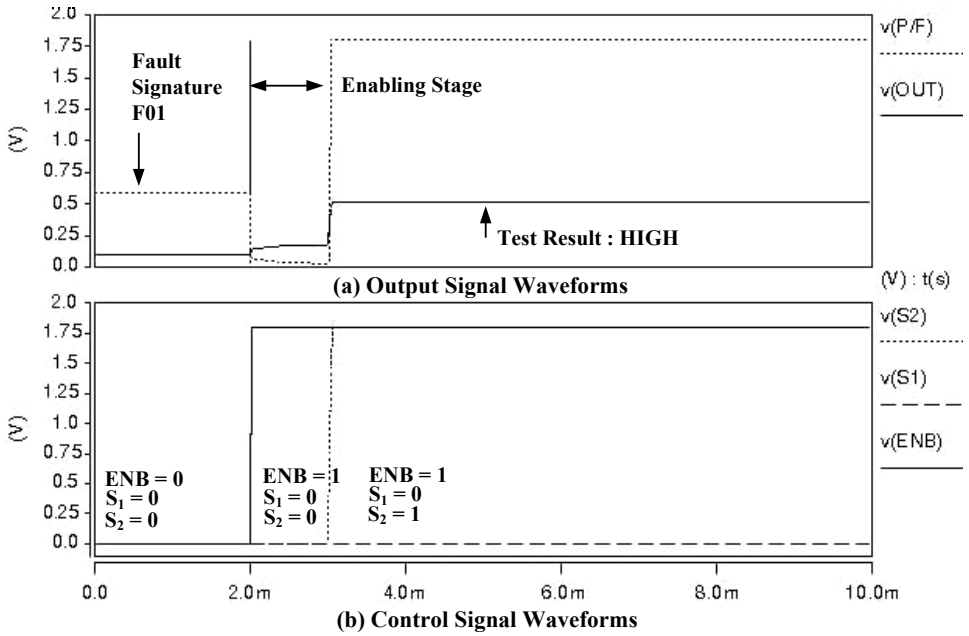


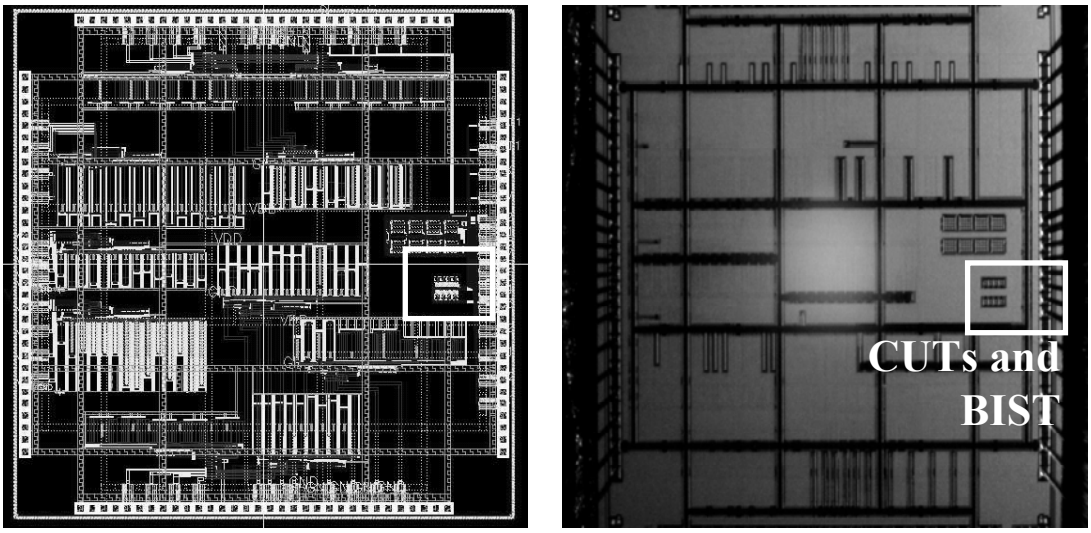

**Fig.2.19.** The waveforms of input, output, and control signals of the fault $F_{01}$.

and therefore the bias current is still supplied to the overall circuit components. Additionally, the potential short at the frequency compensation resistor $R_F$ was not detected. It is suspected that the short at this resistor does not change the DC condition of the overall circuit components. Nonetheless, the functional test at high frequency operation would encounter this fault as the GBW is changed, causing the amplifier to be unstable. These types of fault are acceptable at this pre-screening stage and can be considered as hard-to-detect faults.

**Table 2.6.** Simulated results of injected and detected faults with fault coverage.

| Fault Types | Injected Faults | Detected Faults | % Fault Coverage |
|---|---|---|---|
| Drain-Gate Shorts | 6 | 6 | 100% |
| Drain-Source Shorts | 8 | 8 | 100% |
| Gate-Source Shorts | 2 | 2 | 100% |
| Drain Opens | 8 | 8 | 100% |
| Source Opens | 8 | 8 | 100% |
| Gate Opens | 8 | 7 | 87.5 |
| Capacitor Short/ Open | 2 | 2 | 100% |
| Resistor Short/Open | 2 | 1 | 50% |
| **Total Faults** | **44** | **42** | **95.45%** |

### 2.5.2 Experimental Results




(a) (b)

**Fig.2.20.** Photographs of experiments; (a) the top-cell layout, (b) the fabricated chip.

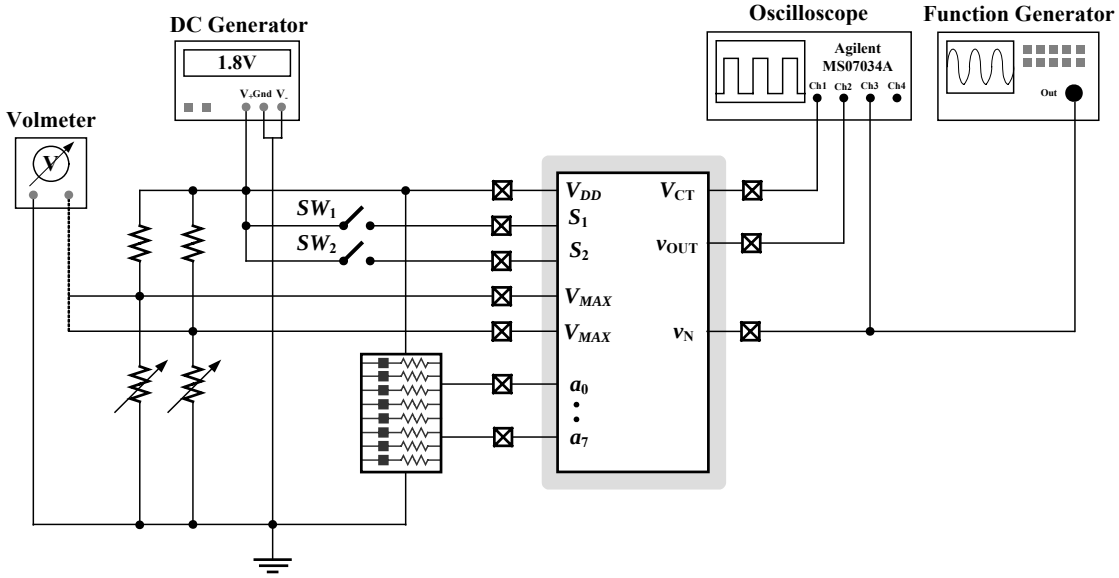



**Fig.2.21.** Photographs of experiments; (a) the top-cell layout, (b) the fabricated chip.

The experimental results were carried out through an available chip model VDEC-PC430-BU7074-AF. Fig. 2.20 (a) and (b) show the photographs of the top-cell layout and the fabricated chip, respectively. Fig.2.21 shows photographs of experiments; (a) the top-cell layout, (b) the fabricated chip. It should be noted that this chip also contains other digital circuits as for academic proposes. The experimental set up employed two function generators as input signal resources for both normal operations and test modes. A

**Table 2.7.** Experimental results of injected and detected faults.

| CUTs | Injected Faults | Test Output $V_{PF}$ | Fault Detected |
|---|---|---|---|
| $CUT_1$ | Fault-Free | 0 | No |
| $CUT_2$ | Fault-Free | 0 | No |
| $CUT_3$ | GDS at $M_3$ | 1 | Yes |
| $CUT_4$ | DSS at $M_5$ | 1 | Yes |
| $CUT_5$ | DO at $M_8$ | 1 | Yes |
| $CUT_6$ | SO at $M_4$ | 1 | Yes |
| $CUT_7$ | GO at $M_1$ | 1 | Yes |
| $CUT_8$ | Short at $R_F$ | 0 | No |

single DC voltage generator was also employed for a voltage supply of 1.8V and for DIP switches. The output test signal is observed through the oscilloscope, i.e. $V_{PF}$=0V for low state that shows the fault-free status and $V_{PF}$=1.8V for high state that shows the faulty status. Table 2.7 summarizes experimental results of injected and detected faults of the test chip. As shown in Table 2.7, the two $CUT_1$ and $CUT_2$ correctly provide test output at low state, indicating fault-free status. Four $CUT_3$ to $CUT_6$ also correctly provide test output at low state, indicating faulty status. The undetected open fault from simulation result, i.e. GO at $M_1$, injected in $CUT_7$ was detected in experimental result. The short of resistor $R_F$ injected in $CUT_8$ was undetected.

Based on the performances in Tables 2.4 to 2.7, the comparison of this work and other four related BIST techniques, which are reviewed previously in Table 2.1, have been made and summarized in Table 2.8. In comparison to previously proposed BIST circuits, particularly for catastrophic fault detection in CMOS two-stage amplifiers, this work provides relatively simple implementation. Evidently, there is no requirement for multiple sensing nodes, BJT transistor, or complicated analog circuits such as a capacitor-based peak detector. Additional requirements of this design are the control signals $S_1$ and $S_2$, and the external reference voltages $V_{MAX}$ and $V_{MIN}$. However, switching mechanisms offer a test for both AC and DC fault signatures, which increases fault coverage. The external reference voltages offer tunability in tolerance adjustment and consequently, as different types of analog circuit have different tolerance. As shown in Table 2.8, two important aspects of BIST techniques are (1) the area over head and (2) the fault coverage. The area overhead of *Dufaza and His* (1996) is very low at 2.5% while this work and Font et al. (2003) are comparable at less than 20%. The area over head of *Harjarni and Vinnakota* (1997) is relatively high at approximately 50%. Considering this work, the area overhead is acceptable at 15%. As a switching mechanism has introduced, this work can be fully

**Table 2.8.** Comparisons of this work and other four related BIST techniques; ×= not reported, SH=Short Fault, OP =Open Fault.

| **Characteristics** | **BIST Techniques** | | | | |
|---|---|---|---|---|---|
| | ***Dufaza & His*** | ***Harjarni & Vinnakota*** | ***Current & Chu*** | ***Font et al.*** | **This work** |
| **Technology** | CMOS | CMOS | Discrete Component | CMOS 0.35-μm | CMOS 0.18-μm |
| **Results** | Simulation | Simulation | Experiment | Simulation | Simulation (Experiment) |
| **CUTs** | Op-Amp | Op-Amp 43 dB@ 28.49 MHz | Op-Amp 71 dB@ 6 MHz | Op-Amp 92.7 dB@ 13.6 MHz | Op-Amp 73.5 dB@ 56 MHz |
| **Input Types** | None | Sinusoid | Sinusoid | None | Sinusoid |
| **Test outputs** | 2 Bits | 2 Bits | 1 Bit | 1 Bit | 1 Bit |
| **Area Overhead** | 2.5 % | 47 % | × | 17 % | 15 % |
| **Fault Models** | SH: 1Ω OP: 100MΩ | × | × | SH: 1Ω OP: 1MΩ | SH: 1Ω OP: 10MΩ |
| **Fault Coverage** | 100% | 95% | × | 97% | 95.45% |

exploited for testing each Op-Amp sequentially by means of a multiplexer, thus providing an even lower area overhead. In the case of fault coverage, *Dufaza and His* (1996) has presented a fault of coverage of a 100%. However, the BIVS technique may suffer from parameter variations after fabrication since the precision of the tolerance band greatly depends on the switching voltage of inverters. In addition, the measurement of two voltages $V_1$ and $V_2$ are from internal nodes of Op-Amp, and therefore performance maybe degraded. Other techniques (*Harjarni and Vinnakota*, 1997; *Font et al*., 2003) showed fault coverage of greater than 95%, which is comparable to this work. In general case, the fault coverage over 80% is acceptable for the pre-screening process of catastrophic defect testing. Therefore, this work offers sufficiently high fault coverage with reasonable area overhead, operating at low power consumption and providing a single bit test output, with no requirement for complex circuits.

## 2.6 Conclusions

This chapter has proposed a two-step AC and DC analog BIST technique, which checks defective circuits by monitoring fault signatures through amplitude and offset of

voltage signals consecutively. The proposed BIST technique was designed particularly for catastrophic fault detection for the pre-screening of defective circuits before high precision testing. Demonstrations of a two-stage differential amplifier using 0.18-μm CMOS technology have shown the fault coverage and the area overhead are 95.4% and 15%, respectively. Comparisons to other related BIST techniques have been made. The advantages of this BIST technique are non-intrusiveness of the testing approach, which does not require the CUT configuration changes, and affordability of digital test outputs. In addition, this BIST technique also offers acceptable catastrophic fault coverage with simple implementation for most types of analog circuits by observing fault signatures at output nodes. Therefore, this BIST technique can be used for cost-effective non-intrusive testing in analog mixed-signal systems.

# Chapter 3

## BIST Technique using Pulse Stimulation and Voltage Sample Capturing on Pulse Responses

### 3.1 Introduction

This chapter presents the BIST technique and implementations in analog domain based on a pulse input stimulus and a single voltage sample captured from pulse responses. This chapter commences by the reviews on related pulse stimulation-based BIST techniques. In this chapter, the proposed technique employs a new pulse generator, which simultaneously provides two short pulses for stimulating a CUT and controlling the sampling process. A single effective voltage on a transient pulse response is initially sampled using a sampled-and-hold circuit and lately employed for fault detection using window comparators. Demonstrations of BIST system for Sallen-Key low-pass filter with a cut-off frequency of 500kHz, containing the total number of 67 faults, show high percentage of fault coverage at 95.5%. Experimental results show an area overhead of approximately 12% with low performance degradation on existing CUT performances. The BIST of four CUT examples and comparisons of related techniques are also included.

### 3.2 Reviews on Related Pulse-Based Test Techniques

Table 3.1 summarizes testing techniques based on pulse model stimulations and pulse response analysis, which are reviewed as related test techniques to the second proposed BIST technique in this chapter. The theoritical analysis on pulse responses and faults modeling proposed by *Su et al.* (2000) is initially reviewed. Three related test techniques for LTI systems previously been proposed by *Singh et al.* (2004), *Variyam et al*. (1997), and *Czaja* (2009) are later involved. As summarized in Table 3.1 (a), Su *et al*. (2000) has introduced pulse response modeling of faults in time domain for LSI circuits. Fig.3.1 shows the block diagram of the fault-free LTI system with parallel and serial fault models. Examples of LTI circuits are passive and active analog amplifiers and filters, which can be characterized entirely through specific input functions such as pulse or step

**Table 3.1.** Summary of related test techniques based on pulse signals.

| Authors | Years | CUTs | Descriptions |
|---|---|---|---|
| (a) *Su et al.* | 2000 | Low-pass filter | Pulse response modelling of faults |
| (c) *Variyam et al.* | 1997 | Sallen-Key low-pass Filter | Random-pulse stimulation and Response sampling |
| (b) *Singh et al.* | 2004 | Universal filter | Differentiator-based impulse response generation and correlation analysis |
| (d) *Czaja* | 2009 | Sallen-Key low-pass filter | Fault detection and localization using Microcontroller-based pulse analysis |

functions. Typically, the transfer function of the LTI system in frequency domain can be described as

$$H(s) = \frac{a_0 + a_1 s + \cdots + a_n s^n}{b_0 + b_1 s + \cdots + b_m s^m} \tag{3.1}$$

where $n \leq m$, and the coefficients $a_h$ and $b_k$ are functions of circuit parameters; $h = 1, 2, ..., n$ and $k = 1, 2, ..., m$. The fault-free LTI system $h(t)$ is characterized by the pulse input $x(t)$. The output response $y(t)$ can be described by convolution operation in time domain, i.e. $y(t)=x(t)*h(t)$, and expressed as

$$y(t) = \int_{-\infty}^{\infty} x(\tau) h(t-\tau) d\tau \tag{3.2}$$

where $\tau$ is a dummy variable for integration. This output response $y(t)$ normally exhibits a certain Gaussian-like pulse shape over a limited time period. In the case where faults exist in the system, the pulse response characteristics may differ from the expected $y(t)$. In order to investigate fault impacts, a parallel fault model $p(t)$ and a serial fault model $s(t)$ can be added independently into the existing $h(t)$. Based on associate and distributive properties of convolution operations, the LTI system with fault models provides two cases of output responses $y_p(t)$ and $y_s(t)$. The output $y_p(t) = x(t)*[h(t)+p(t)]$ is a response of a parallel connection between $h(t)$ and $p(t)$, and can be expressed as

$$y_p(t) = \int_{-\infty}^{\infty} x(t)\left[h(t-\tau) + p(t-\tau)\right] d\tau \tag{3.3}$$

The output $y_s(t) = x(t)*h(t)*s(t)$ is a response of a serial connection of $h(t)$ and $s(t)$, and can be expressed as

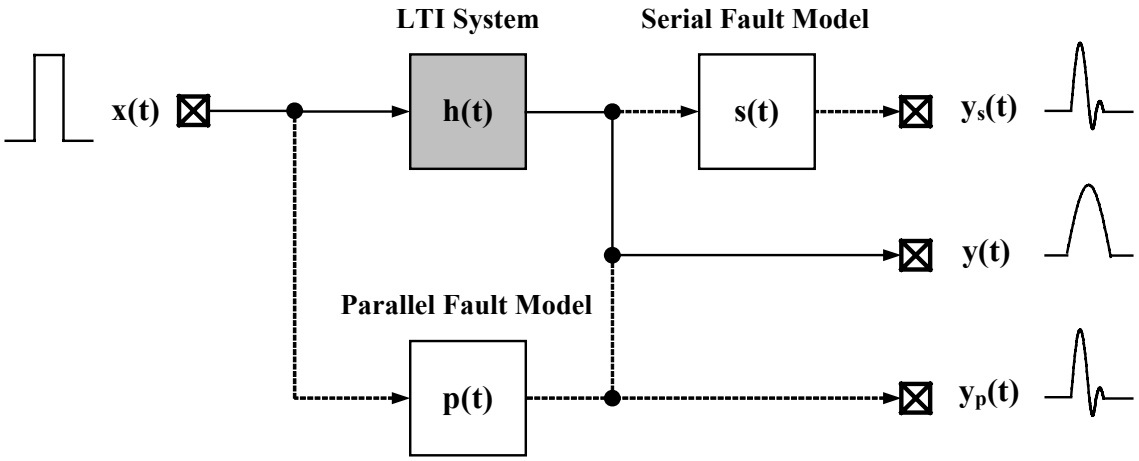



**Fig.3.1.** The fault-free LTI system with possible parallel and serial fault models.

$$y_s(t) = \int_{-\infty}^{\infty}\left(\int_{-\infty}^{\infty} x_{xh}(\tau)h_{hs}(\tau_{hs}-\tau_{xh})d\tau_{xh}\right)s(t-\tau_{hs})d\tau_{hs} \tag{3.4}$$

where $x_{xh}$ is a pulse input signal in the convolution of $x(t)$ and $h(t)$, $h_{hs}$ is a system function in the convolution of $h(t)$ and $s(t)$, $\tau_{xh}$ is a dummy variable for integration associated with the convolution of $x(t)$ and $h(t)$, and $\tau_{hs}$ a dummy variable for integration associated with the convolution of $h(t)$ and $s(t)$. These output responses in the equations (3.3) and (3.4) show apparent changes in pulse response characteristics, depending upon actual functions of $p(t)$ and $s(t)$. Therefore, fault detection based on changes in these pulse responses can be achievable in frequency or time domains.

As shown in Table 3.1 (b), *Variyam et al*. (1997) has early proposed a BIST architecture using random pulse width stimulation and pulse response sampling for analog circuits. This technique employs rectangular pulses of random widths obtained directly from a digital Linear Feedback Shift Register (LFSR) to perform transient testing of the CUT, while synchronization and comparison circuitry perform the BIST operations. Fig. 3.2 shows the overall BIST architecture. As depicted in Fig. 3.2, the random pulse generation is accomplished by the frequency divider and the digital LFSR blocks. Such random pulse widths exhibit many frequencies determined by LFSR characteristic polynomials in order to achieve high fault coverage. As also shown in Fig. 3.2, the pulse response analysis is primarily performed by the sampling process, i.e. pulse responses are sampled by the sampling clock, which is divided from the main input clock. The sampled voltage values are subsequently compared with the reference voltage $V_{REF}$, generating a digital bit stream for the fault signature compaction circuit. Finally, the signature compaction circuit analyses bit streams through the optimization of tolerance band in cooperation with the delayed sampling clock. The advantage of this technique includes the simple implementation where no A/D converter and external DSP are required. However,

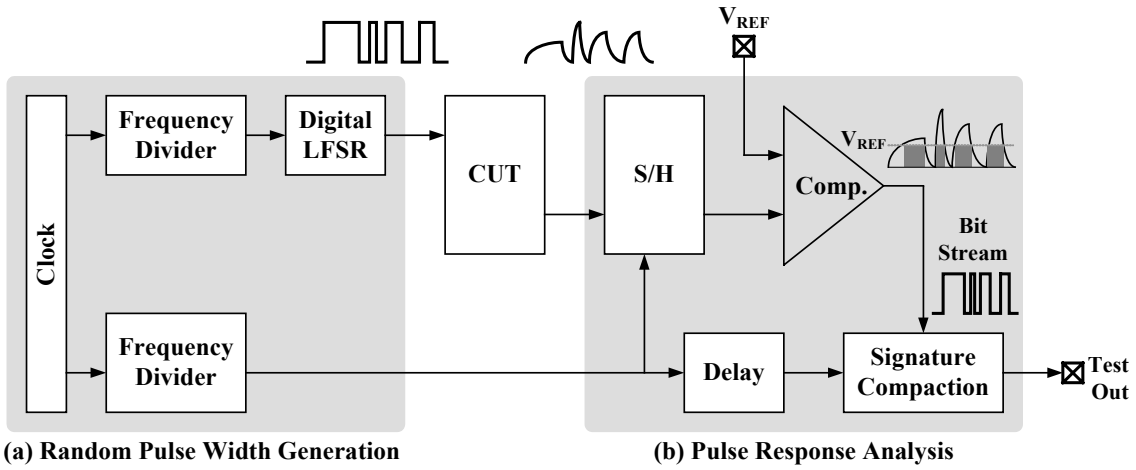



**Fig.3.2.** Random pulse width stimulation, and pulse response analysis in the BIST architecture proposed by *Variyam et al*. (1997).

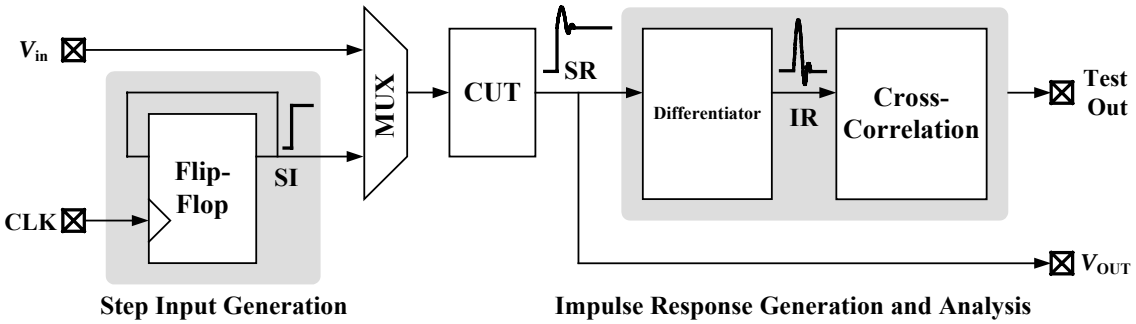



**Fig.3.3.** Step input and impulse response generations with cross/auto-correlation analysis proposed by *Singh et al*. (2004).

complicated algorithms for LFSR and signature compaction circuit remain difficulties, as different CUTs require different algorithms.

As shown in Table 3.1 (c), *Singh et al*. (2004) has proposed pulse generation technique based on the on-chip generation of the impulse response signatures from the corresponding step response. Fig. 3.3 shows step input and impulse response generations with cross/auto-correlation analysis. As shown in Fig.3.3, the step input signal is generated by a single flip-flop, which may be applied externally though primary inputs or by on-chip digital logics. Such a step input is applied to the CUT, generating the step response at the output with some settling behaviors. In order to perform fault analysis, this step response is subsequently converted in to the impulse response through a differentiator. The resulting impulse response is employed for fault analysis using cross/auto-correlation technique. It can be considered that this technique has been proposed to circumvent the need to apply pseudorandom patterns as proposed by *Variyam et al*. (1997). In addition, post processing

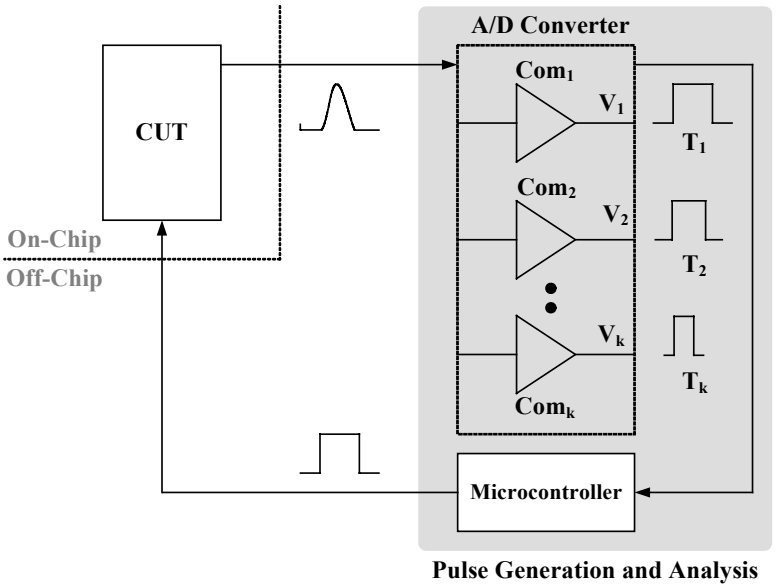
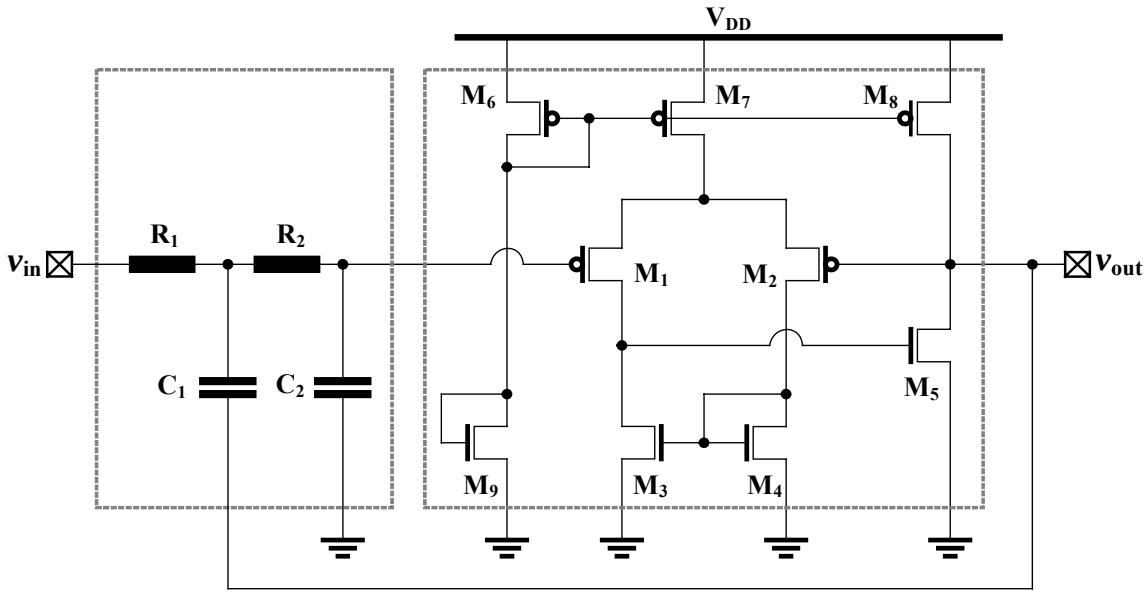



**Fig.3.4.** The BIST architecture using Microcontroller-based pulse response analysis proposed by (*Czaja*, 2009).

using cross/auto-correlation has been proposed to efficiently compare impulse response signatures through a statistical approach based on linear regression and outlier analysis. However, the implementation of differentiator on-chip occupies as large area as the CUT in some cases since an operational amplifier with linear capacitor and resistors are necessary. Another difficulty is an externally statistical analysis, and hence there is no complete BIST since external DSP and programming are required.

As shown in Table 3.1 (d), *Czaja* (2009) has proposed the method of fault detection and localization of analog parts in embedded mixed-signal systems controlled by microcontrollers. Fig. 3.4 shows the BIST architecture proposed by *Czaja* (2009). As can be seen in Fig.3.4, the system consists of three stages. Firstly, stimulations of the tested analog part are performed by means of a square impulse with programmable duration time generated by the microcontroller. Secondly, the measurement of duration times $T_1$, $T_2$,..,$T_K$ of output signals of the $K$ analog comparators with different threshold voltages $V_1$, $V_2$,..,$V_K$ generated by the internal timer of the microcontroller is performed. The output signals are subsequently converted by analog comparators from the time response of the analog part into a square impulse. Finally, fault detection and the localization are realized by the microcontroller based on a measurement result, a fault dictionary and a diagnosis procedure are located in its program memory. The main advantage of the method is cost-effective BIST, which consists only of analog comparators and internal resources of the microcontroller mounted in the system. Nonetheless, the application is limited for those systems, containing microcontrollers and algorithms with specific fault dictionary are necessary.




**(a) A Two-Stage RC Network** **(b) A Buffer Amplifier**

**Fig.3.5.** Circuit configuration of a second-order Sallen-Key low-pass filter.

## 3.3 Proposed BIST Technique using Single Pulse Stimulation and Voltage Response Capturing on Pulse Responses

### 3.3.1 Preliminary Investigations on Pulse Response Characteritics

In order to investigate the fault influences on pulse response waveforms and to evaluate the effectiveness of the use of a narrow width pulse as an input test stimulus, defect-oriented simulations in schematic level were preliminarily conducted. The demonstrated CUT was a 2nd-order Sallen-Key low-pass filter, which offers high linearity and low-noise properties for the implementation of integrated analog base-band filters in RF receivers such as in IEEE 802.11wireless LAN (*Razavi*, 1999) or in CDMA receivers (*Yee et al*., 2000). Fig.3.5 shows the circuit configuration of the Sallen-Key low-pass filter, comprising two major blocks, i.e. a linear RC network and a unity-gain buffer. The linear RC network is formed by two resistors ($R_1$, $R_2$) and two capacitors ($C_1$, $C_2$). The unity-gain buffer was implemented based on a two-stage differential amplifier, consisting of nine CMOS transistors ($M_1$ to $M_9$). The corresponding 2-pole Butterworth transfer function in $s$-domain denoted as $H_f(s)$ can be expressed as

$$H_f(s) = \frac{(2\pi f_c)^2}{s^2 + \frac{2\pi f_c}{Q} s + (2\pi f_c)^2} \tag{3.5}$$

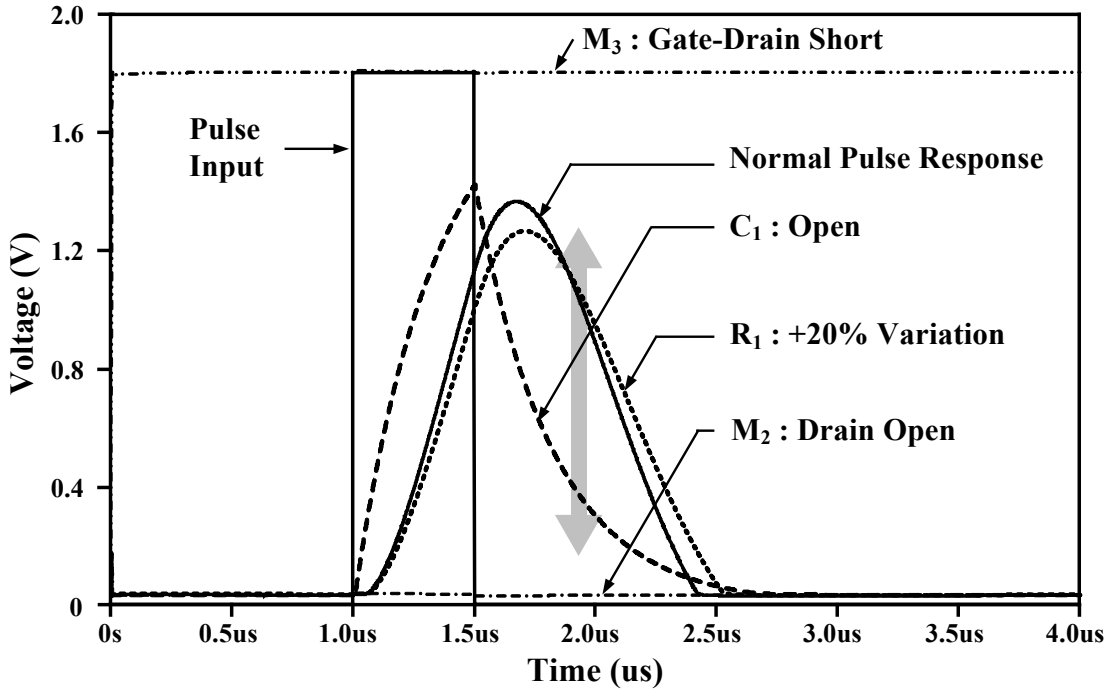



**Fig.3.6.** Transient waveforms of a normal pulse response and four examples of faulty pulse response waveforms.

where $f_c$ and $Q$ are cutoff frequency and quality factor, respectively. It is seen from (3.5) that the transfer function $H_f(s)$ exhibits a 2nd-order LTI system, which satisfies the criteria of $H(s)$ described in (3.1), and is therefore capable to provide the proper pulse response characteristics. As for example, an analog baseband filter with the cutoff frequency of 450 kHz to 500 kHz and a unity quality factor was designed. The values of the resistors $R_1$ and $R_2$ were equally selected at 84 kΩ, and the values of the capacitors $C_1$ and $C_2$ were 8 pF and 2 pF, respectively. The width of the pulse input signal was set at 0.5μs. Since different types of CUTs exhibit different and specific transfer functions, this pulse width of 0.5μs was optimized from a trial and error process so that the output signal possesses a symmetric and narrow pulse response shape.

The injections of catastrophic and parametric faults were primarily performed for fault behavior investigations. In the case of catastrophic faults, shorts and opens were realized by the insertion of a resistor into each component as previously depicted in Fig.2.7. In the case of parametric faults, the component variation was realized where the practical component variations are in an extensive range from 10% to 50%. For purpose of demonstrations, Fig. 3.6 shows the transient waveforms of a normal pulse response and four examples of faulty responses. Such four examples of faults include +20% variation of $R_1$, open at $C_1$, drain open at $M_2$, and gate-drain short at $M_3$. It is seen from Fig.3.6 that the variation in $R_1$ causes small changes in charging and discharging periods, whereas shorts and opens in $C_1$, $M_2$, and short in $M_3$ cause

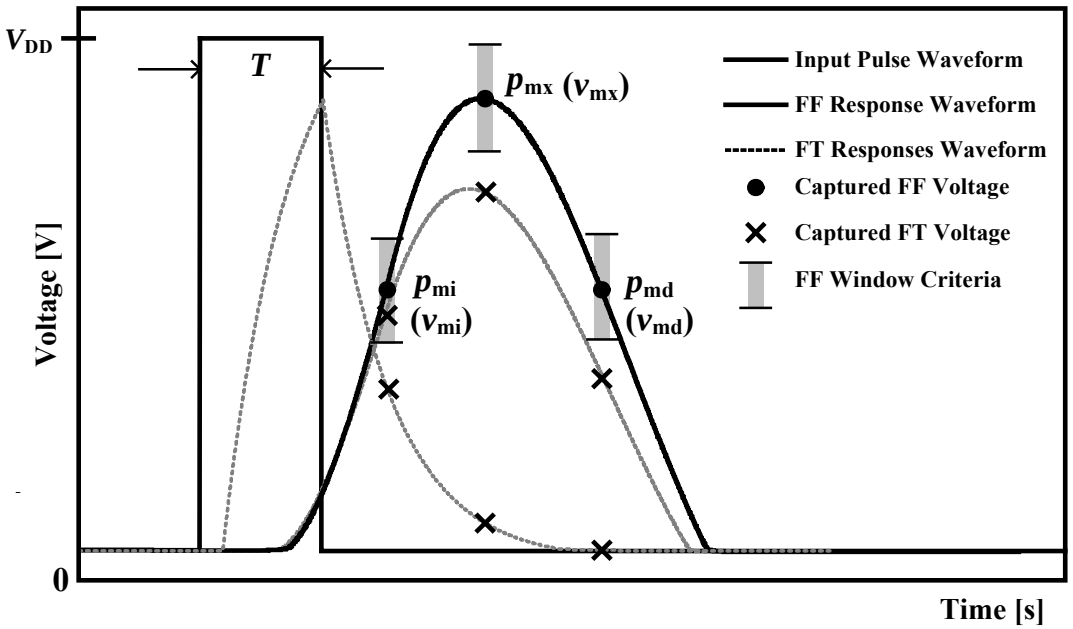



**Fig.3.7.** Demonstrations of a pulse input and pulse response with window criteria.

tremendous changes in pulse response waveforms. As expected, the parametric faults cause small variations whereas the catastrophic faults cause hard changes in pulse response waveforms. In addition, Fig.3.6 also indicates that vertical variations in voltages can be exploited for fault detection.

### 3.3.2 Proposed BIST Technique

Fig.3.7 shows a pulse input, a normal pulse response of a fault-free CUT with window criteria, and two pulse response examples of faulty CUTs. The input is a rectangular pulse with a short duration $T$, and the normal pulse response possesses symmetrically Gaussian-like characteristics. The two pulse response examples of defective CUTs demonstrate significant changes in pulse response characteristics caused by the presence of faults. For purpose of fault detection, this work realizes an approximate investigation of three voltage samples $v_{mi}$, $v_{mx}$ and $v_{md}$ on the normal pulse response, which are sampled at three points $p_{mi}$, $p_{mx}$, and $p_{md}$, respectively. The points $p_{mi}$ and $p_{md}$ are midpoints of increasing and decreasing periods, respectively, while the point $p_{mx}$ is the maximum point. It can be investigated in Fig.3.7 that the values of voltage samples of faulty conditions captured at the three points are significantly different from those of original voltages $v_{mi}$, $v_{mx}$ and $v_{md}$ in the fault-free condition. Therefore, the approximate monitoring of voltage samples on the pulse response waveform can be realized for the pre-screening low-cost fault detection process.

General aspect of this test technique is the use of a single pulse as an input test stimulus, enabling a compact implementation of on-chip test stimuli. High-precision sinusoidal signals or complicated test stimuli is not required. In addition, the output response characterization is based on the capturing of a voltage sample through the sampling of pulse response waveforms. Fault discrimination is performed through a widow criterion in which threshold margins are set by a general consideration of ±5% tolerance. Minimum and maximum threshold margins are obtained by the worse-case boundary method, i.e. the smallest intervals of minimum and maximum tolerances obtained from all associated component variations.

Particular aspect of this test technique is the monitoring of only a single voltage sample $v_{md}$ at the effective point $p_{md}$. As will be seen later, the fault detection at the point $p_{md}$ offers the highest fault coverage, and covers all faults detected by those points $p_{mi}$ and $p_{mx}$. The point $p_{md}$ is located on the decreasing period determined by in resistors and capacitors, and therefore parametric variations cause changes in discharging period, resulting in effective fault detection. These characteristics are also common in most analog circuit types, depending on actual values of time constants. This test technique also affords simple test operations and compact circuit implementations. Two pulses can be generated simultaneously from the pulse generator for use as input pulse stimulus and a control signal in sampling operations. Consequently, this technique alleviates the need for fault-free bit streams, and synchronization processes in digital processing units.

## 3.4 Test System Implementations

### 3.4.1 Circuit Descriptions and Operations

Fig.3.8 shows the descriptive block diagram of the proposed BIST system architecture. The system comprises four major blocks, i.e. an analog CUT, a pulse generation circuit, a sample-and-hold (S/H) circuit with window comparator, and a test control circuit. First, the CUT is an analog circuit embedded in LSI system where primary input and output signals are $v_{PI}$ and $v_{PO}$, respectively. Multiplexer and demultiplexer are facilitated at input and output terminals of the CUT, respectively, in order to enable test accessibility through the mode selecting signal *MS*. Second, the pulse generation circuit provides two pulses $V_{P1}$ and $V_{P2}$, which are short rectangular pulses with different pulse widths. This pulse generation circuit exploits a clock signal *CK* as input, and its operation is enabled by the signal *Enb*. Third, the S/H with a window comparator characterizes the pulse response signal $V_{IR}$, and provides a Pass/Fail test output signal $V_{PF}$. This S/H operation is controlled by the enable signal *Enb* and the pulse $V_{P2}$. Last, the test control circuit provides the signals *CK*, *Enb*, and *MS* for controlling the test operations.

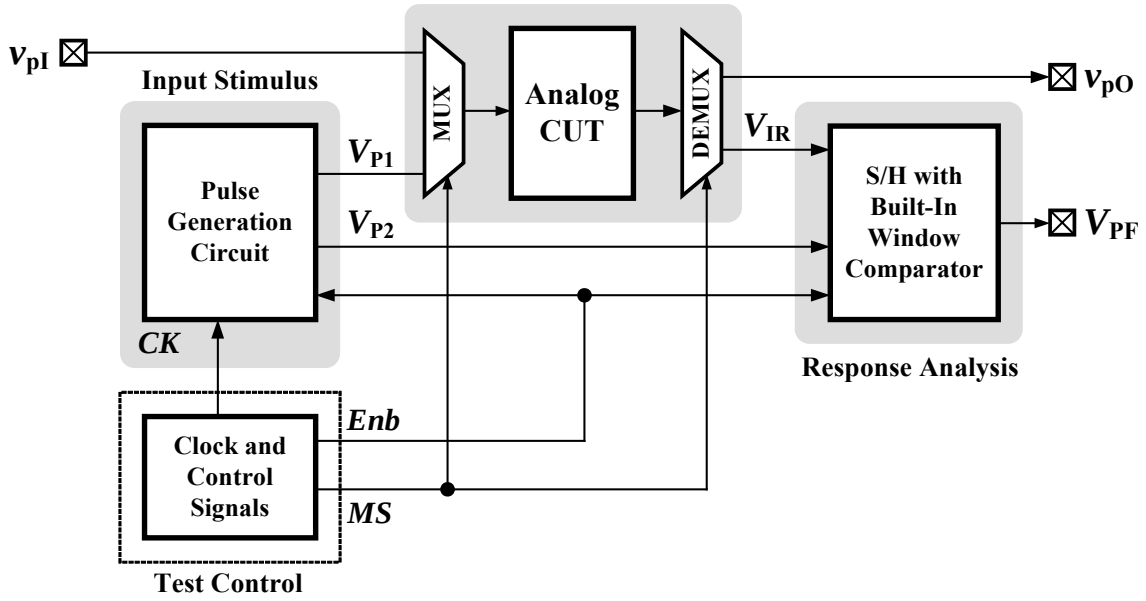



**Fig.3.8.** Descriptive block diagram of the BIST system architecture, showing test stimulus generator and pulse response analysis blocks.

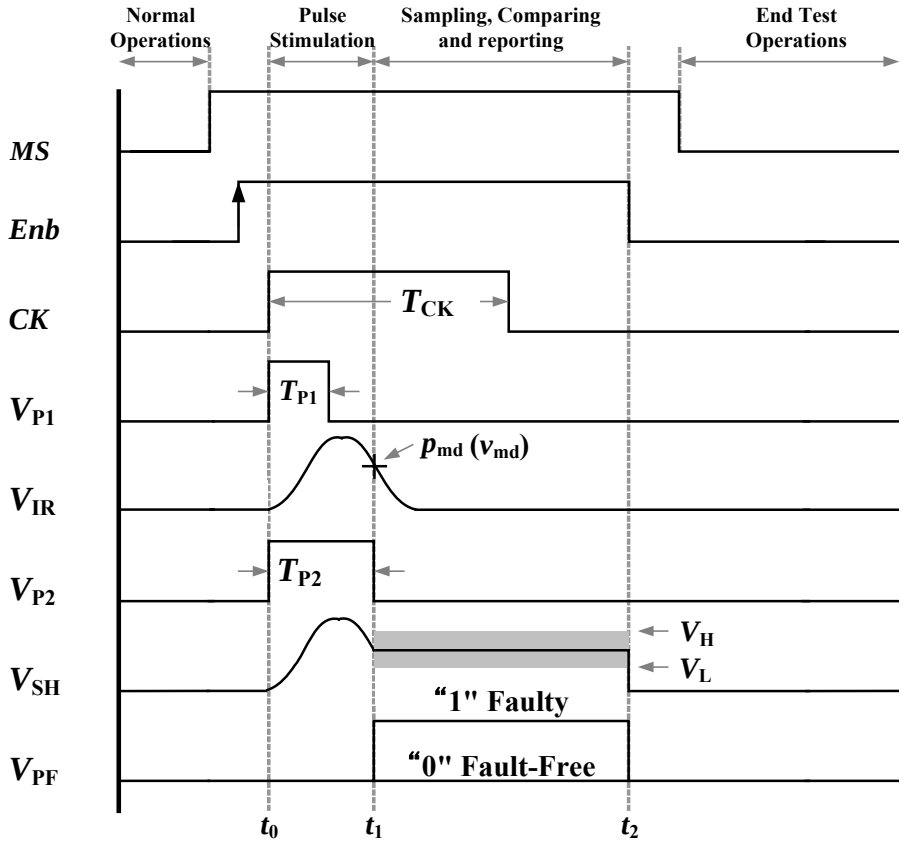



**Fig.3.9.** Timing waveforms of the BIST system operations in four phases.

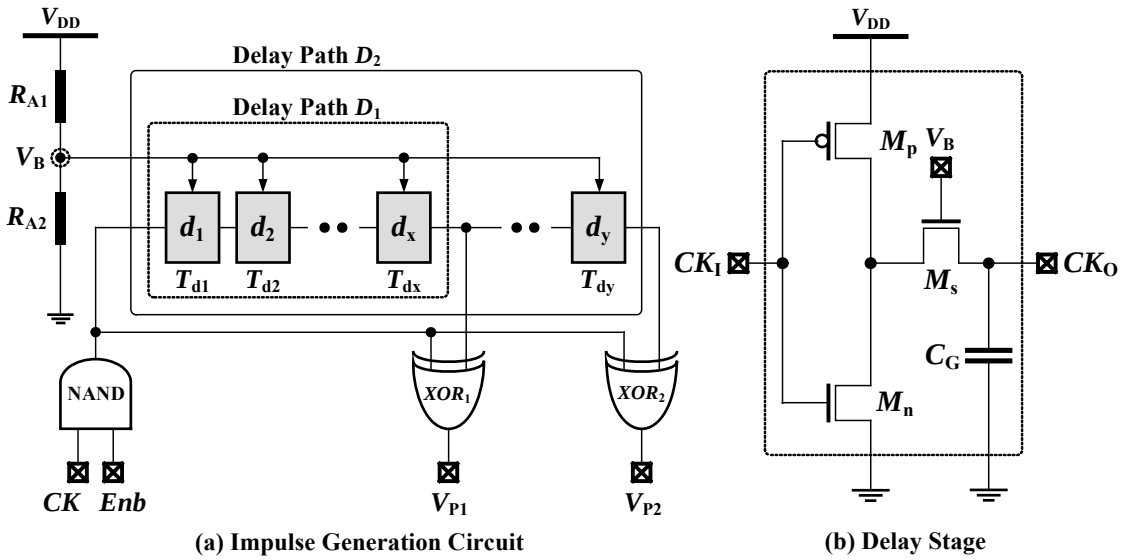



**Fig.3.10.** Circuit diagram of the pulse generation circuit.

Fig.3.9 shows the timing waveforms of BIST operations. This BIST system is capable of operating in two modes, i.e. normal and test modes. In normal mode, the signal *MS* is set to low level, allowing the CUT to operate in normal functions. In test mode, the signal *MS* is switched to high level, disconnecting the signals $v_{PI}$ and $v_{PO}$, and preparing the CUT to be ready for test operations. Test operations commence by switching the enabling signal *Enb* to high level. Initially, the clock *CK* rises to high state duration $T_{CK}$ at time $t_0$, allowing the pulse generator to produces two pulses $V_{P1}$ and $V_{P2}$ with pulse width $T_{P1}$ and $T_{P2}$, respectively. The pulse $V_{T1}$ stimulates the CUT directly in order to generate the pulse response $V_{IR}$. Subsequently, the pulse $V_{T2}$, which controls the sampling switch in S/H circuit, changes to low state in order to hold the voltage sample $V_{SH}$ at time $t_1$. Note that this sampled voltgae $V_{SH}$ is obtained for an effective voltage $v_{pd}$ at the point $p_{md}$ as described previously in Fig.3.7. Finally, the window comparator compares the voltage $V_{SH}$ against high and low threshold voltages $V_H$ and $V_L$, providing the test output voltage $V_{PF}$ during time $t_1$ and $t_2$.

### 3.4.2 Circuit Implementations

With reference to Fig.3.8, the circuit implementation involves the design of a pulse generator and a S/H circuit with window comparator. Since BIST system is an extra circuitry, all components were designed through the use of compact analog and digital circuits in order to achieve low complexity and adequate area overhead. Fig.3.10 shows the circuit diagram of the pulse generation circuit and delay element. The concept of the pulse generation is based on the phase detection through XOR gate, which compares phase

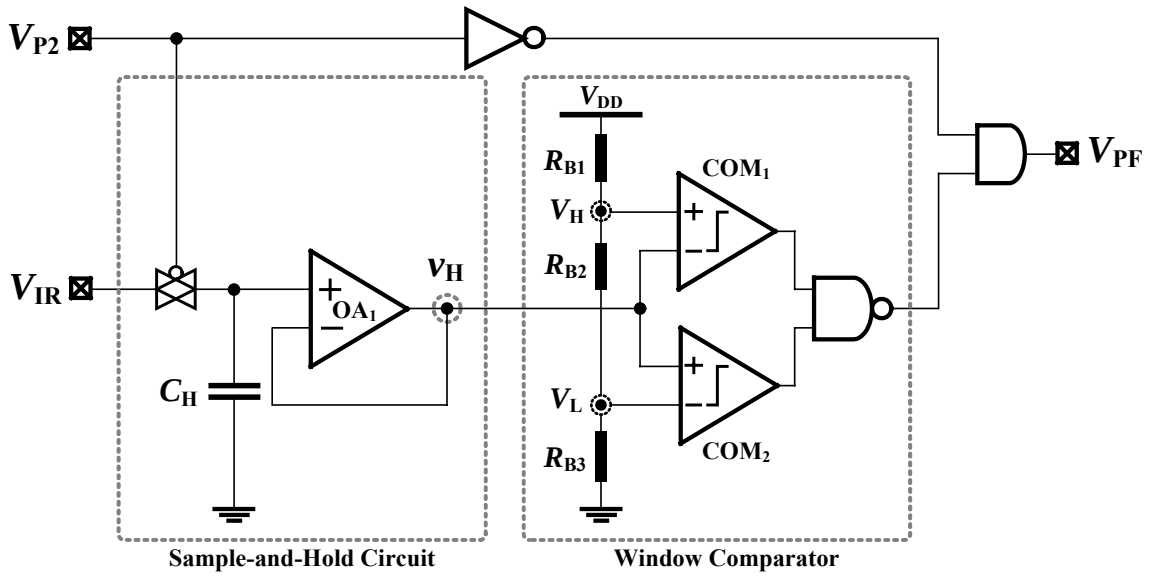



**Fig.3.11.** Circuit diagrams of the S/H with window comparator.

difference at low-to-high state transition time between the input clock and its delayed counter part. As shown in Fig.3.10 (a), the circuit consists of a NAND gate at the input for enabling pulse generation two XOR gates at the two outputs, and a chain of delay elements $d_1$ to $d_y$. These delay elements are identical, providing an equal value of delay time. The delay path $D_1$ delays the clock *CK* through $d_1$ to $d_x$, and therefore the pulse $V_{P1}$ obtained at the output of $XOR_1$ has a pulse width of $T_{P1}=T_{d1}+T_{d2}+\ldots+T_{dx}$. Similarly, the delay path $D_2$ delays the clock *CK* through $d_1$ to $d_y$, and the pulse $V_{P2}$ obtained at the output of $XOR_2$ has a pulse width of $T_{P2}=T_{d1}+T_{d2}+\ldots+T_{dy}$. The value of pulse width $T_{P2}$ determines the input clock frequency. Therefore, the clock *CK* can be set at the highest frequency of value $f_{CK} = 0.5T_{CK} = 0.5T_{P2}$ or at lower frequencies.

Despite the fact that the delay element can generally be implemented using simple inverters, the delay time of each inverter is relatively small. Consequently, the generation of a wide pulse width necessitates a vast number of delay stages, resulting in high power consumption and large area. As shown in Fig.3.10 (b), the delay element is implemented by an inverter formed by transistors $M_N$ and $M_P$, and an active resistor implemented by a transistor $M_S$, operating in linear region set by the bias voltage $V_B$. This voltage $V_B$ can simply be obtained on-chip using the voltage division through resistors $R_{A1}$ and $R_{A2}$ implemented by diode-connected NMOS transistors. Transistor $M_S$ develops an inherent low-pass filter, incorporating the gate capacitance $C_G$ of the next-stage inverter. This low-pass filter provides a large time constant due to a large value of active resistor, resulting in a large delay time. As a result of inserting $M_S$, each delay stage provide a sufficient delay time in the range of microsecond. The required number of delay elements for each particular CUT depends on the actual pulse width value that effectively produces a

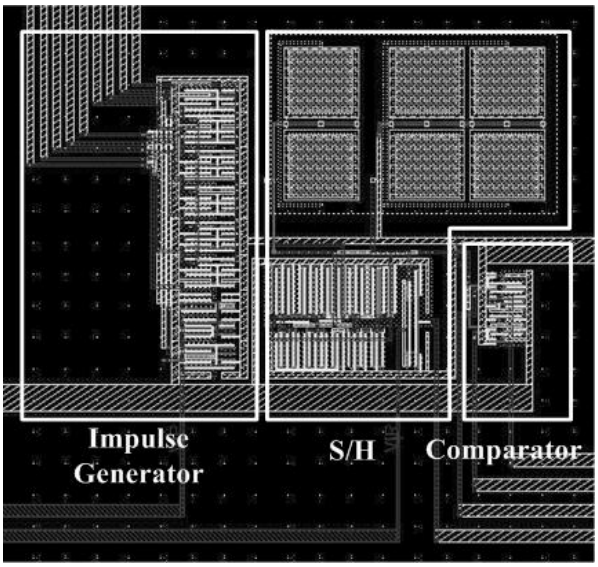



**Fig.3.12.** Layout diagram of the pulse generator and the S/H with window comparator.

proper output pulse shape investigated from pre-simulation process.Fig.3.11 shows circuit diagrams of the S/H with built-in window comparator. The S/H circuit was designed based on a unity-gain sampler, consisting of a sampling switch, a holding capacitor and a buffer amplifier. The sampling switch was implemented by a complementary switch in order to reduce an on-resistance and clock-feedthrough errors. The holding capacitor $C_H$ was implemented by available on-chip linear capacitors. The buffer amplifier was implemented by a two-stage operational amplifier with compensation. The voltage comparator comprises two simple differential amplifiers and a single NAND gate, reporting Pass/Fail test output $V_{PF}$. Fig.3.12 shows the layout diagram of the pulse generator and the S/H with window comparator.

## 3.5 Results and Discussions

### 3.5.1 Simulation Procedures and Preliminary Evaluations

Fig.3.13 shows the flow diagram of fault-free and faulty test simulation procedures. On the one hand, the fault-free simulations are performed for evaluating CUT specifications and determining some parameters required for BIST operations. The layout is initially designed, and extracted until the expected specifications are achieved. Random pulse width simulations are subsequently performed in order to obtain the optimal pulse widths $T_{P1}$ and $T_{P2}$ by investigating the proper pulse response shapes, and the fault-free voltage $V_{P3}$, representing an effective voltage $v_{pd}$ at the point $p_{md}$, is finally obtained. On the other hand, the fault injection simulations are performed for evaluating fault coverage

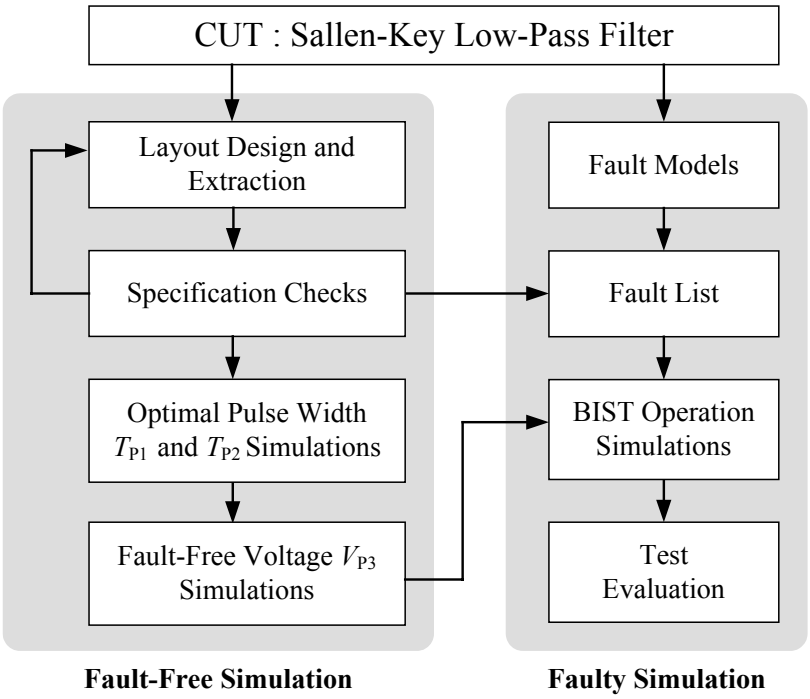
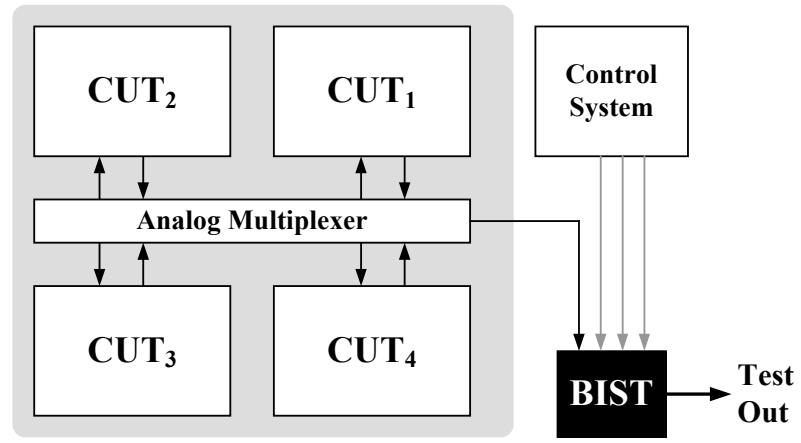


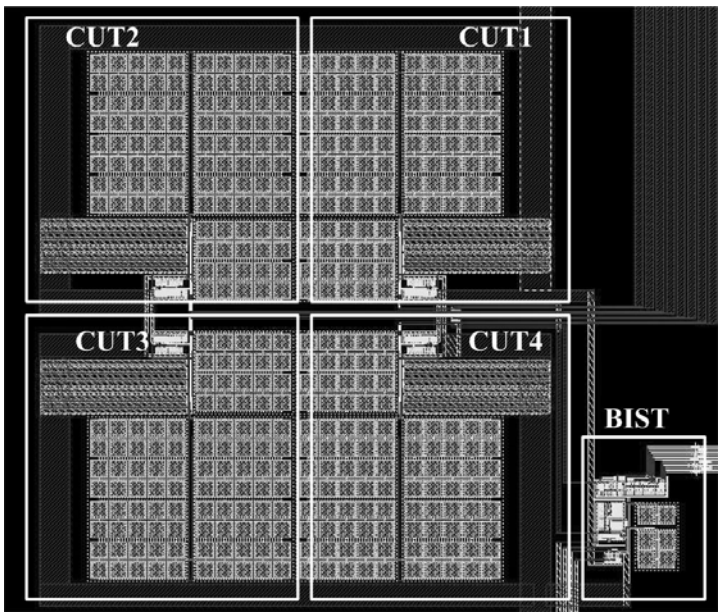

**Fig.3.13.** Flow diagrams of fault-free and faulty test simulation procedures.

that indicates the effectiveness of the test technique. The fault list, which covers all possible faults, is initially generated. Each fault is injected independently into the CUT at one time. The fault coverage is evaluated in percentage by the ratio of the number of detected faults detected to the number of all possible faults.

Fig.3.14 (a) and (b) respectively show the block diagram and the layout diagram of the Sallen-Key low-pass filter, which is designed corresponding to Fig.3.5. Four CUTs with partitioning multiplexers were included for demonstrating different fault types. The fault-free $CUT_1$ was employed as a reference. Other three $CUT_2$, $CUT_3$ and $CUT_4$ were employed as examples of faulty cases with GDS at $M_3$, open at $C_2$, and short between $R_1$ and $R_2$, respectively. In this design example, the BIST system occupied the area overhead of approximately 12%. These CUT exhibits a cut-off frequency of 500kHz. The resistors $R_1$ and $R_2$ were equally set at 80 kΩ, and the capacitors $C_1$ and $C_2$ were 8pF and 2pF, respectively. The pulse width $T_{P1}$ of the input pulse $V_{P1}$ was found at 0.5μs so that the resulting pulse response possesses a noticeably symmetric shape. In addition, the pulse width $T_{P2}$ of the pulse $V_{P2}$ was found at 1μs. The voltage sample $V_{SH}$ was measured at 0.7V. Catastrophic fault injections were performed using the resistor insertion technique; shorts were modeled by inserting a small 1-Ω resistor in parallel between each pair of component terminals while opens were modeled by inserting a large 10-MΩ resistor in series to the components. Parametric fault injections were performed through the variation of 10% in resistors and capacitors. As a result, the total number of 67 faults was investigated, including 20 faults at the RC network and 47 faults at the buffer.




(a)




(b)

**Fig.3.14.** Architecture of the partitioned CUTs with BIST circuit; (a) Block diagram, (b) Layout diagram.

Prior to fault injection procedures, the four identical CUTs were in fault-free condition and circuit performance can be ensured and investigated through switch arrangements. Since each CUT exhibits a $2^{nd}$-order filter, the cascade connections of more than two CUTs yield $4^{th}$-oder, $6^{th}$-order and $8^{th}$-order filter transfer functions. Fig. 3.15 shows the frequency response of CUTs. The actual values of DC gain and cutoff frequency were measured at 0dB and approximately 500 kHz, respectively. It is seen in Fig. 3.15 that all the CUT were operating correctly and ready for pulse stimulation and fault injections. Fig.3.16 shows the impulse responses to 5-μs input impulse test stimuli of four filter orders. It is shown in Fig.3.16 that the $2^{nd}$–order filter exhibit relatively high impulse peak with low propagation time, whereas $4^{th}$–order, $6^{th}$-order and $8^{th}$–order filters show evident of

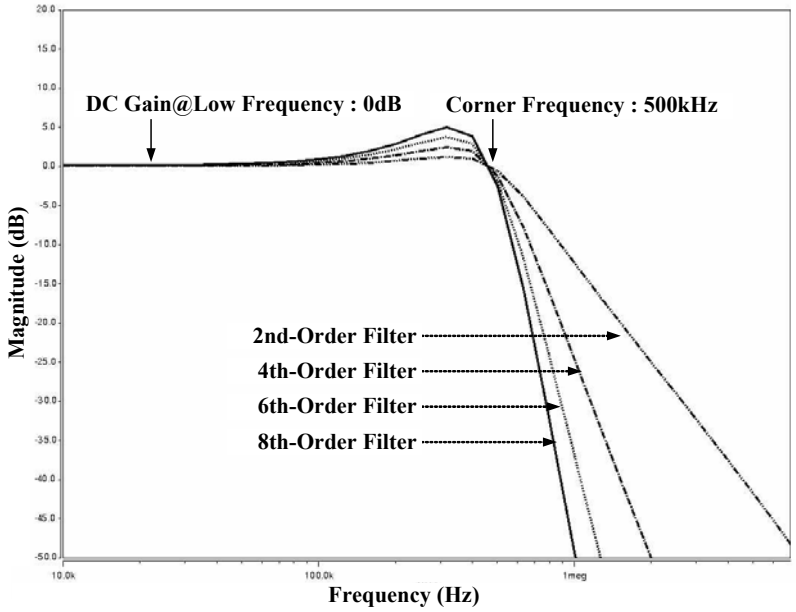



**Fig.3.15.** Frequency response of CUTs at different orders.

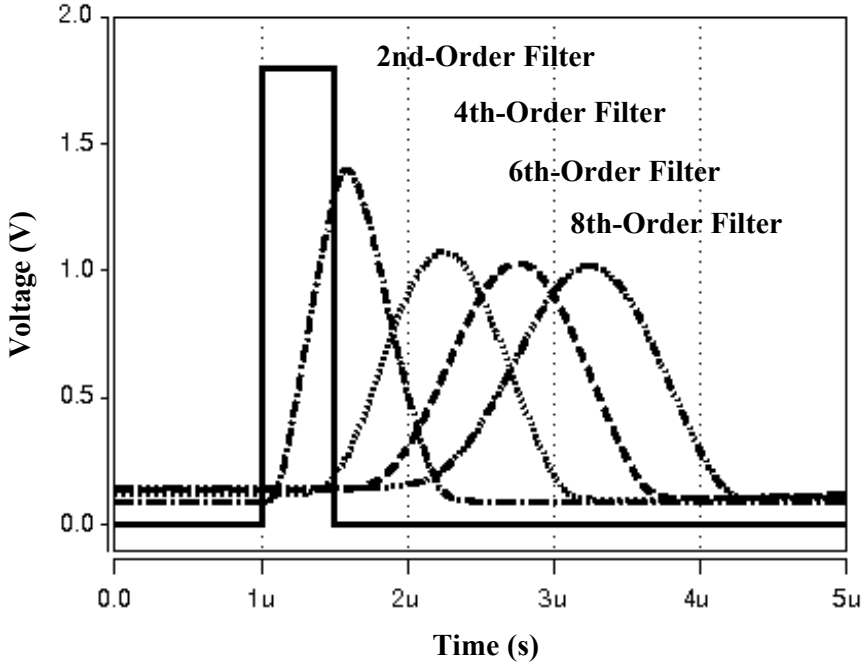



**Fig.3.16.** Pulse response of CUTs at different orders.

low peak values with longer offset times. Therefore, four identical building blocks of the CUT were implemented by the 2nd-order Sallen-Key lowpass filters. As depicted in Fig. 3.16, the divided CUT is controlled through a multiplexer. Portioning the complicated CUTs into sub-blocks assists the direct accessibility to each building block for high fault coverage and the simplicity of fault location diagnosis.

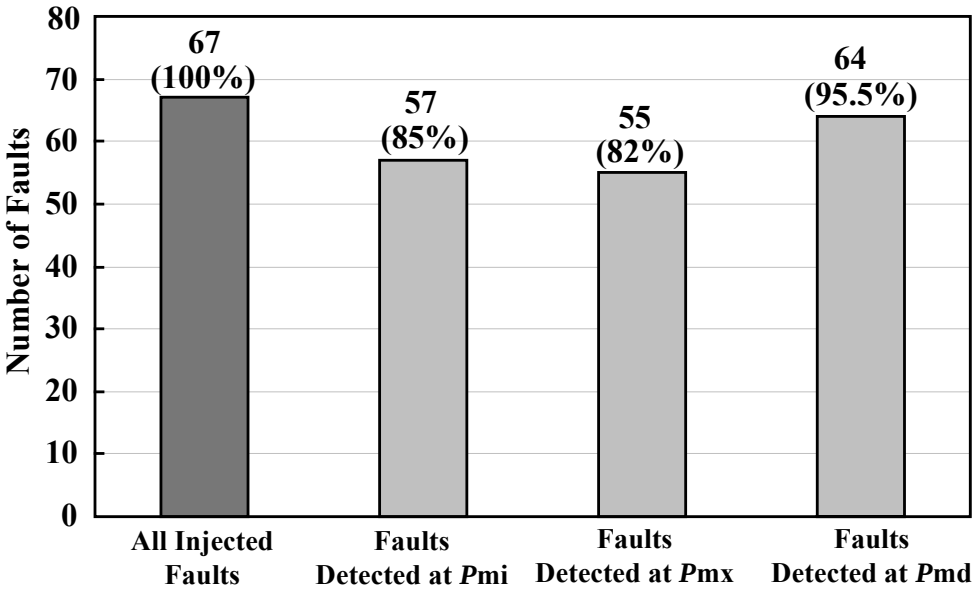



**Fig.3.17.** Bar graphs of the numbers of injected and detected faults at three investigating points $p_{mi}$, $p_{mx}$, and $p_{md}$.

The post-layout fault injections were simulated based on the procedures described in Fig.3.13 in order to investigate the fault coverage and the effectiveness of voltage monitoring at the point $p_{md}$. Fig.3.17 shows the bar graphs of numbers of injected and detected faults at the three points. With the total injected faults of 67 faults, fault detection at points $p_{mi}$, $p_{mx}$, and $p_{md}$ reveal the fault coverage of 85%, 82% and 95.5%, respectively. Consequently, the concept of realizing the approximate investigation at the three points is acceptable for fault detection as the fault coverage were relatively high, i.e. greater than 80%. Moreover, fault detection at only the point $p_{md}$ offers the maximum fault coverage of 95.5% and covered all faults detected at points $p_{mi}$ and $p_{mx}$. As expected, the proposed technique through the monitoring of only a single effective voltage $v_{pd}$ at the point $p_{md}$ is effective and suitable for low-cost BIST system.

### 3.5.2 Experimental Results

The experimental results were carried out through the fabricated chip model VDEC-PC459-BU7078-BC. Fig. 3.18 (a) and (b) show the photographs of the top-cell layout and the fabricated chip, respectively. It should be noted that this chip also contains other digital circuits as for academic proposes. Fig.3.19 shows the chip microphotograph of the fabricated BIST system where four CUTs with partitioning multiplexers were included for demonstrating different fault types. Fig.3.20 shows the diagram of experimental setup with the power supply of at 1.8V. Fig.3.21 shows the photograph of experimental setup.

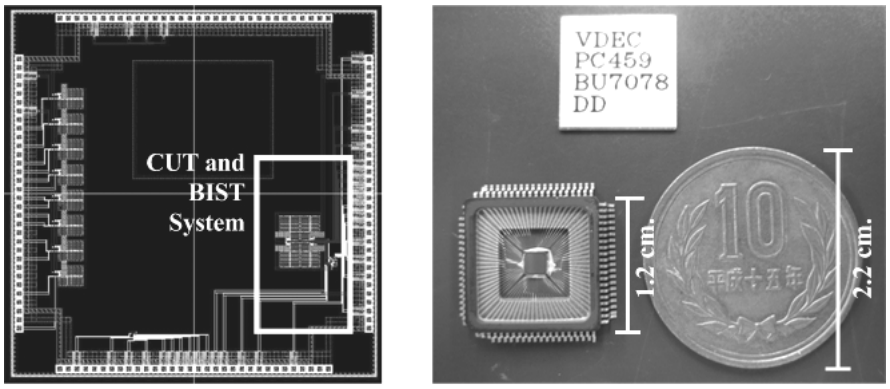



**Fig.3.18.** Photographs of (a) the top-cell layout design and (b) the fabricated chip.

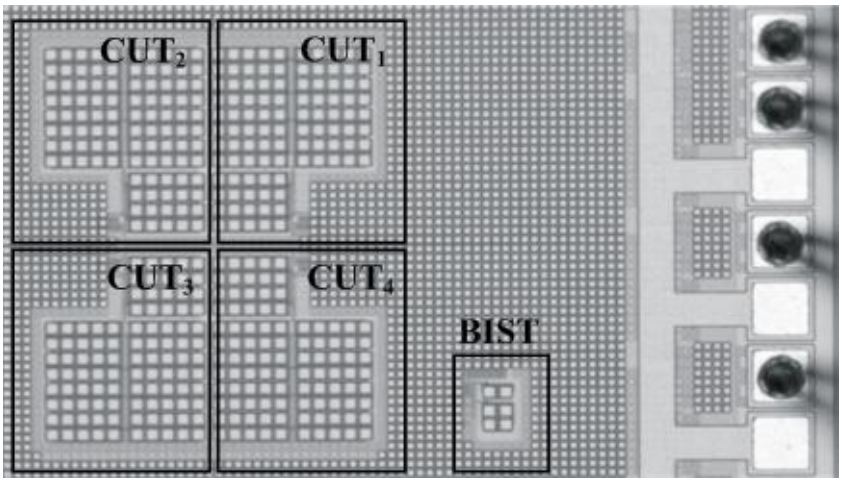



**Fig.3.19.** Chip microphotograph of the fabricated CUTs and BIST system.

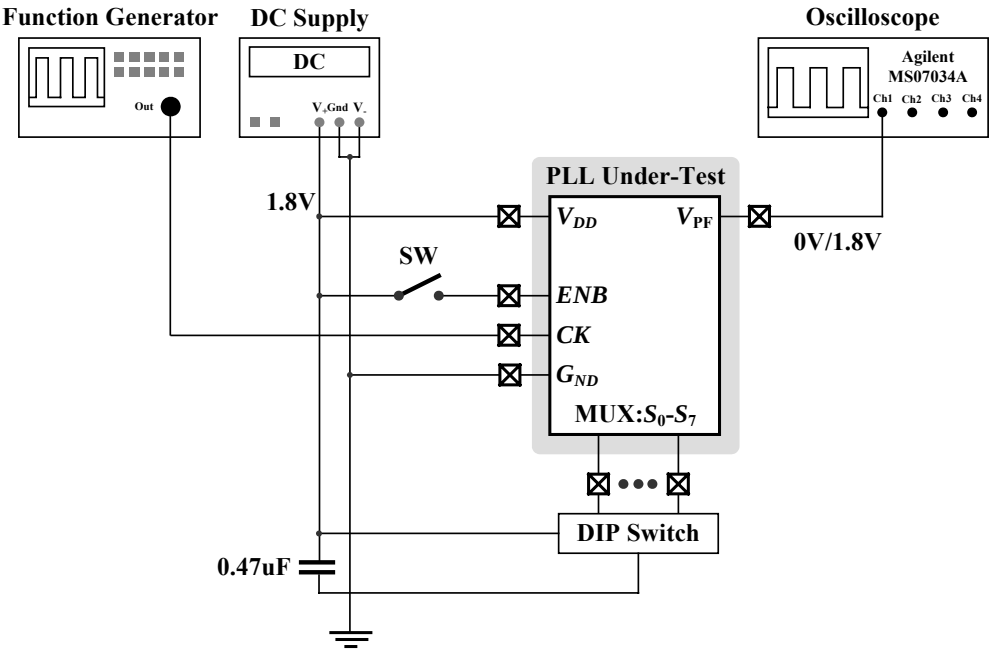



**Fig.3.20.** Diagram of experimental setup.

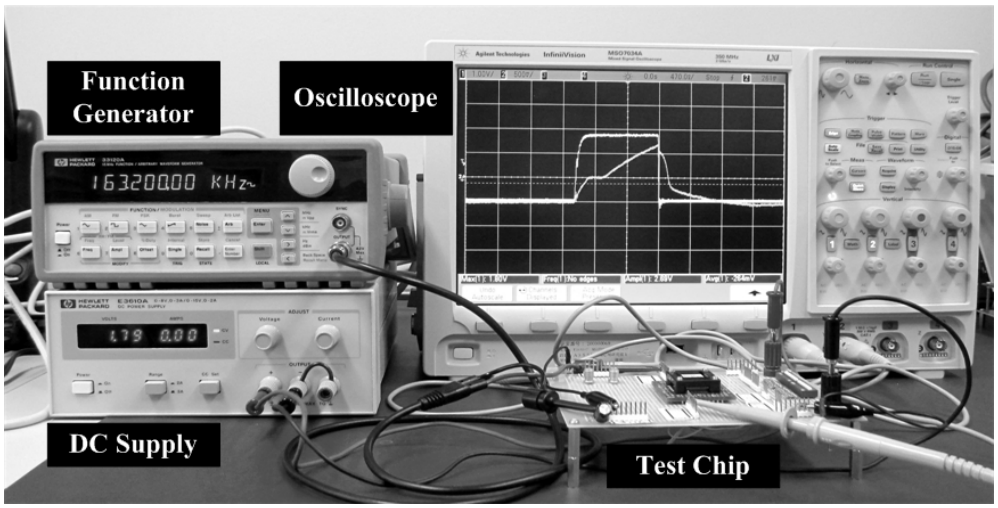



**Fig.3.21.** A photograph of experimental setup.

Initially, the performance degradation caused by additional facilities from BIST system on the existing CUT was investigated. Fig.3.22 shows the Bode magnitude plots of the measured low-pass characteristics of CUTs with and without BIST system, and corresponding magnitude errors. The data of the CUT with BIST were obtained from $CUT_1$, while the data of the CUT without BIST were obtained from a separately redundant filter. Both CUTs with and without BIST offer expected second-order low-pass characteristics. The magnitude errors defined as the difference between the measured magnitudes of CUT with and without BIST system at each particular frequency were relatively low of less than 0.6 dB. These small errors may caused by some parasitic capacitances and resistances in the partitioning multiplexers. The BIST was disconnected in the normal operation mode, and hence no loading effects degrade the performance of the CUTs.

Pulse responses were investigated through externally supplied pulses where the input pulse width was set at 0.5μs. Fig.3.23 show four cases of pulse responses where horizontal and vertical axes are 300ns/Div. and 500mV/Div., respectively. The response of the $CUT_1$ yields a reference voltage of 0.7V. The DGS at $M_3$ caused a stuck-at-$V_{DD}$ response in which the sampled voltage was measured at 1.76V. The $CUT_3$ and $CUT_4$ caused changes in response shapes where the sampled voltages were measured at 0.4V and 0.3V, respectively. As expected, three faulty CUTs show some changes in response waveforms, resulting visibly tremendous deviations in sample voltage values. The BIST operations for the four CUTs were performed completely on-chip. The enable signal *Enb* and the clock *CK* were applied to the chip as BIST inputs, and the test output $V_{PF}$ was observed where low (0) and high (1) states indicate fault-free and faulty status, respectively. Table 3.2 summarizes parameter settings for BIST operations. The bias voltage $V_B$ was set at 0.34V so that each delay cell has a delay time of 0.25V. Therefore, two delay cells were implemented for setting $T_{P1}$ at 0.5μs and four delay cells were

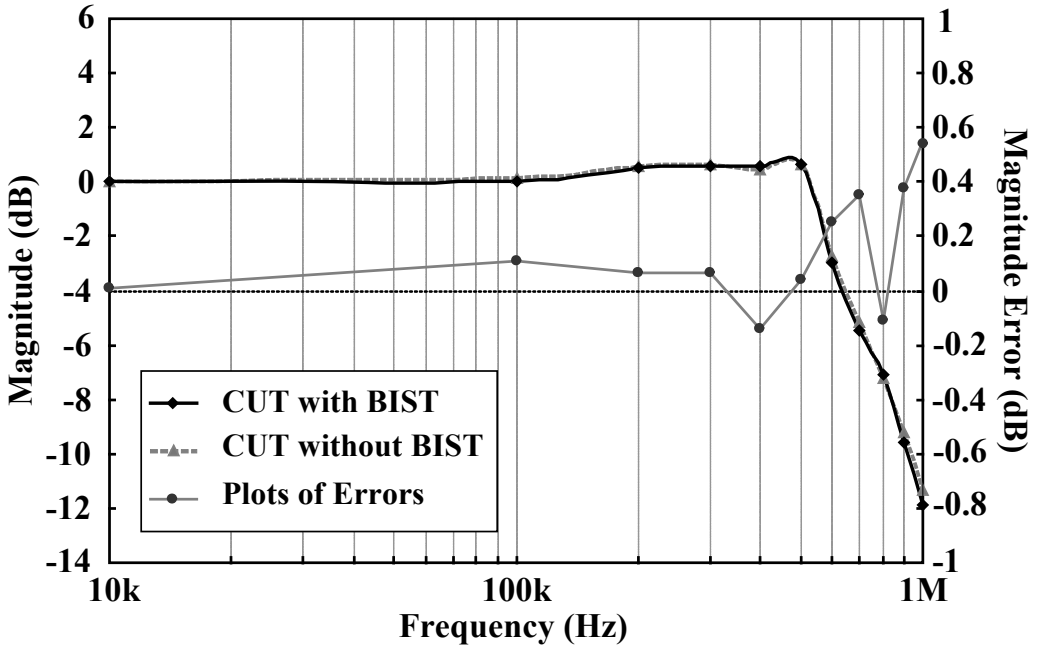



**Fig.3.22.** Bode magnitude plots of measured low-pass characteristics of CUTs with and without BIST system, and magnitude errors.

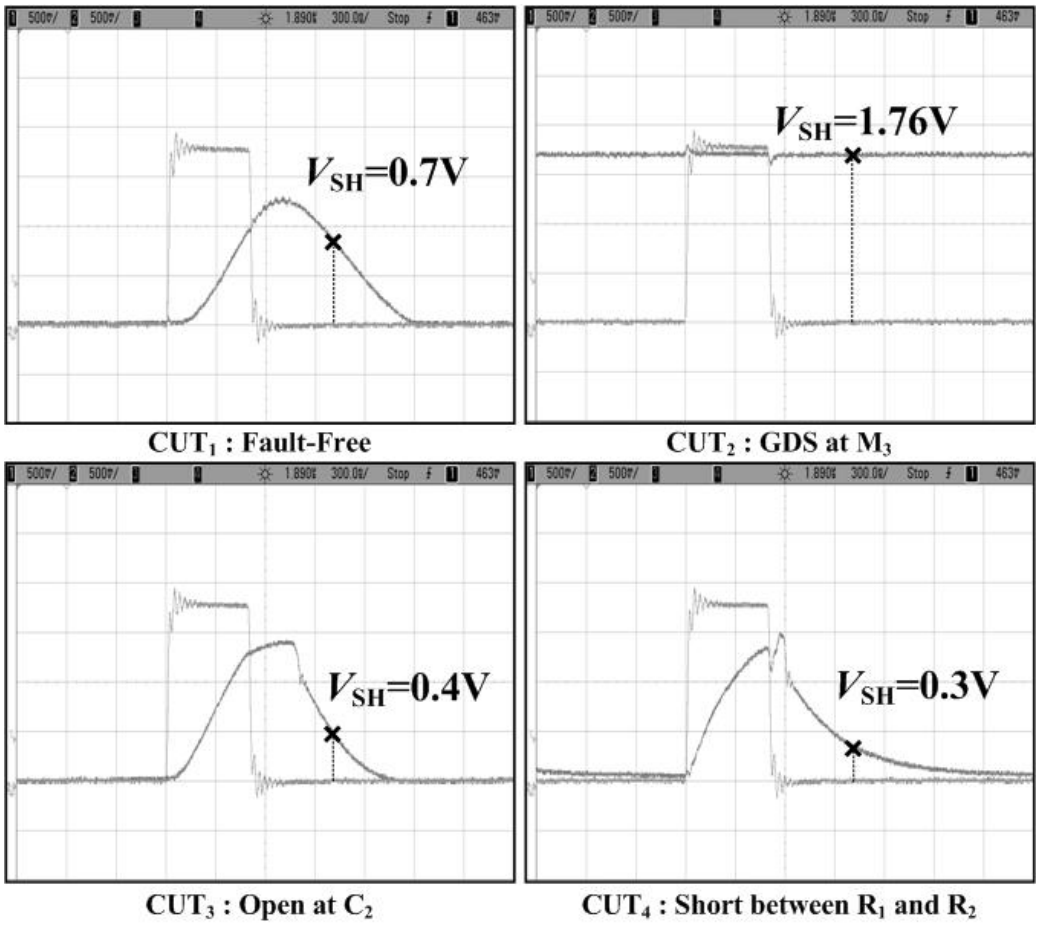



**Fig.3.23.** Measured response waveforms of pulse inputs in four demonstrating CUTs.

**Table 3.2.** Summary of parameter settings in BIST operations.

| Parameters | Values | Units |
|---|---|---|
| Bias Voltage $V_B$ | 0.34 | V |
| Frequency of $CK$ | 300 | kHz |
| Pulse Width $T_{P1}$ | 0.5 | μs |
| Pulse Width $T_{P2}$ | 1 | μs |
| Reference Fault-Free Voltage $V_{SH}$ | 0.7 | V |
| + 5% Tolerance $V_H$ | 0.735 | V |
| - 5% Tolerance $V_L$ | 0.665 | V |

**Table 3.3.** Summary of the measured fault detection outputs.

| CUTs | Fault Types | Test Outputs | Detected |
|---|---|---|---|
| $CUT_1$ | Fault-Free | 0 | No |
| $CUT_2$ | GDS at $M_3$ | 1 | Yes |
| $CUT_3$ | Open at $C_2$ | 1 | Yes |
| $CUT_4$ | Short between $R_1$ and $R_2$ | 1 | Yes |

implemented for setting $T_{P2}$ at 1μs. The frequency of the clock $CK$ was optimally set at 300kHz. With reference to the fault-free voltage 0.7V obtained from $CUT_1$ in Fig.3.23, $V_H$ and $V_L$ based on ±5% tolerance in the window comparator were set to 0.735V and 0.665V, respectively. As a result, Table 3.3 summarizes the measured fault detection outputs. The fault free $CUT_1$ provides a low state signal, indicating a fault-free CUT. Other three CUTs provides high state signals, indicating all CUTs are defective. It can be considered from Table 3.3 that the BIST operated effectively as expected.

Finally, BIST features of this work and other related pulse response based BIST techniques were compared. Table 3.4 compares the proposed BIST technique to those of existing BIST techniques. In an attempt to enable fair comparison, three particular references that previously proposed BIST techniques based on pulse stimulation and measurement are considered. First, this work offers low implementation cost through the use of a simple delay cell based pulse generator. Neither digital LFSR, which is commonly used in digital testing, nor microcontroller is required. Furthermore, the proposed BIST technique enables the use of a simple S/H with window comparators for fault detection process while other techniques necessitate complex devices such as A/D converter, microcontroller, and DSP with specific algorithms for fault signature compaction or cross-correlation analysis. Second, this work uses low testing time within a single duration, and the fault detection procedure performs instantaneously during sample and hold operations, generating the Pass/Fail output in digital forms. Other techniques employ a

**Table 3.4.** Comparisons of this work and other four related BIST techniques; ×= not reported, SH=Short Fault, OP =Open Fault.

| Characteristics | BIST Techniques | | | |
|---|---|---|---|---|
| | ***Marzocca and Corsi*** | ***Variyam and Chatterjeee*** | ***Czaja*** | **This work** |
| **Technology** | - | CMOS | Discrete Components | CMOS 0.18-um |
| **Results** | Simulation | Simulation | Experiment | Simulation & Experiment |
| **CUTs** | Butterworth Filter | Sallen-Key Filter | Sallen-Key Filter | Sallen-Key Filter |
| **Input Types** | Pseudo-Random Pulses | Random-Width Pulse Trains | Multiple Pulses | Single Pulse |
| **Fault Analysis** | Cross Correlation | Signature Compaction | Algorithms in Microcontroller | Sampling and Comparison |
| **Pulse Generation** | × | Digital LFSR | Microcontroller | Delay Cell |
| **Test outputs** | × | × | 1 Bit | 1 Bit |
| **Area Overhead** | × | 47 % | × | 12 % |
| **Fault Models** | × | × | × | SH: 1Ω, OP: 10MΩ |
| **Fault Coverage** | × | × | × | 95.5%: 4 Examples |

random width pulse sequence or a multiple pulse train as input stimuli. Therefore, the fault detection procedures require time for processing long pulse sequence responses in digital domain through the use of digital counters or microcontroller. Last, the fault coverage of this work is relatively high as demonstrated for the testing of Sallen-Key low-pass filter. Noted that fault coverage depends on test set-up environments such as CUT specifications and tolerance conditions.

## 3.6 Conclusions

This chapter has presented the BIST technique for analog integrated circuit using concurrent pulse stimulation and response sampling. The proposed BIST technique employed a single pulse input stimulus and a single effective voltage sample on a pulse response waveform for fault discriminations. Simple BIST implementations and operations have achieved by a concurrent pulse generation and sample-and-hold operation with low area overhead and low power consumption. Demonstrations of BIST system for

Sallen-Key low-pass filter with a cut-off frequency of 500kHz, containing the total number of 67 faults, show high percentage of fault coverage at 95.5%. Experimental results show an area overhead of approximately 12% and low degradation on existing CUT performances. The proposed technique is relatively compact by eliminating the need for fault-free bit streams, high-precision on-chip analog stimuli, and characterizations and synchronization processes. In conclusion, the proposed pulse response based-BIST technique has offered a potential alternative to low-cost and high-speed BIST system for the pre-screening test process for defective analog integrated circuits in mixed-signal systems.

# Chapter 4

## BIST Technique using Fault Signature Characterization and the Extension of IEEE 1149.4 Standard

## 4.1 Introduction

This chapter presents the BIST technique using a fault signature characterization and the extension of IEEE 1149.4 standard. This chapter begins by the reviews on IEEE 1149.4 Standard and its related test techniques. The testing technique is a sinusoidal fault signature characterization and the realization of two level crossing voltages. The test system is an extension of the IEEE 1149.4 standard through the modification of an analog boundary module, affording functionalities for both on-chip testing capability and accessibility to internal components for off-chip testing purposes. A demonstrating CUT is a $4^{th}$-order $G_m$-$C$ low-pass filter. Both catastrophic and parametric faults are potentially detectable at the minimum parameter variation of 0.5%. The fault coverage associated with CMOS transconductance operational amplifiers and capacitors are approximately 94% and 100%, respectively.

## 4.2 Reviews on IEEE 1149.4 Standard and Previous IEEE 1149.4 Standard Based BIST Techniques

### 4.2.1. The 1149.4 Mixed-Signal Test Bus Standard

The IEEE 1149.4 mixed-signal test bus standard has been developed for testability enhancements of analog mixed-signal circuits by facilitating two analog access ports and on-chip test buses. Standardizing tests using the IEEE 1149.4 standard resolve the limitation of physical access to internal test points, and interconnecting tests are also applicable. Fig. 4.1 shows the block diagram of the simplified architecture of the IEEE 1149.4 standard. This architecture affords internal components for testing in both digital and analog circuits, comprising a digital boundary module (DBM), analog boundary module (ABM), test bus interface circuit (TBIC), and control circuitries. As illustrated in

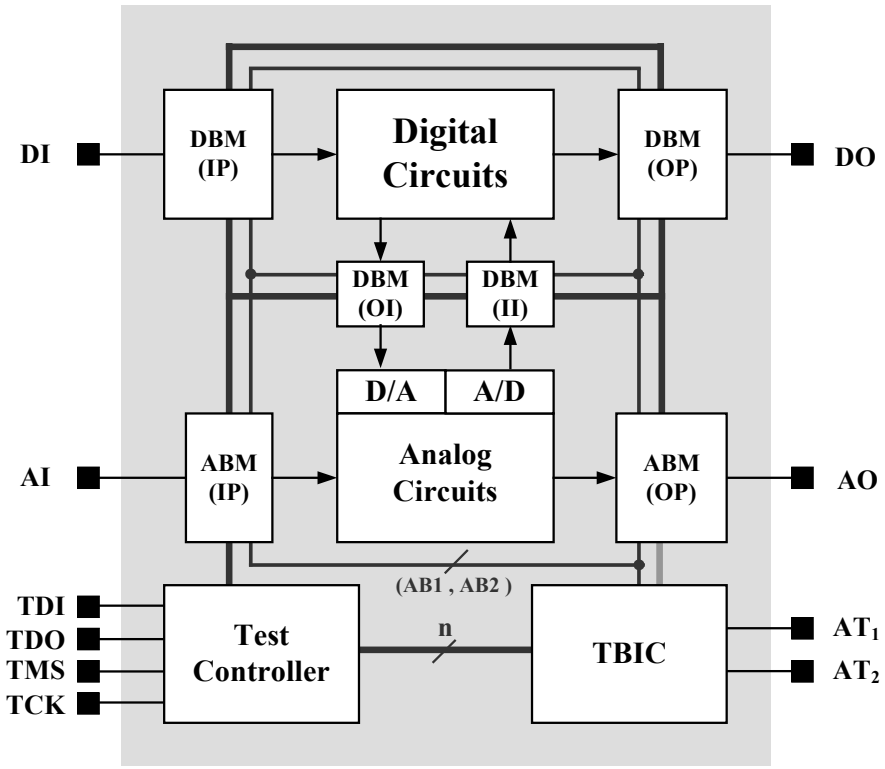



**Fig. 4.1.** Block diagram of the architecture of IEEE 1149.4 mixed-signal test bust standard.

Fig.4.1, the DBMs scan targeting digital circuits, and shift test data through a serial interface. These DBMs are generally enclosed in digital core circuits and located at input pin (IP), output pin (OP), input and output interfaces to D/A and A/D converters (OI and II). The ABMs provide internal bus connections to each particular CUT. The TBIC conveys input and output analog test signals to ABMs via two analog internal buses (AB1 and AB2), and offers functions for interconnect testing. The control circuitries, consisting of shift registers and decoding logics, control the operation of overall test systems through the four major control signals: test-data-in (TDI), test-data-out (TDO), test-clock (TCK), and test-mode-select (TMS).

Fig. 4.2 shows the circuit configurations of two major blocks, including (a) ABM and (b) TBIC, in the IEEE 1149.4 standard, particularly for testing in analog mixed-signal systems. As shown in Fig. 4.2(a), the ABM, comprising a voltage comparator (1-bit digitizer) and six switches. The switch $S_D$ is used for disconnecting the ABM from CUT. The switches $S_{B1}$ and $S_{B2}$ control the connection to the internal analog test buses AB1 and AB2, respectively. The switches $S_H$ and $S_L$ are associated with connections to the voltages $V_H$ and $V_L$, which perform as standard DC voltage of logical values. This ABM is capable of two modes of operations, i.e. digital and analog modes. In digital mode, the input is initially digitized by the comparator, and then preloaded in control registers (CRs). The output captured from the comparator is re-loaded into CRs and the decoding logic decides

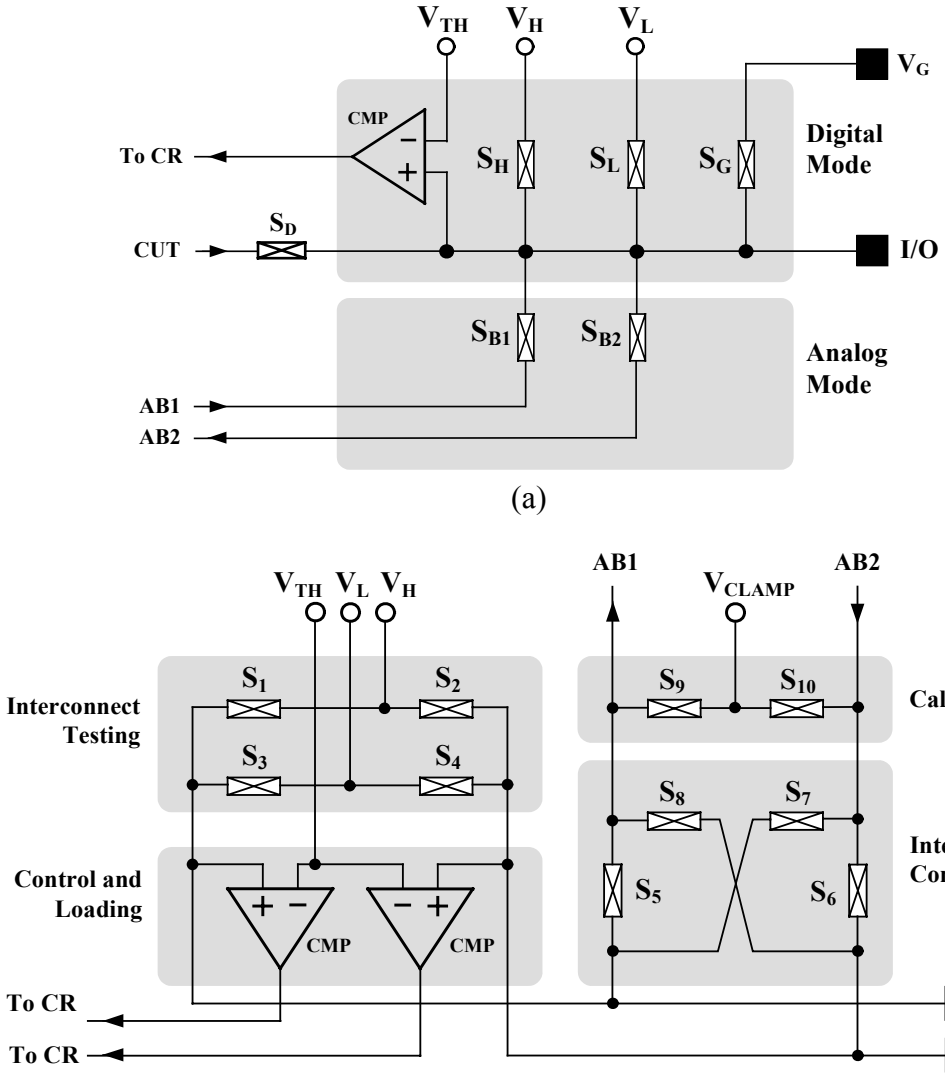



**Fig. 4.2.** Circuit configurations of two major blocks in the IEEE 1149.4 standard for test accessibility to analog mixed-signal systems; (a) ABM, (b) TBIC.

output logics for reporting the test results. In analog mode, an input signal stimulus is sourced via port AT1 and an output response is provided at port AT2. In addition, the output response also forms a current return to the ground voltage $V_G$ through the on-resistance of the switch $S_G$. Fault detection of analog response is accomplished externally through measurement devices such as interfacing testing chips or ATEs. As shown in Fig. 4.2(b), the TBIC provides interconnect testing between chips by means of the switches $S_1$ to $S_4$, associating with voltages $V_H$ and $V_L$. Selection of internal bus connections of each analog CUT is accomplished through the switches $S_5$ to $S_8$. Calibration of internal bus voltages is also available through the clamp voltage $V_{CLAMP}$, connecting to the switches $S_9$ and $S_{10}$. Additionally, two comparators are employed for controlling the switch network, and loading signals to the scan paths.

**Table 4.1.** Summary of related 1149.4 standard-based test techniques.

| Authors | Years | 1149.4 Standard-Based Test Techniques |
|---|---|---|
| (a) *Kac and Novak* | 2003 | Extending operating mode of ABM in 1149.4 standard |
| (b) *Gorodetsky* | 2005 | Bridge-for-Testability of ABM in 1149.4 standard |
| (c) *Syri* | 2005 | RF interface architecture of ABM in 1149.4 standard |

### 4.2.2. Reviews on IEEE 1149.4 Standard-Based BIST Techniques

In regards to the architecture of IEEE 1149.4 mixed-signal test bust standard described in Figs. 4.1 and 4.2, Table 4.1 summarizes related 1149.4 standard based test techniques, involving three techniques that have previously been proposed by *Kac and Novak* (2003), *Gorodetsky* (2005), and *Syri* (2005).

As shown in Table 4.1(a), *Kac and Novak* (2003) proposed the extension of operating mode of ABM in 1149.4 standard. According to the typical IEEE 1149.4 shown in Fig. 4.2(a), the analog INTEST instruction sustains external circuitry connected to the analog core, which requires controlling the external onboard circuitry to provide appropriate operating conditions or to ensure that inputs are quiescent. To circumvent this limitation in the original ABM structure, Fig. 4.3 shows the two additional switches $S_1$_Int and $S_2$_Int, which are connected to $AB_1$ and bypass the core disconnect switch $S_D$, respectively. This modification allows circuit controller to open $S_D$ during the INTEST instruction, eliminating the need to control external circuitry and simplifying test development. For this extended INTEST procedures on a multiple input analog core, this approach is, however, limited since the analog stimulus generator can drive only a single input through the analog test bus. The switch $S_G$_Int, which connects the remaining core inputs to the known reference voltage, $V_G$, is therefore added. The original and modified ABM architectures suit different types of test strategies. This modified ABM structure allows system-wide functional reconfiguration, which is useful in analog functional tests.

As shown in Table 4.1(b), *Gorodetsky* (2005) alternatively proposed the non-invasive technique called Bridge-for-Testability that exploits the 1149.4 test access standards for contactless in-circuit continuous monitoring and testing of nodes in densely populated mixed-signal circuit boards with limited nodal access. Fig. 4.4 shows the system architecture of Bridge for Testability of ABM in 1149.4 standard. It can be seen in Fig. 4.4 that two additional multiplexers and control tap are introduced. These circuits are introduced in order to enable more than two input types, i.e. *B*, *C*, *D*, and *E*, while two ABM are exploited. Noted that the input *A* is a common digital test signal. Different types of those four inputs are described as follows. Firstly, the *B*-type digital functional pin is

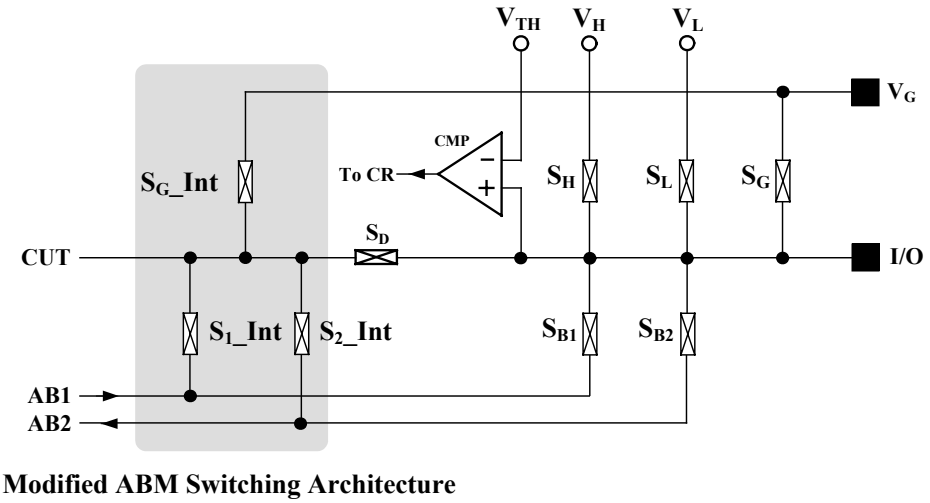



**Fig. 4.3.** Circuit configurations of the modified ABM (*Kac and Novak*, 2003).

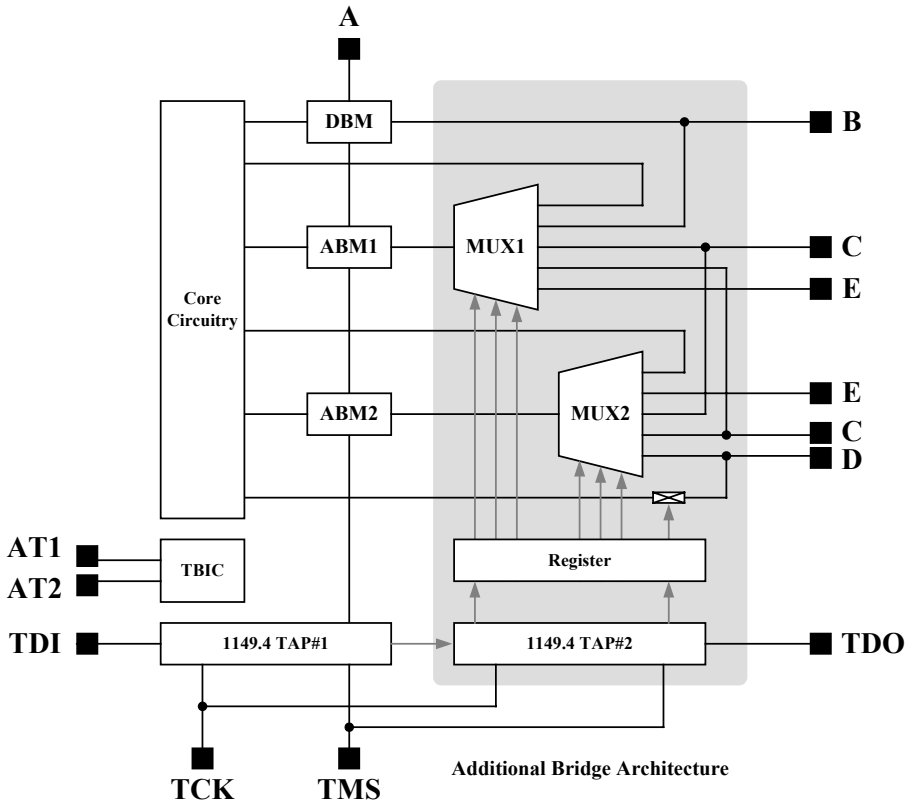



**Fig. 4.4.** Architecture of Bridge for Testability of ABM (*Gorodetsky*, 2005).

connected to MUX1 and also to the dedicated digital module DBM. This B-type pin is isolated from the core by DBM while being connected to MUX1, becoming to be the "1149.4- probable" pin. Secondly, the *C*-type analog functional pin has full 1149.4 support through one or both multiplexers. This pin is usable for both the in-circuit PCB level test purposes and for the connection to the core via ABM1 and ABM2 when the IC is in test mode. Thirdly, The *D*-type mixed-signal functional pin is connected to analog multiplexers and to the dedicated analog switches. When the IC is in test mode, the *D*-type pin is

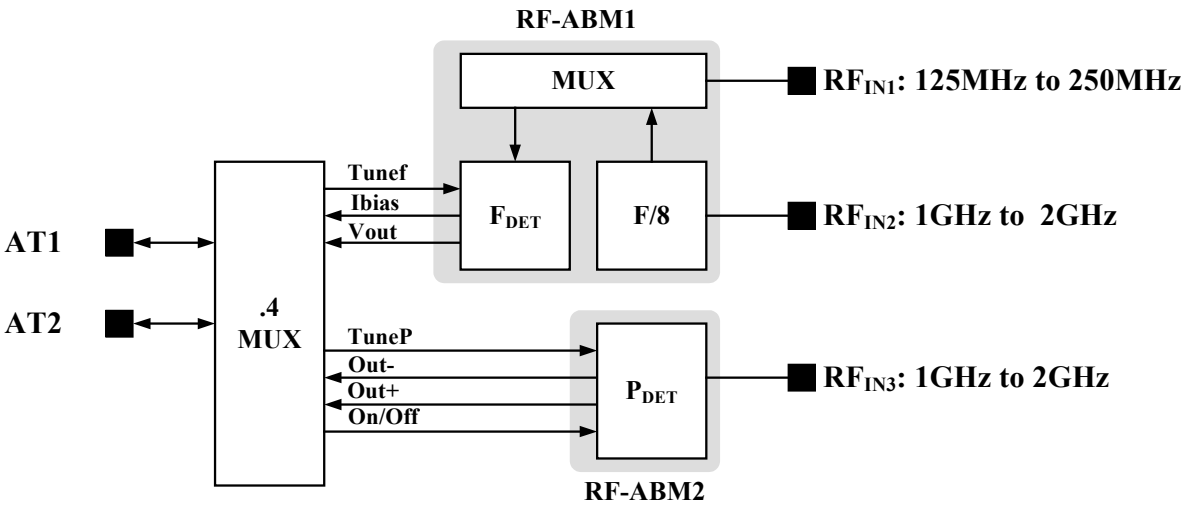



**Fig. 4.5.** Architecture of the RF interface in ABM in 1149.4 Standard based (*Syriy*, 2005).

connected to the core via its switch, which is closed and disconnected from ABM1 and ABM2, according to the proper neutral multiplexer address. Fourthly, the *E*-type mixed-signal non-functional external pin is not 1149.4-compliant, and has no functional usage when the IC is in test mode. These in-circuit prober/injector pins are connected to multiplexers, becoming to be the "1149.4-probeable" pin and employing for the in-circuit PCB level test purposes. Lastly, the *F*-type non-functional internal I/O pin is also not 1149.4-compliant. These in-circuit prober/injector pins are connected to multiplexers, also becoming to be the "1149.4-probeable" pin and employing for the in-circuit PCB level test.

As shown in Table 4.1(c), *Syri* (2005) proposed the 1149.4 standard-based ABM architecture for high-frequency signal interface since the IEEE 1149.4 standard is mainly targeted for low frequency testing. Fig. 4.5 shows the system architecture of RF interface architecture of ABM in 1149.4 standard. It is seen in Fig. 4.5 that signal processing must be included and performed inside the ABM in order to allow RF measurement. This processing extracts information from the RF signal, and represents the result as a low-frequency signal, which can be further processed. The circuit is composed of two individual RF-ABMs structures. The main parts of the two RF-ABMs are frequency (Fdet) and power detectors (Pdet) in which output DC quantities is relative to the input signal power and frequency, respectively. Measurement results (Vout, out- and out+) and tuning inputs (tunef and tuneP) to the detectors themselves can be connected to the IEEE 1149.4 type analog test ports using a programmable switch matrix (.4 MUX). The developed RF-ABMs can be used in basic frequency and power measurements. The developed DC-calibration also decreases measurement errors considerably.

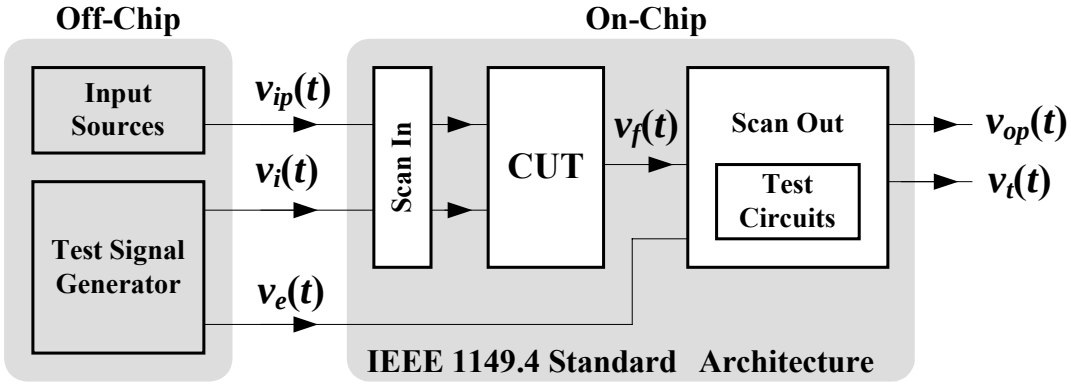



**Fig.4.6.** Block diagram of the basic approach of the proposed test scheme.

## 4.3 Proposed Sinusoidal Fault Signature Characterization Technique Through Two Level Crossing Voltages

Despite the fact that these existing ABM and TBIC potentially enable the accessibility to internal nodes for EXTEST, several restrictions in analog mixed-signal testing still remain, involving the requirement for duplicated ABMs at all pins, the lack of multiple pin accessibility at one time, and particularly the lack of INTEST capability. As previously summarized in Section 4.2, the extension to IEEE 1149.4 standard have recently been proposed as alternative solutions for these restrictions. It has also been reported that the output of built-in $V_{DDQ}$ and $I_{DDQ}$ monitoring can be scanned out in compliant with the IEEE 1149.4 standard (*Omayra and Angulo*, 2003). However, no complete parametric and dynamic INTEST capability with increased observability for both AC and DC fault signatures has been investigated. Consequently, this chapter aims to resolve this restriction through the extension of the IEEE 1149.4 architecture, and to develop a suitable testing circuit that exploits existing facilities including DC voltages, test buses and access ports.

### 4.3.1. Basic Approach to Sinusoidal Fault Signatures

Fig. 4.6 shows the diagram of basic approach of the proposed test scheme through the extension of the IEEE 1149.4 standard architecture. Unlike other approaches in which testing circuits are separated from the ABM, it is seen in Fig.4.6 that the testing circuit is included in the output ABM, generalizing the design of testing circuits and offering full test functionality with versatility for all types CUTs. In normal operation mode, the CUT obtains the primary input signal $v_{ip}(t)$, and provides the primary output signal $v_{op}(t)$. In test mode, the test signal generator provides two signals, i.e. a test stimulus signal denoted as $v_i(t)$ and a fault-free signal denoted as $v_e(t)$, easing the need for extra area for the registration of test pattern generation and fault-free bit streams. The test stimulus is

specifically a sinusoidal signal, which is an ordinary operating signal in most analog circuits, and has been employed extensively for testing purposes. The test output, denoted as $v_t(t)$, is reported in digital form, complying with both internal scan path operations and external monitoring. With reference to Fig.4.6, the proposed test strategy is the investigation on a response of a CUT to the presence of faults so called a fault signature, denoted as $v_f(t)$. This fault signature can be either single or combined changes in sinusoidal characteristics, involving changes in DC gain, amplitude, frequency and phase shift. This test strategy is purposely applied for the testing of analog portions in mixed-signal systems such as amplifiers and filters. In addition, this test strategy investigates and characterizes all possible fault signature types, including small and hard changes, at an initial design stage. Therefore, this test strategy offers high fault observability and eliminates the need for pre-simulation of actual fault signature characteristics.

The fault detection technique is a comparison of changes between the fault signature and the fault-free signal in time domain. Primarily, the sinusoidal input test stimulus can be expressed as

$$v_i(t) = V_i + v_i \sin(\omega_i t + \Phi_i) \tag{4.1}$$

where $V_i$ is DC offset level in volts, $v_i$ is amplitude in volts, $\omega_i$ is frequency in radian per second, and $\Phi_i$ is phase shift in degree per second. The details of the fault detection technique are described by two cases as follows. In the case when applying the sinusoidal test stimulus to a fault-free CUT, the expected output signal remains a sinusoid with some specific parameters, depending on operating conditions of the CUT such as amplitude amplification or frequency filtering. When the operating condition of the fault-free CUT is set for testing purposes, this expected output is known. The test signal generator consequently generates the fault-free signal $v_e(t)$, which has the same value as this expected output signal. In the case when applying the sinusoidal test stimulus to a faulty CUT, the presence of faults may cause some changes. The fault signature may different from the fault-free signal $v_e(t)$ and can be expressed as

$$v_f(t) = V_f + v_f \sin(\omega_f t + \Phi_f) + \Sigma v^n_f \sin(\omega_f t + \Phi_f)^n \tag{4.2}$$

It is seen in (4.2) that the fault signature is the summation of three constituents, i.e. a DC offset voltage, a major tone signal, and distortion components. Such differences in sinusoidal characteristics between $v_f(t)$ and $v_e(t)$ are observable through some changes in parameters, ranging from output parameter deviation that exceeds acceptable tolerances to extremely deformed sinusoids. Therefore, this chapter realizes the comparison between the signals $v_e(t)$ and $v_f(t)$ for fault detection. The comparison process is achieved by

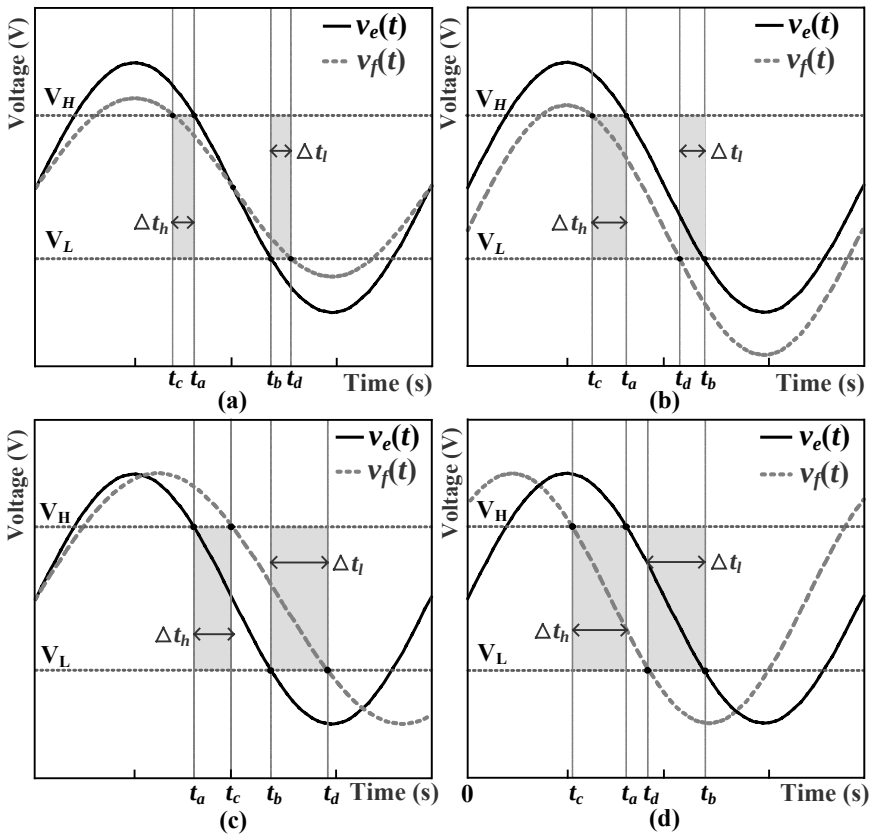



**Fig.4.7.** Examples of fault signature waveforms resulting from small changes in the distinct case $v_{fmax} > V_H > V_L > v_{fmin}$ .

characterizing sinusoidal characteristics through the use of two threshold voltages $V_H$ and $V_L$. This fault detection technique has purposely been proposed for the suitability of the implementation of a testing circuit embedded in the ABM of the IEEE 1149.4 architecture.

### 4.3.2 Sinusoidal Fault Signature Characterization Technique

Fault signature characterization is accomplished by two threshold voltages $V_H$ and $V_L$ as the crossing levels. Fault detection is performed by monitoring the values of crossing time difference between signals $v_e(t)$ and $v_f(t)$. The crossing time difference at $V_H$ is defined as $\Delta t_h = |t_a - t_c|$ where $t_a$ and $t_b$ are time when $v_e(t)$ and $v_f(t)$ cross over $V_H$, respectively. The crossing time difference at $V_L$ is defined as $\Delta t_l = |t_d - t_b|$ where $t_b$ and $t_d$ are time when $v_e(t)$ and $v_f(t)$ cross over $V_L$, respectively. This fault signature characterization process classifies fault signatures into two varieties of changes, i.e. small and hard changes.

On the one hand, the small change is defined as occurring in the distinct case $v_{fmax} > V_H > V_L > v_{fmin}$ where $v_{fmax}$ and $v_{fmin}$ are maximum and minimum peak amplitudes of $v_f(t)$, respectively. The measured parameters includes DC level, amplitude, frequency, and phase shift. Fig.4.7 demonstrates four particular examples of fault signature waveforms resulting

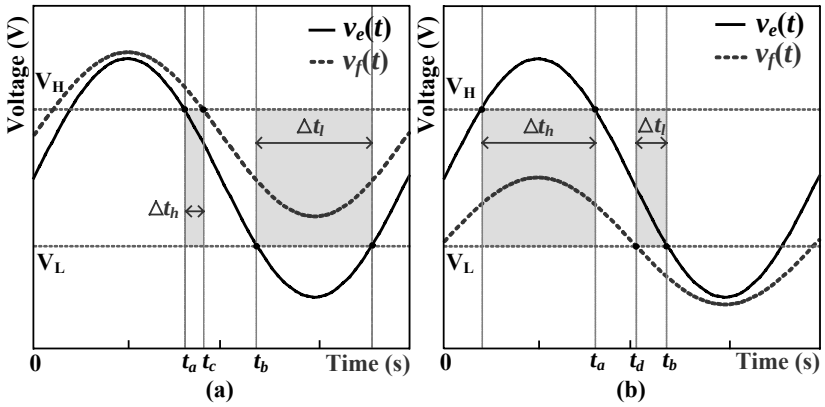



**Fig.4.8.** Examples of fault signature waveforms resulting from hard changes; (a) $v_f(t)$ showing $v_{fmax}>V_H>v_{fmin}>V_L$, (b) $v_f(t)$ showing $V_H>v_{fmax}>V_L>v_{fmin}$.

from small changes. The monitoring is investigated in the region of $T/4$ to $3T/4$ where $T$ is a signal period. Fig. 4.7 (a) demonstrates the fault signature with a decrease in amplitude, and shows that the values of $\Delta t_h$ and $\Delta t_l$ are equal. Increases in amplitude also exhibit similar characteristics. Fig. 4.7 (b) demonstrates the fault signature with a decrease in DC offset level and reveals that $\Delta t_h$ is greater than $\Delta t_l$. In cases where the DC offset increases, $\Delta t_h$ is smaller than $\Delta t_l$. Fig. 4.7 (c) shows the fault signature with a decrease in frequency, and shows that $\Delta t_h$ is less than $\Delta t_l$. In cases where the frequency is higher, $\Delta t_h$ is greater than $\Delta t_l$. Fig. 4.7 (d) demonstrates the fault signature with phase lagging behavior and shows that $\Delta t_h$ and $\Delta t_l$ are equal. Phase leading behavior also exhibits similar characteristics.

On the other hand, the hard change is defined as occurring in other cases except for the case of small changes. This hard change exhibits an enormous amplitude reduction or even steady DC outputs. Therefore, the amplitude of fault signatures dominates the measurement. Fig.4.8 demonstrates two particular examples of fault signature waveforms resulting from hard changes. The time differences are investigated throughout the signal period. Fig. 4.8 (a) demonstrates the fault signature with the case $v_{fmax}>V_H>v_{fmin}>V_L$. The value of $\Delta t_h$ is detectable in the similar manner to Fig. 4.7 (a). As there is no crossing of the fault signature at $V_L$, the value of $\Delta t_l$ is obtained at time between two crossing points of the signal $v_e(t)$ at $V_L$. Fig. 4.8 (b) demonstrates the fault signature with the case $V_H>v_{fmax}>V_L>v_{fmin}$. The value of $\Delta t_l$ is also detectable as demonstrated in Fig.4.7 (a). Similarly, the value of $\Delta t_h$ is obtained at time between two crossing points of the signal $v_e(t)$ at $V_H$. In addition to these two cases demonstrated in Fig.4.8, the hard changes include hardly deformed sinusoidal characteristics in other three possible cases, i.e. $v_{fmax}>v_{fmin}>V_H$, $V_H>v_{fmax}>v_{fmin}>V_L$, and $V_L> v_{fmax}>v_{fmin}$. In addition, fault signatures can also exhibit DC outputs, including stuck-at-$V_{DD}$ or stuck-at Gnd. These types of fault signatures provide the values of $\Delta t_h$ and $\Delta t_l$ throughout the signal period, and consequently faults are easily detected through this characterization process.

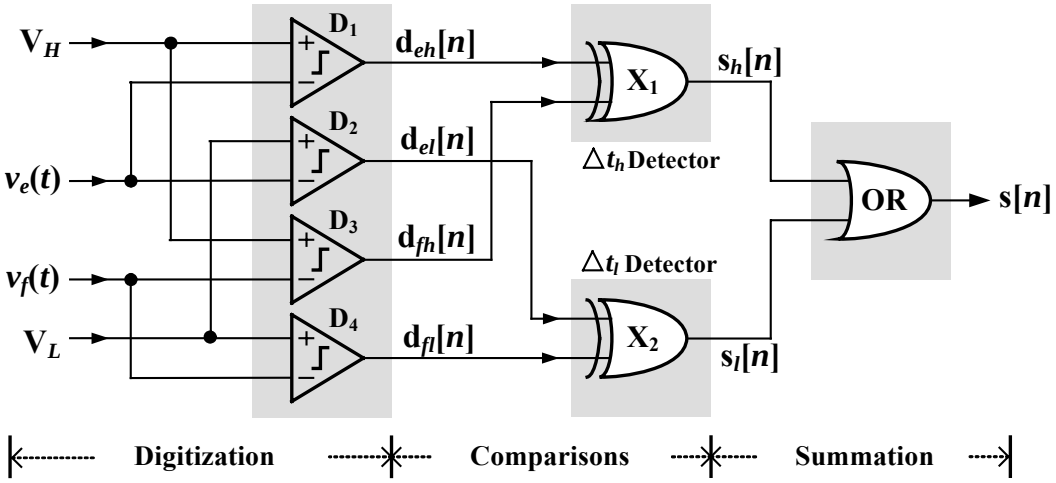



**Fig. 4.9.** Circuit diagram of the fault signature characterization-based testing circuit.

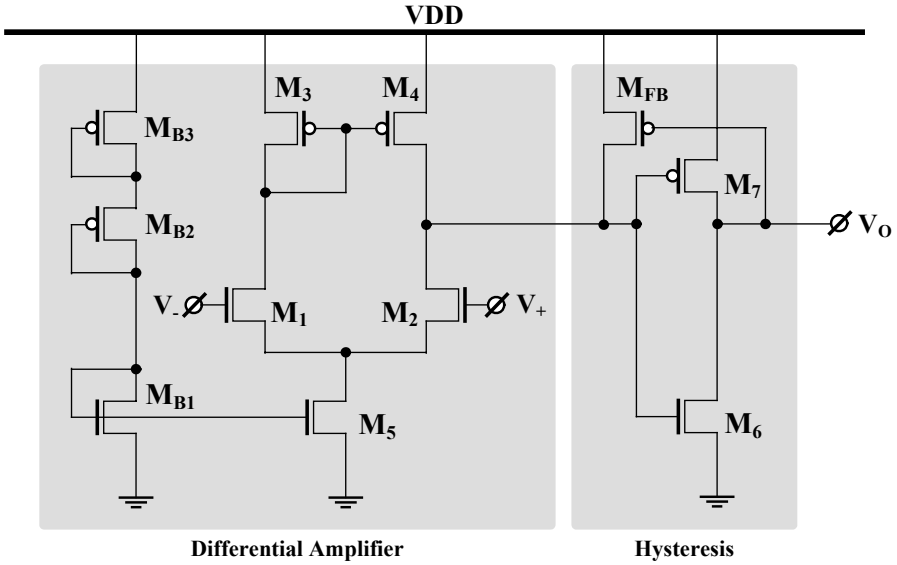



**Fig. 4.10.** Circuit configuration of the comparator with hysteresis.

### 4.3.3 Fault Signature Characterization Test Circuit

Fig.4.9 shows the circuit diagram of the designed testing circuit that performs fault signature characterization process. As shown in Fig.4.9, the fault detection process is performed consecutively in three steps, i.e. digitization, comparison and summation. Firstly, the digitization is performed by four comparators $D_1$ to $D_4$, which operate as 1-bit A/D converters. The signal $v_e(t)$ is digitized against $V_H$ and $V_L$ through $D_1$ and $D_2$, providing two sets of digital output signals $d_{eh}[n]$ and $d_{el}[n]$, respectively. The signal $v_f(t)$ is digitized against $V_H$ and $V_L$ through $D_3$ and $D_4$, providing two sets of digital output signal $d_{fh}[n]$ and $d_{fl}[n]$, respectively. Secondly, the comparison is performed by means of two XOR gates $X_1$

and $X_2$. This detection process simply monitors the difference between logics 1 and 0, and reports the outputs as 1 when the two inputs have different logical values. In this process, the comparison of $d_{eh}[n]$ and $d_{fh}[n]$ is performed for detecting the values of $\Delta t_h$ reported as $s_h[n]$. Similarly, the comparison of $d_{el}[n]$ and $d_{fl}[n]$ is performed for detecting the values of $\Delta t_l$ reported as $s_l[n]$. Finally, the summation of two signal $s_h$[n] and $s_l[n]$ are carried out through OR gate in order to report a single test output $s[n]$. Fig.4.10 shows the circuit configuration of the comparator with hysteresis realized for those four comparators $D_1$ to $D_4$ in Fig.4.9.

## 4.4 Test System Designs and Implementations

### 4.4.1 Overall Test System Designs

Fig. 4.11 shows the circuit configuration of the proposed ABM with extended functionality for on-chip and off-chip testing capability. The circuit comprises four major blocks, i.e. an analog CUT, an input ABM, an output ABM, and an internal switching network. First, the CUT can be a class of analog functional blocks such as amplifiers and filters. The primary inputs can be either an external input $v_{ip1}$ or an internal $v_{ip2}$ obtained from a D/A converter, and a primary output is $v_{op}$. Second, the input ABM located at the input pin comprises mainly the voltage comparator $C_D$ and the switches $S_D$, $S_G$, $S_L$, $S_H$, $S_{B1}$, $S_{B2}$, and $S_{GI}$. Third, the output ABM located at the output pin consists of the same components utilized in the input ABM except for the switch $S_{GI}$, and the testing circuit of Fig.4.9 with five control switches $S_T$. Last, the internal switching network located between the outputs of an internal D/A converter comprises the switches $S'_D$, $S'_{B1}$, $S'_{B2}$, and $S'_{GI}$, offering of testing accessibility in the case where $v_{ip2}$ is realized.

This ABM is capable of four testing modes as follows. Mode 1 is a traditional digital scan mode where the switches $S_D$, $S_G$, $S_L$, $S_H$ of both input and output ABMs are operating, corresponding to TDI signals, while other switches are opened. This Mode 1 allows the ABM to operate as the DBM by detecting bridging faults at the output terminal through the comparator $C_D$ and shifting to the serial digital test bus. Mode 2 is a traditional external analog test mode where the switches $S_{B1}$ of the input ABM and $S_{B2}$ of the output ABM are closed, while other switches are opened. The input signal stimulus sourced at the port AT1 is contributed to the CUT through the bus AB1. The output response from the CUT is provided at the bus AB2 and subsequently conveyed to the port AT2 for the external testing.

Mode 3 is an extended external analog test mode where the switch $S_{GI}$ of the input ABM is closed and the alternative input is sourced at $V_G$ terminal. This mode 3 provides the multiple-pin accessibility at one time by means of the direct access to the CUT, and the

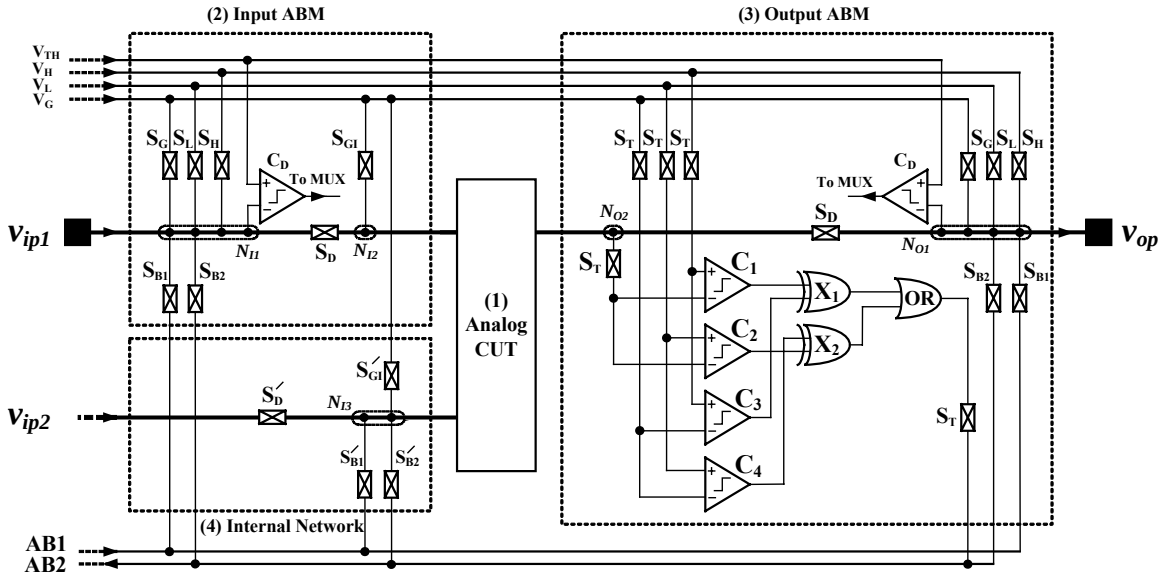



**Fig. 4.11.** Circuit configuration of the ABM with on-chip testing circuit.

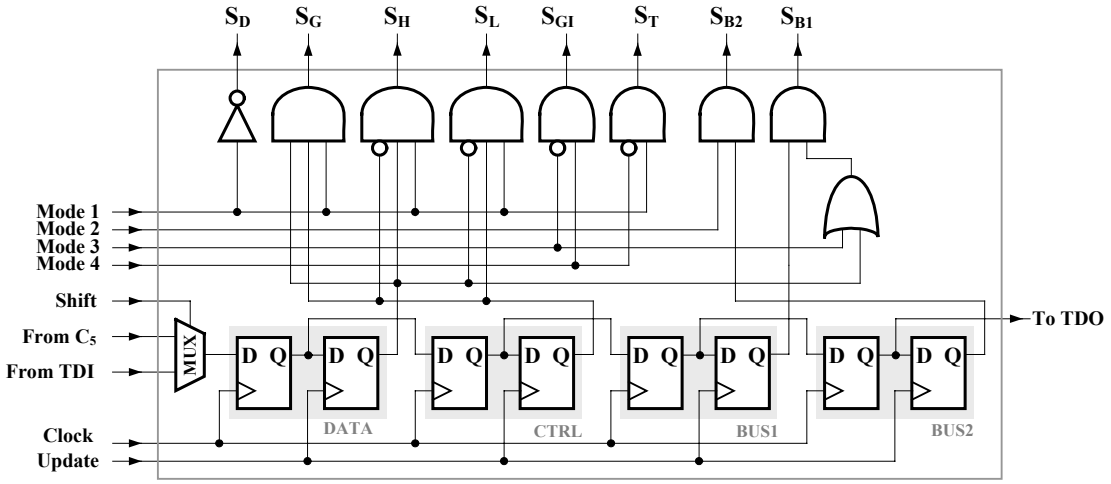



**Fig. 4.12** Block diagram of the control circuitry.

disconnection of input ABM and internal test buses. The corresponding output can be monitored separately at the output pin by closing the switch $S_D$ of the output ABM. Mode 4 is an extended on-chip testing mode through the signal characterization process where the switches $S_D$ and $S_{B1}$ of the input ABM are closed and all switches $S_T$ of the output ABM are closed, and others are opened. With reference to Fig.4.6, the input signal stimulus $v_i(t)$ sourced at the port AT1 is contributed to the CUT through AB1. The fault signature $v_f(t)$ obtained from the CUT at node $N_{O2}$ and the expected signal $v_e(t)$ sourced at the port $V_G$ are conveyed to the testing circuit. Subsequently, the test circuit processes signal characterizations and provides the test output to the output node $N_{O1}$. As the test circuit reports the faultiness by logic "1", the comparator $C_D$ subsequently captures the test output $s[n]$ at node $N_{O1}$ is then loaded in to the serial interface in order to complete a boundary

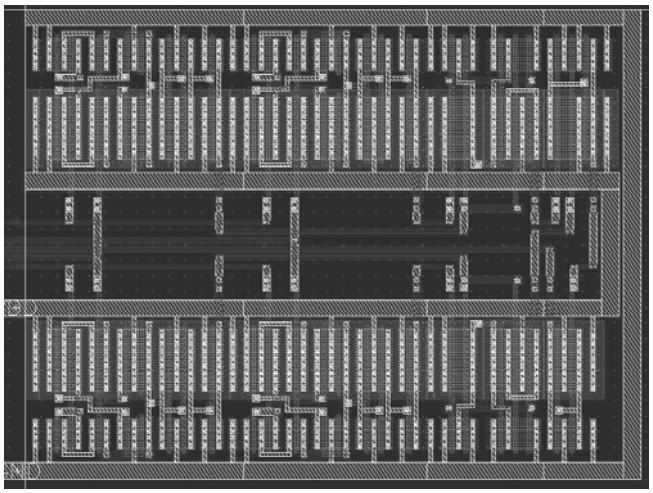


**Fig. 4.13.** Layout diagram of the fault signature characterization-based testing circuit.

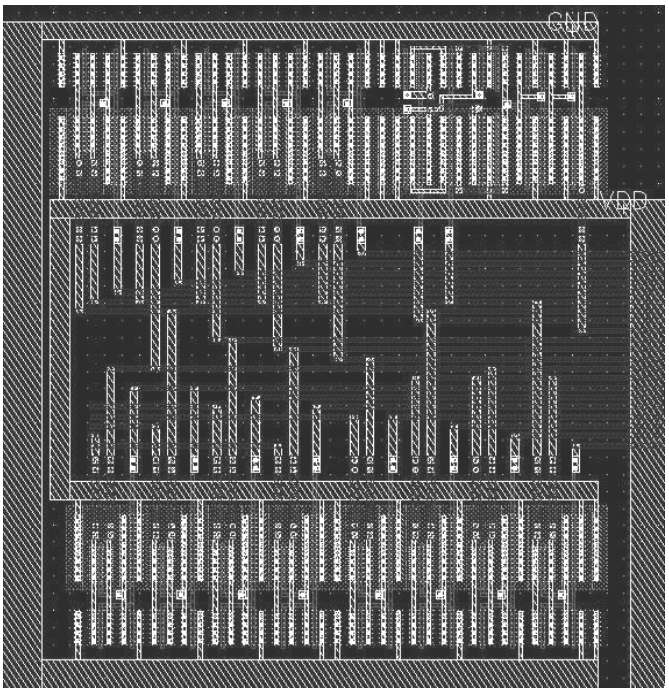



**Fig. 4.14.** Layout diagram of the arrangement of transmission gate switches.

scan throughout the system. This test output also called $v_t(t)$ also visible at the port AT2 conveyed by the bus AB2. Fig.4.12 shows the circuit diagram of the control circuitry, suggesting for the use in a full system implementation. The control and update shift registers, are utilized for loading control instruction and test data. However, the decoding logic is specially designed for accomplishing the four modes of operations. The decoded signals are exploited for controlling all the switches. In addition, the existing TIBC be employed directly for multiplexing the input and output test signals. Fig. 4.13 shows layout diagram of the fault signature characterization-based testing circuit. Fig. 4.14 shows layout diagram of the arrangements of transmission gate switches.

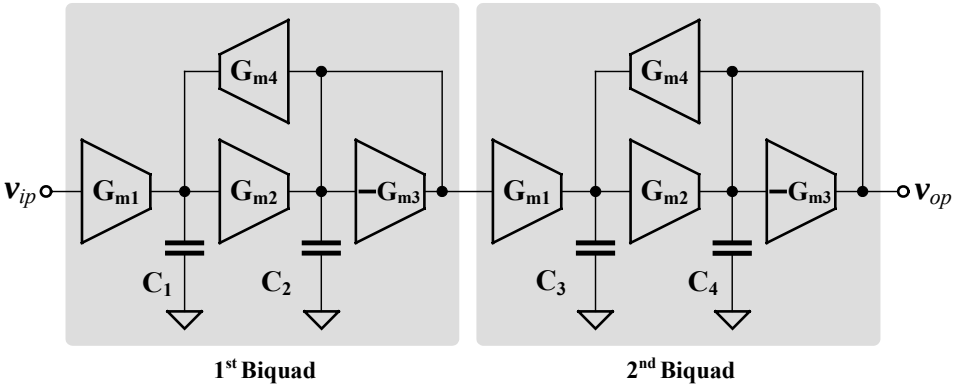



**Fig. 4.15.** Block diagram of the 4th-order $G_m$-$C$ filter.

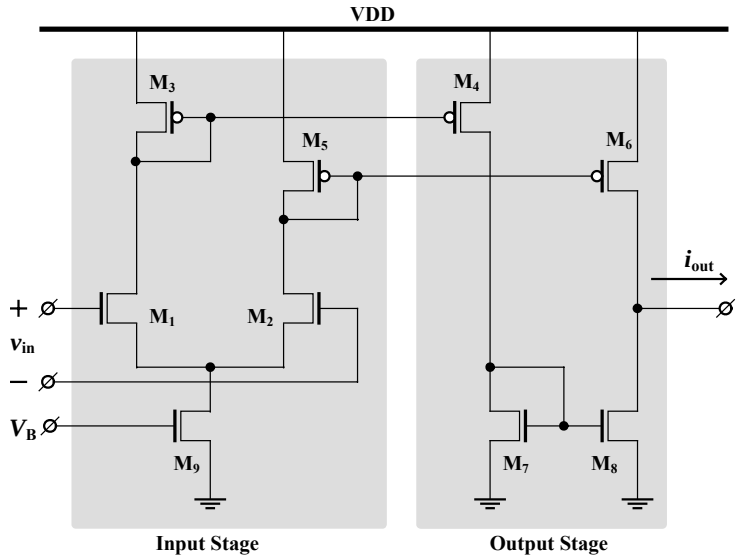



**Fig. 4.16.** Circuit diagram of the operational transconductance amplifier.

### 4.4.2 CUT Designs: The 4th-order $G_m$-$C$ low-Pass filter

As a particular example, a baseband 4th-order $G_m$-$C$ lowpass filter has been chosen as a CUT. The $G_m$-$C$ lowpass filter has been utilized extensively in base-band sections of RF receivers. These base-band sections are generally implemented by means of CMOS mixed-signal LSI chips, owing to the capability to operate at higher frequency compared to passive RC filters. Fig. 4.15 shows the block diagram a 4th-order low-pass $G_m$-$C$ filter, comprising a cascade connection of two identical 2nd-order $G_m$-$C$ biquads. The values of $G_{m1}$, $G_{m2}$ and $G_{m4}$ are equal, while the value of $G_{m3}$ is twice, i.e. $0.5G_{m3} = G_{m1} = G_{m2} = G_{m4}$. The values of capacitors $C_1$ and $C_2$ are equal, and capacitors $C_3$ and $C_4$ are also equal. These capacitors were implemented by linear on-chip capacitors. The $G_m$ blocks are balanced CMOS operational transconductance amplifiers (OTA). Fig. 4.16 shows the circuit configuration of a CMOS operational transconductance amplifier, which is utilized as the $G_m$ block in the CUT. The OTA comprises three major components, i.e. an nMOS

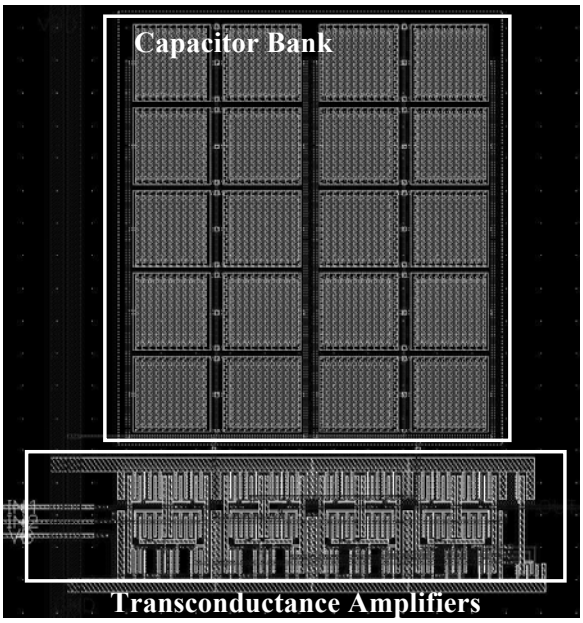



**Fig. 4.17.** Layout diagram of the 4th-order $G_m$-$C$ low-pass filter.

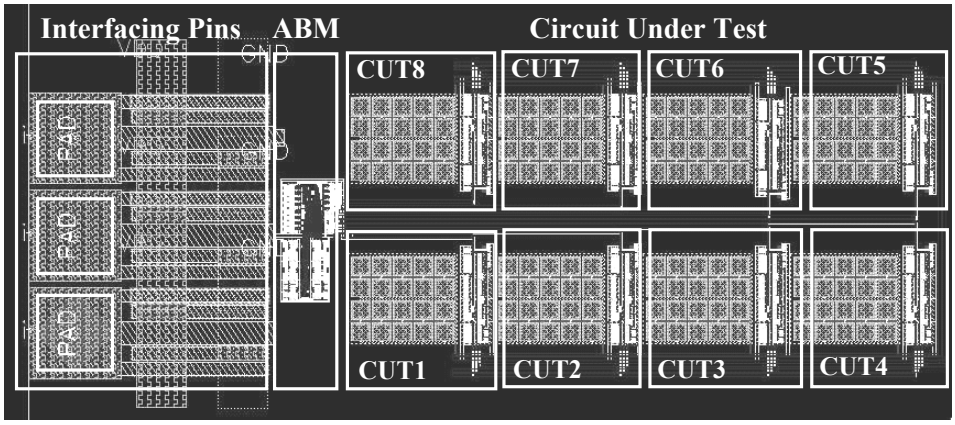



**Fig. 4.18.** Layout diagram of eight multiplexed CUTs using a single ABM.

differential pair formed by transistors $M_1$ and $M_2$, two pMOS current mirrors formed by transistors $M_3$ to $M_6$, and an nMOS current mirror formed by transistors $M_7$ to $M_8$. This OTA employs a single power supply voltage $V_{DD}$. Input and output signals are a voltage signal $v_{in}$ and a current $i_{OUT}$, respectively. Fig. 4.17 shows the layout diagram of the 4th-order $G_m$-$C$ low-Pass filter. Fig.4.18 shows the layout diagram of eight examples of CUTs with a single ABM, including two fault-free CUT6 and CUT7 without ABM, one fault-free CUT8 with ABM, and five faulty CUTs with ABM. Realistic faults were injected into these five sets of faulty CUTs. Three examples are defects in MOS transistors of OTAs considered from critical areas in the designed layout, including an internal metal layer bridge at $G_{m1}$ in CUT1, a metal crack $G_{m4}$ in CUT2, and a floating gate at $G_{m3}$ in CUT3. Other two examples are capacitance variation at $C_2$ in CUT4 and the potential open at $C_3$ in CUT5.

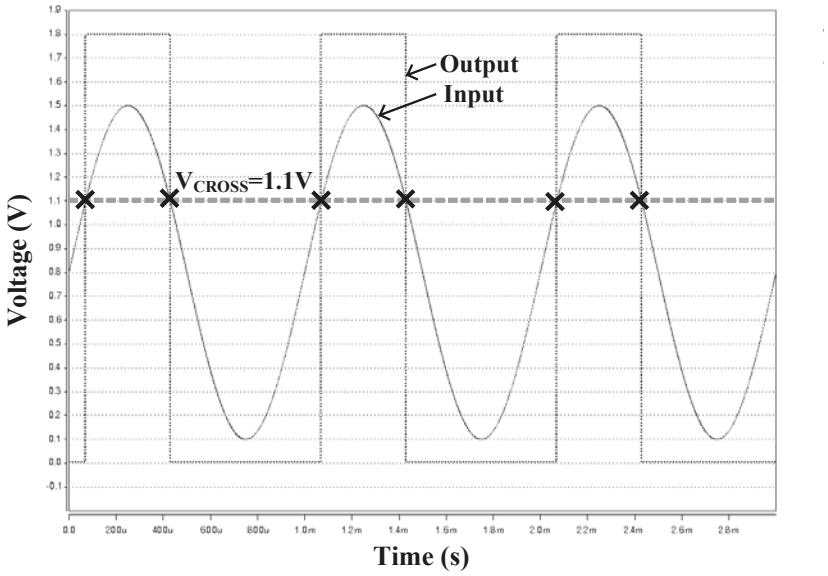



**Fig. 4.19.** Example of transient characteristics of comparator operations that trigger a sinusoidal input signal against the level crossing voltage of 1.1V.

**Table 4.2.** Summary of performances of the testing circuit shown in Fig.4.9.

| Testing Circuit Performances | | Values | Units |
|---|---|---|---|
| Comparator Performances | Maximum $V_H$ | 1.6 | V |
| | Minimum $V_L$ | 0.2 | V |
| | Offset Error | 0.042 | V |
| Minimum Detectable Variation | | >0.5 | % |
| Maximum Operating Frequency | | 260 | MHz |

## 4.5 Simulation Results and Discussions

As mentioned earlier, the proposed ABM with testing circuit were implemented using 0.18-μm standard CMOS technology, and simulated using Hspice. As depicted in Fig.4.18, the physical layout of the implemented system, including the ABM, CUTs and PADs. The transistor length was kept minimum at 0.18 μm. The sizes of transistor width were optimized. The area overhead is 18.5%. Note that the area overhead depends upon types of CUTs. Particularly, the testing circuit in this work was shifted into the ABM, which is shared for multiple internal analog building blocks. The area overhead may not present the difficulty in the overall system. This layout was initially extracted in order to obtain the circuit netlist prior to the simulation. The evaluation of design and test preprocess were performed as follows.

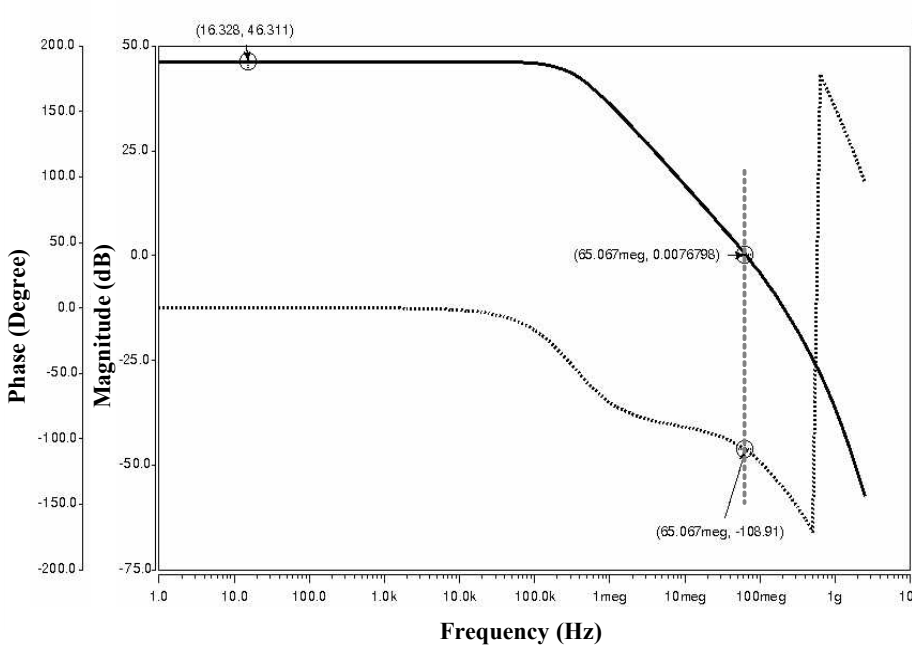



**Fig. 4.20.** Plots of magnitude and phase diagram of the transconductance amplifier.

**Table 4.3.** Comparisons of performances between a primitive CUT and a CUT with an exclusion of the IEEE1149.4 standard testing system.

| CUT Performances | Simulated Values | | | |
|---|---|---|---|---|
| | $CUT_{EXC}$ | $CUT_{INC}$ | % Dev. | Units |
| Cutoff Frequency | 11 | 11 | - | MHz |
| DC Gain | 4 | 3.99 | 0.0025 | dB |
| Linearity ($v_{pp}$=300mV) | 0.0067 | 0.00664 | 0.895 | % |

The performance of the fault signature characterization based test circuit is investigated as a major component in this design. The digital logic XOR and OR gates were implemented using standard cells, and all analog switches were implemented by a typical CMOS transmission gate in order to reduce an on-resistance. The comparators, which yield the accuracy of the test circuit and particularly designed based on hysteresis, was initially investigated through its transient characteristics. Fig. 4.19 shows the example of comparator operation that trigger a sinusoidal input signal against the level crossing voltage of 1.1V. It is seen in Fig.4.19 that the sinusoidal voltage above 1.1V is logic "1" while the sinusoidal voltage below 1.1 is logic "0". Therefore, this comparator is operating properly for further use in the test circuit. Table 4.2 summarizes the resulting performances of the ABM with testing circuit. As shown in Table 4.2, the comparators are capable to operate in a wide voltage comparison range of 0.2V to 1.6V with relatively low offset error

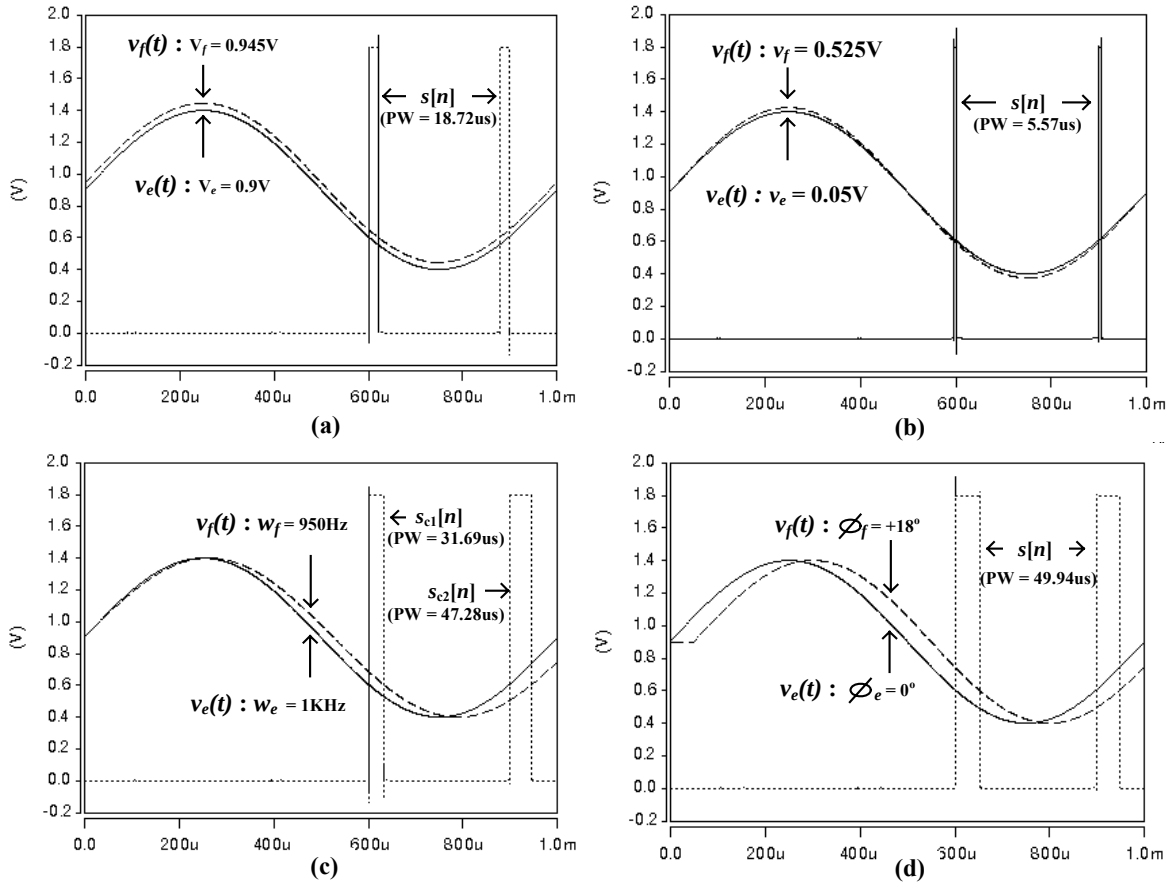



**Fig. 4.21.** Simulated waveforms of $v_e(t) = 0.9+0.5sin(2\pi 1000t)$ and $v_f(t)$ with 5% deviation.

of 0.042V throughout this range. Therefore, the voltages $V_H$ and $V_L$ can be adjustable broadly, depending on actual amplitude of a sinusoidal test stimulus. In addition, the maximum operating frequency is 260 MHz, offering a capability to obtain a wide range of input test stimulus frequency prior to this maximum frequency.

As the transconductance amplifier is major critical block in the $G_m$-$C$ low-pass filter. Fig. 20 shows the plots of magnitude and phase diagram of the transconductance amplifier. The DC gain is measured at 46.31 dB and the bandwidth is approximately 65 MHz. This condition is sufficient for implementing a $G_m$-$C$ low-pass filer. With reference to Fig.4.17, the performances of two filters were simulated and compared in order to validate testing operations and investigate performance degradation. Such two CUTs are the primitive CUT, called $CUT_{EXC}$, and the CUT with an inclusion of the IEEE1149.4 standard testing system, called $CUT_{INC}$. The CUT was designed with the cutoff frequency and DC gain of 11MHz and 4 dB, respectively. Table 4.3 shows the comparison of the performances between these two CUTs, measured at the pads of output pins. Although the performances deviation are expectedly introduced by additional stray capacitances and on-resistances of the switches, the deviation percentage shown in Table 4.3 are relatively low, including the deviation of the DC gain and the linearity of values 0.0025% and

0.895%, respectively, while no deviation of the cutoff frequency was evident. It can be concluded that the proposed testing system affects low impacts on primitive CUTs.

The capability of fault signature characterization were investigated and demonstrated. Fig.4.21 shows the simulated waveforms of the demonstrating fault-free signal $v_e(t)$ of $0.9+0.5sin(2\pi 1000t)$ and the fault signature $v_f(t)$ with 5% deviation of each sinusoidal parameters, including changes in DC level, amplitude, frequency and phase shift. In this test condition, the voltages $V_H$ and $V_L$ were optimally set at 1.2V and 0.6V, respectively. Fig. 4.21 (a) shows the increase in DC level $V_f$ at 0.945V, and the test output $s[n]$ reports the digital pulse with a pulse width (PW) of 18.72 μs. Fig. 4.21 (b) shows the increase in amplitude $v_f$ at 0.525V, and $s[n]$ reports a digital pulse with PW of 5.57μs. Fig. 4.21 (c) shows the decrease in frequency $\omega_f$ at 950Hz, and two pulses $s_{c1}[n]$ and $s_{c2}[n]$ report two digital pulses with PW of 31.69μs and 47.28μs, respectively. Fig. 4.21 (d) shows the change in $\Phi_f$ at $+18^o$, and $s[n]$ reports a digital pulse with PW of 49.94 μs. These four fault signatures in Fig. 4.21 indicate that the ABM with testing circuit effectively detects the faults that exhibit small variations. Consequently, this technique is potentially applicable for the detection of catastrophic faults, which generally exhibit hardly deformed sinusoidal outputs as previously shown in Fig.4.8. Moreover, it can be seen from Table 4.2 that this ABM with testing circuit could detect a minimum change in each single sinusoidal parameter at 0.5%. Therefore, parametric faults, which generally exhibit a variation in ±5% tolerance band, are also detectable.

Last, fault injections were performed, corresponding the fault models and the fault list of the CUT. Table 4.4 summarizes number of faults, detected and undetected faults, and fault coverage in percentages. As seen from Table 4.4, the simulation of fault injections, only one fault was injected in the CUT while other circuit elements and parameters are kept at their designed values. As the cut-off frequency of the filter is at 11 MHz, two test frequencies, i.e. a low frequency of 1KHz and a high frequency of 11.2 MHz, were realized. The fault coverage of faults associated in OTA is relatively high at approximately 94 % for both frequencies. Some undetected faults in OTAs were considered as hard-to-detect faults, such as transistor gate opens, which do not produce fault signatures at the output waveforms. The CUTs that have these hard-to-detect faults can be considered as non-defective CUT in the pre-screening of fault detection. Catastrophic faults and parameter variations of 15% of capacitors were completely detected, yielding fault coverage of 100%.

In this chapter, the propagation delay of the CUT, resulting from high-frequency operations or process variations, may cause some phase and gain changes. In order to avoid this problem, the testing condition of the CUT should be performed in a stable region, such as in the filter passband at unity gain, prior the maximum operating frequency of the testing circuit. In addition, the externally supplied fault-free signal should be in

**Table 4.4.** Summary of detected and undetected faults, and fault coverage.

| Fault Types | Faults | Fault Simulation Results | | | |
|---|---|---|---|---|---|
| | | Input frequency =1 kHz | | Input frequency =11.2 MHz | |
| | | Detected | Fault Coverage | Detected | Fault Coverage |
| (a) OTA (Catastrophic) | 352 | 331 | 94.03% | 334 | 94.87% |
| (b) Capacitors (Catastrophic) | 8 | 8 | 100% | 8 | 100% |
| (c) Capacitors (±15% Var.) | 8 | 8 | 100% | 8 | 100% |

**Table 4.5.** Comparisons of operating modes of related techniques.

| Characteristics | BIST Techniques | | |
|---|---|---|---|
| | ***Kac and Novak*** **(2003)** | ***Gorodetsky*** **(2005)** | **This work** |
| Digital Scan Mode | Yes | Yes | Yes |
| Analog Scan Mode | Yes | Yes | Yes |
| EXTEST Mode | Yes | Yes | Yes |
| INTEST Mode | No | No | Yes |

synchronization with the input stimulus using, for example, an external phase shifter or an available synchronized signal generator. The extra requirements, compared to the existing configuration, include an additional pin for the expected output signal and some additional transmission gate switches. The limitations of this work include testing for high-frequency circuits such as front-end RF receivers, and testing for analog circuits, which do not operate or provide sinusoidal signals, such as neural oscillators. In comparisons to other existing works, Table 4.5 shows the comparisons of operating modes of related techniques. The advantage of this work is a fully available functionality for both INTEST for on-chip testing with acceptable fault coverage, and the EXTEST for high-quality off-chip testing of some hard-to-detect faults and functional tests. In particular for INTEST, this work provides a non-intrusive and a complete detection of all possible fault signatures in standard environments rather than an individual testing circuits for each specific CUT. The proposed test strategy and technique can be further applied for analog-mixed signal circuits such as phase-locked loops and data converter circuits. Moreover, a complete BIST implementation using the proposed testing technique is also possible for some particular applications by only storing the fault-free signal in the system memory. The future planned

work involves the enhancement for high frequency testing and the applications for complete mixed-signal circuits and systems.

## 4.6 Conclusions

This chapter has presented the analog circuit test scheme through the extension of the IEEE 1149.4 standard. The proposed fault signature characterization technique provided the complete detection of sinusoidal fault signatures. The system implementation afforded functionalities for both INTEST for on-chip pre-screening of defective chips, and EXTEST for high-quality off-chip testing. The $4^{th}$-order $G_m$-$C$ low-pass filter with the inclusion of the proposed testing approach was fully implemented in the physical level. The maximum operating frequency of the ABM with testing circuit was measured at 260MHz, where both catastrophic and parametric faults were potentially detectable at the parameter variation greater than 0.5% with low performance degradation. The fault coverage of faults associated in CMOS and capacitors acceptable at approximately 94% and 100%, respectively. This chapter has offered the enhancement of standardizing test approach, which reduces the complexity of testing circuit, provides non-intrusive testing circuit, and is effectively applicable for pre-screening of defective devices.

# Chapter 5

## Regulated Supply Tuning Current-Starved Voltage-Controlled Oscillator with Built-In Self Test and Calibration

## 5.1 Introduction

This chapter presents the regulated supply tuning current-starved voltage-controlled ring oscillator with built-in self test and calibration. The chapter initially reviews the typical current-starved VCO, and related BIST and calibration techniques. A low-dropout regulator with an integrated low-pass filter operates as a frequency-tuning element with inherent noise suppression. Frequency calibration employs a bias current tuning in three frequency ranges for adjusting an oscillation frequency shift caused by parametric faults. Built-in voltage and current sensor facilitates on-chip accessibility and testability for catastrophic faults. Implementations show low jitter performance of less than 14.32ps at the oscillation frequency of 200MHz. High and low frequency ranges can be calibrated with the offset frequencies of 22MHz and 20MHz, respectively, through two-bit control signals. Tests for shorts and opens show total fault coverage of 83.68%.

## 5.2 Reviews on Current-Starved VCO with Related BIST and Calibration Techniques

### 5.2.1 Typical Current-Starved VCO Configuration

A VCO has been employed in a variety of applications such as in Phase-Locked Loops (PLLs) or in clock-and-data recovery circuits. Two types of oscillators are LC-based and ring-based VCOs. The LC-based VCOs offer low jitter performance determined by passive components, and relatively immune to power supply noises due to a differential topology. However, most LC-based VCOs require large chip area for inductors, and provide narrow tunning range, limiting applications to narrow-frequency range applications. In contrast, ring-based VCOs offer a wide tunning range, and occupy small chip area since no passive devices are necessary. Nonetheless, power supply noise is a

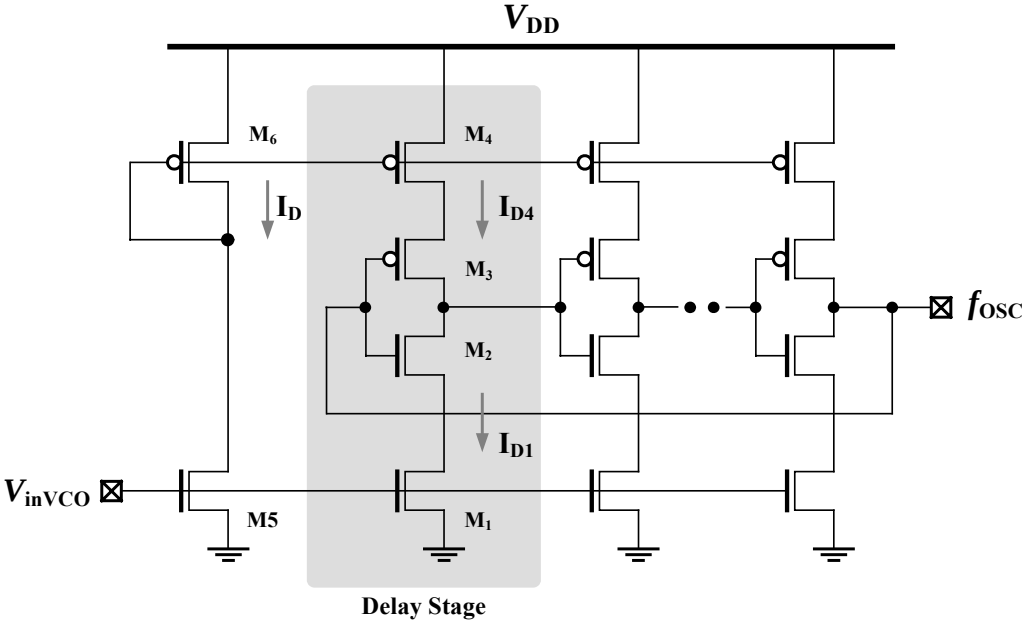



**Fig. 5.1.** Circuit configuration of the typical current-starved VCO.

major critical factor in ring-based VCOs, and has detrimental effects on jitter performance. The current-starved ring VCO has been employed extensively since wide tuning range and high-frequency oscillating signal can be achieved.

Fig. 5.1 schematically shows the configuration of the typical current-starved VCO. As shown in Fig. 5.1, transistors $M_2$ and $M_3$ operate as an inverter, while $M_1$ and $M_4$ operate as a current source. This current source limits the current available to the inverter. The drain currents of $M_5$ and $M_6$ are identical, and are set by the input control voltage $V_{\text{inVCO}}$. The currents in $M_5$ and $M_6$ are mirrored to each inverter and current source in each stage. Fig. 5.2 shows the simplified diagram of a single stage of the current-starved VCO. With reference to Fig. 5.2, the total capacitance $C_{\text{tot}}$ on the drain of transistors $M_2$ and $M_3$ is given by

$$C_{\text{out}} = C_{\text{out}} + C_{\text{in}} = C_{\text{OX}}(W_{\text{P}}L_{\text{P}} + W_{\text{N}}L_{\text{N}}) + \frac{3}{2}C_{\text{OX}}(W_{\text{P}}L_{\text{P}} + W_{\text{N}}L_{\text{N}}) \tag{5.1}$$

where $C_{\text{out}}$ and $C_{\text{in}}$ are output and input capacitances of the inverter. $C_{\text{OX}}$ is a gate-oxide capacitance. $W_{\text{P}}$ and $L_{\text{P}}$ are effective width and length of PMOS transistor, respectively. $W_{\text{N}}$ and $L_{\text{N}}$ are effective width and length of NMOS transistor, respectively. It can be considered that the time required for charging $C_{\text{tot}}$ from zero to the switching voltage $V_{\text{SP}}$ with the current $I_{\text{D4}}$ is given by

$$t_1 = C_{\text{tot}}\left(\frac{V_{\text{SP}}}{I_{\text{D4}}}\right) \tag{5.2}$$

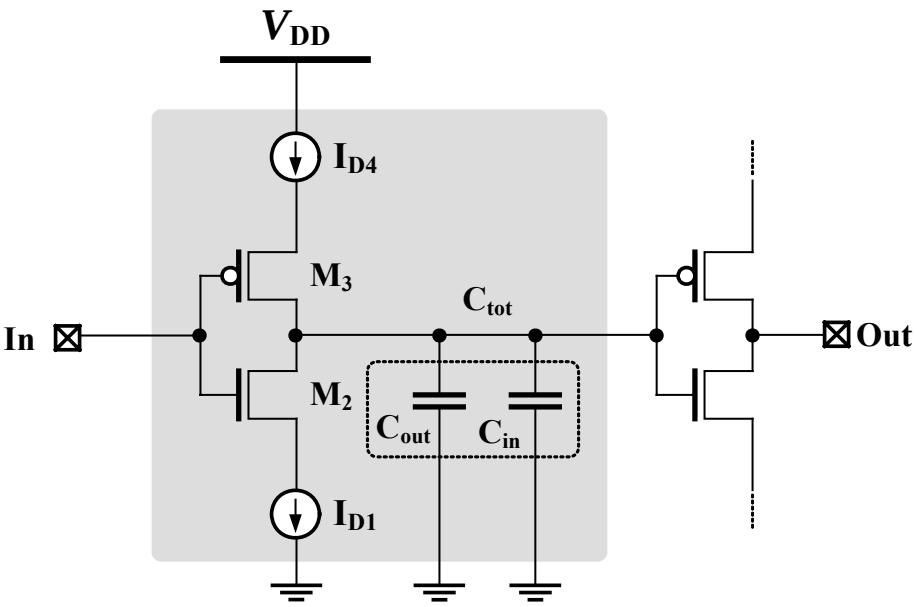



**Fig.5.2.** The simplified diagram of a single delay.

while the time required to discharge $C_{tot}$ from $V_{DD}$ to $V_{SP}$ is given by

$$t_2 = C_{tot}\left(\frac{V_{DD} - V_{SP}}{I_{D1}}\right) \tag{5.3}$$

If the currents are set as $I_{D4} = I_{D1} = I_{D,}$ the summation of $t_1$ and $t_2$ can be expressed as

$$t_{tot} = t_1 + t_2 = \frac{C_{tot}V_{DD}}{I_D} \tag{5.4}$$

The oscillation frequency $f_{OSC}$ of the current-starved VCO for N of the stage is given by

$$f_{OSC} = \frac{1}{Nt_{tot}} = \frac{I_D}{NC_{tot}V_{DD}} \tag{5.5}$$

The center frequency $f_{CENTER}$ of the VCO is at $V_{DD}/2$. Generally, the output of the current-straved VCO is normally buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can be significantly affecting the oscillation frequency or lower the gain of the oscillator and therefore oscillation cannot be sustained.

### 5.2.2 Reviews on Related BIST and Calibration Techniques for VCOs

Table 5.1 summarized three related BIST and calibration techniques for VCOs, involving *Azais et al.* (1998), *Perlemo et al.* (2000), and *Nakanishi et al.* (2005). As shown in Table 5.1(a), *Azais et al.* (1998) proposed the test technique based on the reconfiguration

**Table 5.1.** Summary of related BIST and calibration techniques for VCOs.

| Category | Authors | Years | Techniques |
|---|---|---|---|
| (a) BIST | *Azais et al.* | 1998 | Inverter delay test |
| (b) Calibration | (b.1) *Perlemo et al.* | 2000 | Switching capacitance loads |
| | (b.2) *Nakanishi et al.* | 2005 | Switching current sources |

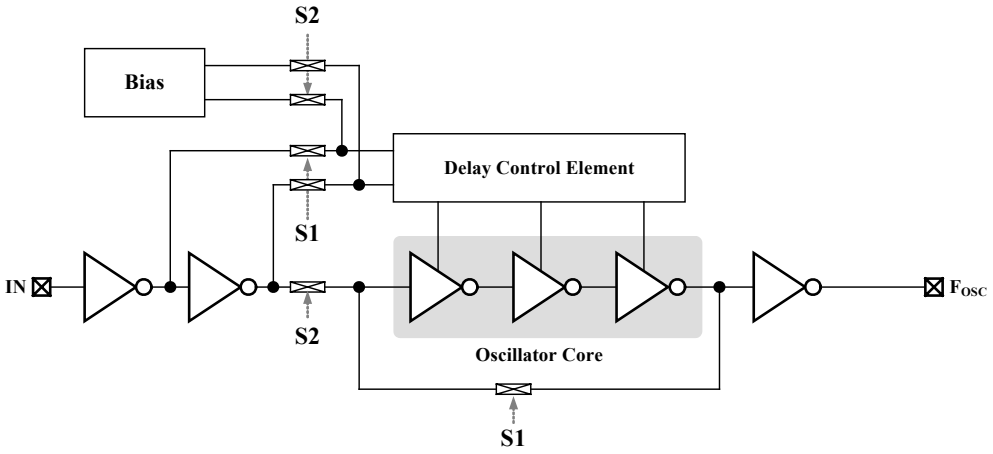



**Fig.5.3.** Circuit diagram of the BIST based on the re-configurable VCO (*Azais et al.*, 1998)

concept in which the VCO is modified in order to operate as a digital structure in test mode. Under this condition, the test can be performed on standard digital test equipment. Fig. 5.3 shows the re-configurable VCO principle. The typical VCO is configured through five switches, controlled by the signals $S_1$ and $S_2$. In normal mode, the switch $S_1$ and $S_2$ are closed and opened, respectively, and therefore the circuit is operating as a normal oscillator. In test mode, the switch $S_1$ and $S_2$ are opened and closed, respectively, and therefore the circuit is configured as a cascade connection of inverters. The square input is applied to the inverter chain, and the delay is measured. In the case where catastrophic and parametric faults exist in the VCO, the delay is different from the expected value, yielding in fault detection capability. Additionally, the delay control element is connected to the bias voltage during test operation in order to extend the capability to detect those hard-to-detect faults. This technique performs only BIST operation with the fault coverage of 80%.

As shown in Table 5.1(b.1), *Perlemo et al.* (2000) proposed a calibration technique for a current-starved VCO with tunable capacitive loads. Changing the propagation delay of the inverting cells by adjusting the effective amount of loading capacitance is used to tune the VCO output frequency. Fig.5.4 shows the delay cell with calibration technique using one continuously tuned capacitive load and three discrete tuning capacitors**.** On the one hand, the NMOS active resistor $M_C$ is tuned by the controlling voltage $V_C$ in order to adjust the effective value of capacitor $C_C$ that the delay

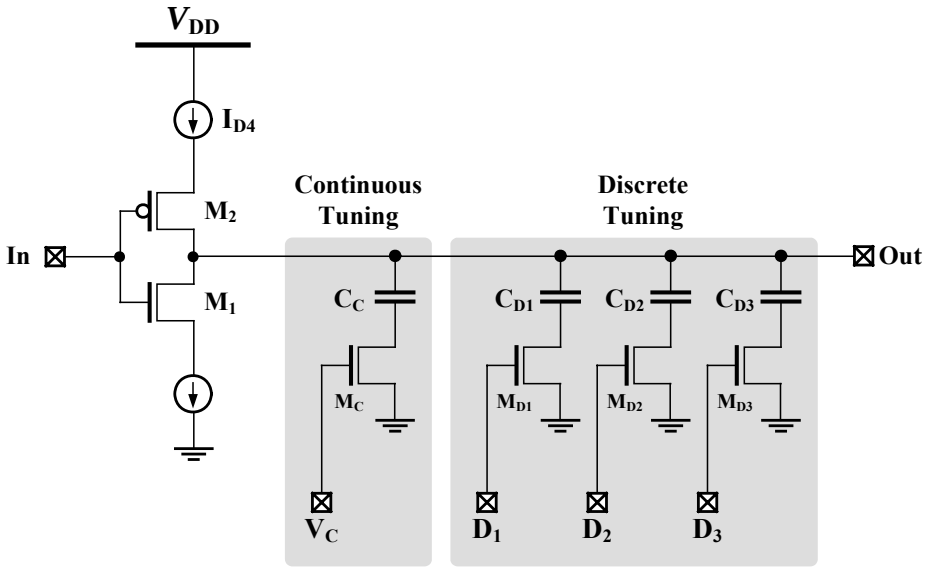



**Fig.5.4.** Frequency calibration using switching capacitance loads (*Perlemo et al.*, 2000).

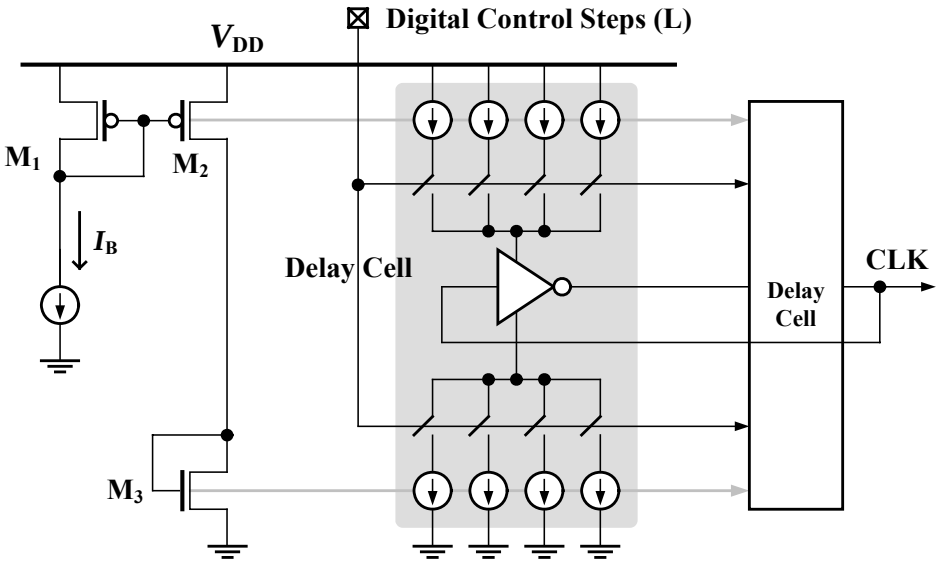



**Fig.5.5.** Frequency calibration using switching current sources (*Nakanishi et al.*, 2005).

cells must drive. This VCO delay cell with NMOS active resistors displays a negative conversion gain since the increase in control voltage results in the decrease in active resistance, causing the delay elements to be loaded by more effective capacitance, which increases their propagation delay. On the other hand, switching in discrete capacitors $C_{D1}$ to $C_{D3}$ allows the oscillator to achieve a wide range of operation while maintaining a low conversion gain. Realizing three identical discrete tuning capacitors permits the oscillator to operate in four different frequency bands. The amount of adjacent band overlap is inversely proportional to the amount of discrete capacitance that is incrementally applied to the delay cells. This frequency overlap may be adjusted to suit individual design requirements by appropriately sizing the discrete capacitors.

As shown in Table 5.1(b.2), *Nakanishi et al.* proposed a current-starved VCO with calibration technique using switching current sources. Fig.5.5 shows frequency calibration using switching capacitance loads. It is seen that the self-calibrating operation is realized by multiplexing the output of the variable current source in the delay cell. The digital control steps L are ranging from 1 to 4. The proposed VCO is expected to have good jitter characteristics compared with the conventional VCO even if the digital control step $L$ is small. Realizing a multi-current source in the delay cell yields linear tuning characteristics of the VCO gain and also provides frequency calibration capability in PLL applications.

## 5.3 Proposed Regulated Supply Tuning Current-Starved Ring VCO with Built-In Test and Calibration Circuits

Power supply noise minimizations in ring-based VCOs can be achieved by using a power supply calibration technique (*Wu et al*, 2007) or a jointly biasing the supply and control voltage (*Hsieh et al.*, 2009). Alternatively, power supply regulation techniques (*Brownlee et al.*, 2005; *Alon et al.*, 2006) have been suggested for suppressing power supply noises in ring-based VCOs. The regulator operates as a frequency control element, transferring a control voltage for tunning an oscillation frequency through a virtual supply voltage. As there is no direct connection between the VCO and the power supply, the regulator with inherent supply noise rejection eliminates supply noises that generally contribute to the VCO, resulting in low jitter performance.

In addition to the power supply noise suppression issue, BIST and calibration process applied to VCO accommodates parametric variations, particularly in scaling CMOS technology. As described in Section 5.2, those techniques have achieved test and frequency calibration functionalities. However, the modification of delay cells and additional components in all delay stages is required. In addition, the test procedures necessarily require external test equipment. No complete built-in test technique has been investigated since additional test circuitries may cause noises and performance degradations. Therefore, this section presents a regulated supply tuning current-starved VCO with built-in test and calibration. BIST and calibration processes are achieved with low supply noises and performance degradation.

### 5.3.1 Circuit Descriptions and Operations

Fig.5.6 shows the circuit diagram of the regulated supply tuning current-starved VCO with built-in voltage and current sensors and frequency calibration circuit. As shown in Fig.5.6, the overall circuit consists of four major components, including a current-starved VCO core, a regulator (REG), a frequency calibration circuit (CAL), and

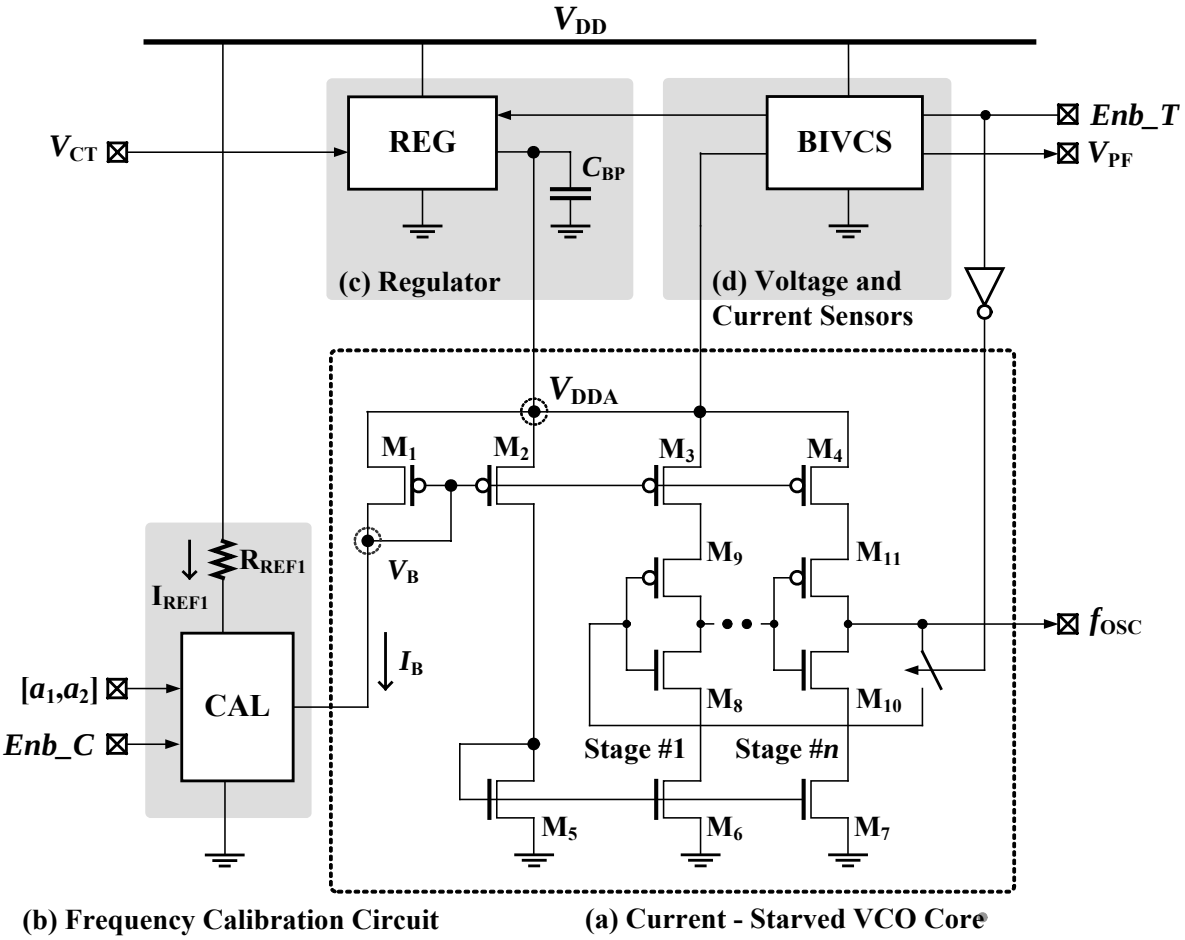



**Fig. 5.6.** Circuit diagram of the proposed regulated supply-tuning current-starved ring VCO with BIST and calibration circuits.

a built-in voltage and current sensor (BIVCS). First, the current-starved ring VCO core comprises $n$ stages of inverters connected in a closed loop, providing an output oscillation frequency $f_{OSC}$. Frequency tuning of VCO is performed by changes in a virtual supply $V_{DDA}$ while frequency calibration is performed by changes in a bias current $I_B$. Second, the regulator is operating as a frequency control element where input and output voltages are a control voltage $V_{CT}$ and the virtual supply $V_{DDA}$. Third, the frequency calibration circuit switches the values of the bias currents corresponding to two-bit control signals $a_1$ and $a_2$. Last, the built-in voltage and current sensor connected between $V_{DD}$ and the virtual supply $V_{DDA}$ monitors internal defective components, providing a test output voltage $V_{PF}$

The proposed VCO is capable of operating in three modes, including normal oscillation, test, and calibration modes. These three modes are controlled by Test Enable (*Enb_T*) and Calibration Enable (*Enb_C*) signals. In normal oscillation mode, the BIVCS is removed from other blocks by setting *Enb_T* = 0 and *Enb_C* = 0. Although no test and calibration are performed, the frequency calibration circuit still provides a constant current

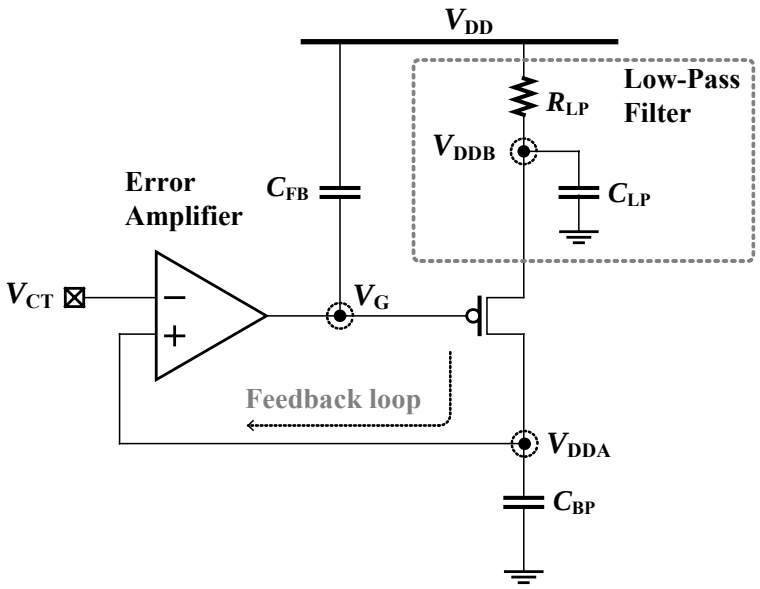



**Fig.5.7.** Circuit diagram of the modified low-dropout regulator with a low-pass filter.

$I_B$ for proper bias conditions. In test mode, the loop is disconnected by setting *Enb_T* = 1 and *Enb_C* = 0, allowing the BVICS to perform test operations for other three blocks. In calibration mode, the BVICS is removed and the calibration are performed by setting *Enb_T* = 0 and *Enb_C* = 1, allowing the two-bit signals to switch the frequency ranges.

### 5.3.2 Oscillation Frequency and a Low Dropout Regulator

With reference to Figs.5.6 (a) and (b), the current source in the calibration circuit constantly provides the bias current $I_B$, which is contributed to inverters through the current steering circuit formed by transistors $M_1$ to $M_7$. This current steering circuit starves an equal value of bias currents in all inverters formed by, for example, $M_8$ to $M_{11}$. The oscillation frequency $f_{OSC}$ of the *n*-stage ring VCO can be described as $f_{OSC} = I_B/(n.C_T.V_{DDA})$ where $C_T$ is a total capacitance at the drain terminals of each delay stage. It can be considered that the oscillation frequency of this *n*-stage ring VCO is a function of three parameters, i.e. $I_B$, $C_T$ and $V_{DDA}$, which can be exploited for frequency tunning and calibrations. Tunning the oscillation frequency through $I_B$ offers a positive VCO gain as $I_B$ is directly proportional to $f_{OSC}$. Tunning the oscillation frequency through $C_T$ and $V_{DDA}$ offers a negative VCO gain as $C_T$ and $V_{DDA}$ are inversely proportional to $f_{OSC}$. This work tunes the oscillation frequency through $V_{DDA}$, and calibrates operating frequency ranges through $I_B$. As shown in Fig.5.6 (c), the regulator couples the power supply $V_{DD}$ and the VCO core. Preferable performances are low voltage drop, high power supply noise rejection and high stability. Conventional low-dropout regulator (*Brownlee et al.*,2005) has

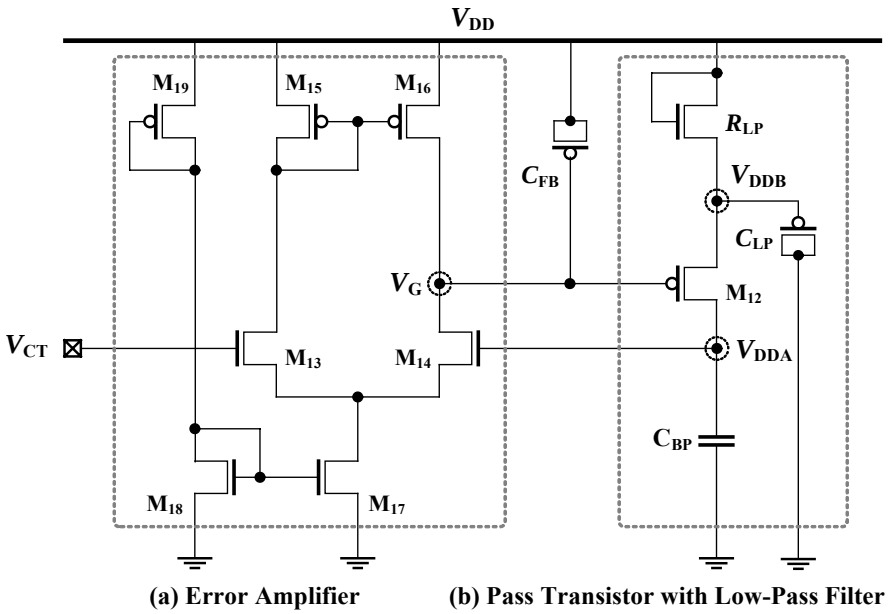



**Fig.5.8.** Circuit configurations of the modified low-dropout regulator.

low power supply rejection at high frequency. In order to increase the power supply rejection, the replica-compensated linear regulators (*Alon et al.*, 2006) have proposed by replacing the error amplifier in a local replica feedback loop. However, optimisations for the replica load and accurate loop stability analysis are necessary in order to achieve a high power rejection. Therefore, this chapters presents a modified low dropout regulator that suppresses both low and high frequency power supply noises using a low-pass filter.

Fig.5.7 shows the circuit diagram of the modified low-dropout regulator with an integrated low-pass filter. A pMOS device with large transistor size implements the pass transistor in order to achieve a low voltage drop. The error amplifier *EA* compares the voltage values between $V_{DDA}$ and $V_{CT}$, providing an error voltage $V_G$ as an output voltage. The positive feedback loop forces $V_G$ to be zero at steady state, yielding $V_{DDA} = V_{CT}$. The low-frequency noise is filtered by the transfer function of the loop formed by the amplifier and the pass transistor. The low-pass filter formed by $R_{LP}$ and $C_{LP}$ is inserted between $V_{DD}$ and the source terminal of the pass transistor. This low-pass filter introduces a new supply voltage $V_{DDB}$ for the pass transistor, and filters out high-frequency noises. The positive feedback loop is stabilised by the bypass capacitor $C_{BP}$ in order to prevent the Darin current oscillation. The capacitor $C_{FB}$ sets the bandwidth of the closed-loop transfer function. Fig.5.8 shows the circuit configurations of the modified low-dropout regulator using CMOS implementations. The pMOS transistor $M_{12}$ implements the pass transistor. The error amplifier is formed by transistors $M_{13}$ to $M_{19}$. The resistor $R_{LP}$ is a diode-connected nMOS transistor in order to occupy small area. Both capacitors $C_{FB}$ and $C_{LP}$ are implemented by MOS capacitors. The bypass capacitor $C_{BP}$ is a linear capacitor.

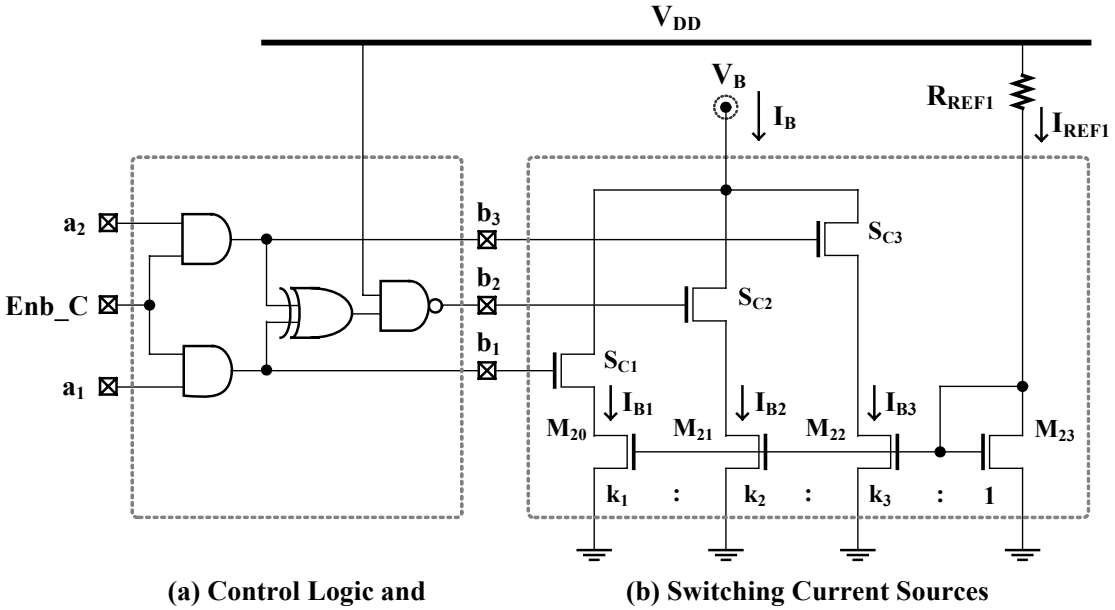



**Fig.5.9.** Circuit configuration of the frequency calibration circuit.

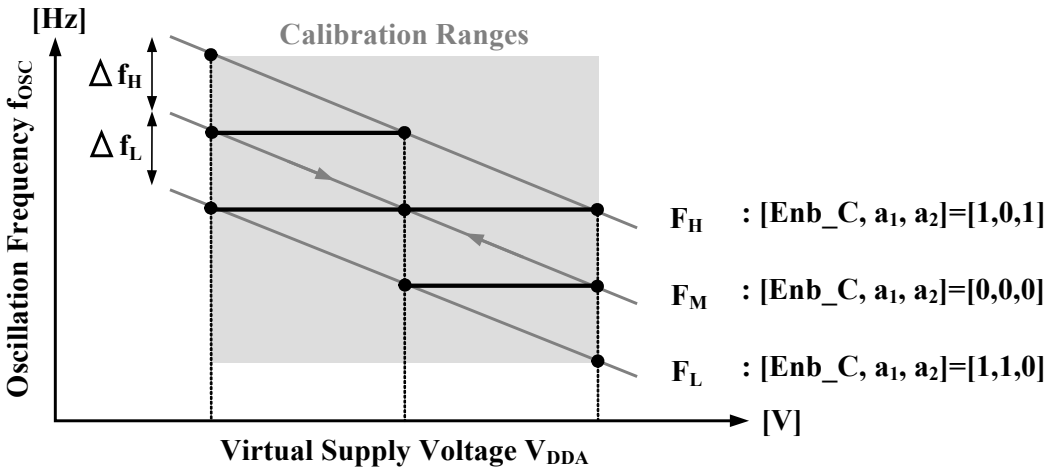



**Fig.5.10.** Three frequency ranges in frequency calibration operations.

### 5.3.3. Proposed Frequency Calibration Circuit

As previously described in Chapter 1, parametric faults involve changes in circuits that degrade expected performances. Parametric faults are caused by intrinsic failures, including gate-oxide shorts and process parameter variations of nominal values. As parametric faults in CMOS technology typically depend on tolerance band acceptability, modeling of parametric faults is relatively complicated at physical design level, and high-precision testing after fabrication is generally realized. Therefore, the calibration circuit is facilitated during design process in order to accommodate parametric faults after fabrications. Frequency calibration strategy of this work is the use of current-starved inverters instead of simple inverters, enabling the separation of the tuning through the

control voltage $V_{CT}$ and the bias current $I_B$. No current sources or loading capacitances are required for every delay stages. In addition, this calibration technique incorporates a logic control circuit that performs the switching to both high and low frequency ranges by means of two-bit control signals. Fig.5.9 shows the circuit configurations of the frequency calibration circuit. Two major components are the control logic and the switching current sources. The control logic implemented by AND, XOR, and NAND gates is introduced for controlling the switches $S_{C1}$, $S_{C2}$, and $S_{C3}$. Hence, calibrating for both high and low frequency ranges can be achieved. The current sources mirror the reference current $I_{REF1}$ obtained from $R_{REF1}$, and provide three values of bias currents based on the transistor parameters, i.e. $k_1$ to $k_3$. A current steering circuit formed by $M_{20}$ to $M_{23}$ implements three current sources. The transistor parameters are set as $k_1 > k_2 > k_3$ by designing a proportional value of the aspect ratio (W/L), resulting in $I_{B1} > I_{B2} > I_{B3}$.

Fig.5.10 demonstrates three frequency ranges in frequency calibration operations. First, the middle frequency range $f_M$ is the expected operating frequency range, indicating a proper operation of the VCO and no calibration process is required. No control bits for this frequency range $f_M$ are applied, i.e. [*Enb_C*, $a_1$, $a_2$] = [0,0,0]. The switch control signals are consequently given by [$b_1$, $b_2$, $b_3$] = [0,1,0]. As one of input terminal of NAND gate is always connected to $V_{DD}$, the switch $S_2$ in closed, yielding in $I_B = I_{B2}$. Second, the range $f_L$ is a low frequency range that deviates from $f_M$ by the frequency offset $\Delta f_L$. When the actual frequency traces on this $f_L$, calibration can be performed in order to increase $f_{OSC}$ to retrace on $f_M$. The control bits are [*Enb_C*, $a_1$, $a_2$] = [1,1,0], resulting in [$b_1$, $b_2$, $b_3$] = [1,0,0]. Therefore, the switch $S_{C1}$ is closed and the current $I_B = I_{B1}$, increasing the oscillation frequency to retrace on $f_M$ since the bias current $I_{B1}$ is greater than $I_{B2}$. Last, the range $f_H$ is a high frequency range that deviates from $f_M$ by the frequency offset $\Delta f_H$. When the actual frequency traces on this $f_H$, calibration can be performed in order to decrease $f_{OSC}$ to retrace on $f_M$. The control bits are [*Enb_C*, $a_1$, $a_2$] = [1,0,1], resulting in [$b_1$, $b_2$, $b_3$] = [0,0,1]. Therefore, switch $S_3$ in closed and the current $I_B = I_{B3}$, decreasing the oscillation frequency to retrace on $f_M$ since the bias current $I_{B3}$ is less than $I_{B2}$.

### 5.3.4 Proposed Built-In Voltage and Current Sensor (BIVCS)

As mentioned earlier, catastrophic faults involve changes in circuits that cause circuit operations to fail catastrophically. A quiescent current testing technique ($I_{DDQ}$) has been employed as effective fault detection method for various analog circuits (*Wang et al.*, 1998; *Dragic et al.*, 2004). This $I_{DDQ}$ testing technique is relatively simple based on the comparison between $I_{DDQ}$ and a reference current through a built-in current sensor connected between $V_{DD}$ and CUT. However, major limitations are power supply variation and voltage headroom. In addition to $I_{DDQ}$ testing, a voltage testing technique ($V_{DDQ}$) has

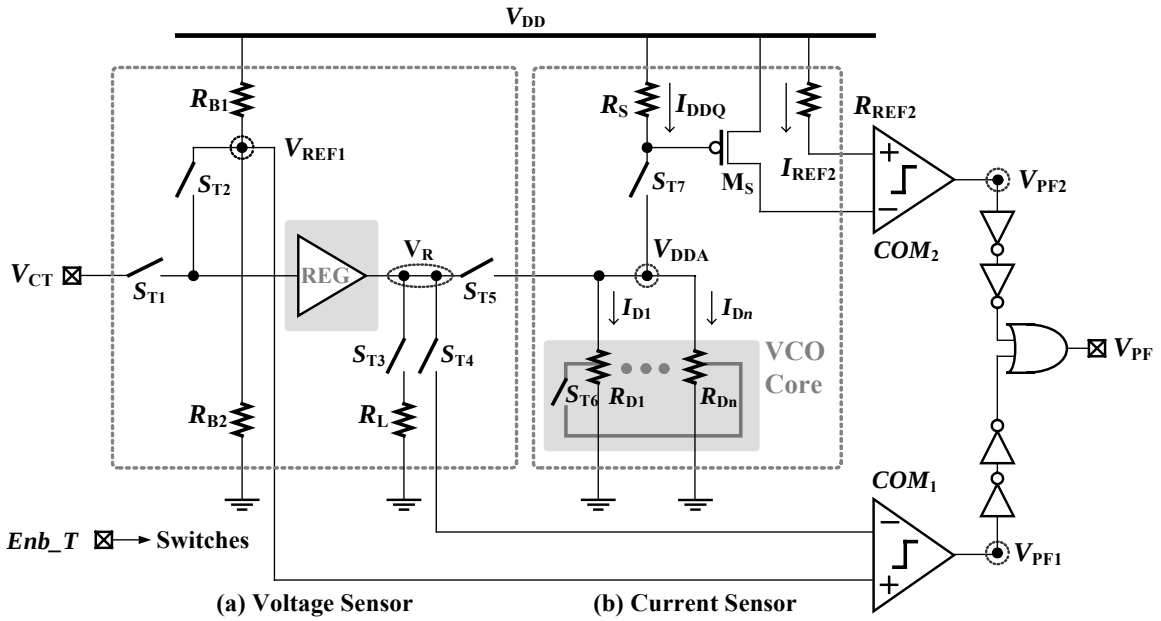



**Fig.5.11.** Circuit diagrams of the built-in voltage and current sensor.

also proposed based on the comparison between the voltage values at each node and the reference voltages using a voltage sensor (*Omayra et al.*, 2003; *Gyvez et al.*, 2005). This $V_{DDQ}$ testing offers internal observability without interrupting power supply system, and high fault coverage can be achieved when multiple nodes are monitored. This work realizes a combined current and voltage testing method as a test strategy applied to the regulated supply tuning current-starved ring VCO through the use of a built-in voltage and current sensor, so called "BIVCS". The voltage testing is applied to the regulator without multiple-node monitoring, while the current testing is applied to the VCO core without interrupting power supply during normal operation mode. Moreover, no extra power supply system is required. Fig. 5.11 shows the circuit diagram of the VCO-under-test and the BIVCS. Voltage and current sensing processes are performed simultaneously when the test enable signal *Enb_T* is high, providing a single test output $V_{PF}$ in a one-bit digital form where "1" and "0" indicate faulty and fault-free status, respectively.

As shown in Fig.5.11 (a), the voltage sensor is based on the concept that the regulator is operating as a buffer, conveying $V_{CT}$ to $V_{DDA}$. When $V_{CT}$ is switched to connect to a constant voltage $V_{REF1}$, the output voltage $V_R$ across the load resistor $R_L$ in steady state is consequently equal to $V_{REF1}$, indicating a fault-free regulator. When $V_R$ is significantly different from $V_{REF1}$, the regulator fails to operate properly and faults are detected. The voltage sensor section comprises three resistors $R_{B1}$, $R_{B2}$, and $R_L$, and a voltage comparator $COM_1$. In test mode, the regulator is removed from the VCO core. The switch $S_{T1}$ and $S_{T5}$ are opened while $S_{T2}$, $S_{T3}$, and $S_{T4}$ are closed, changing $V_{CT}$ to $V_{REF1}$. Subsequently, $V_R$ is compared with $V_{REF1}$ through $COM_1$ for fault detection.

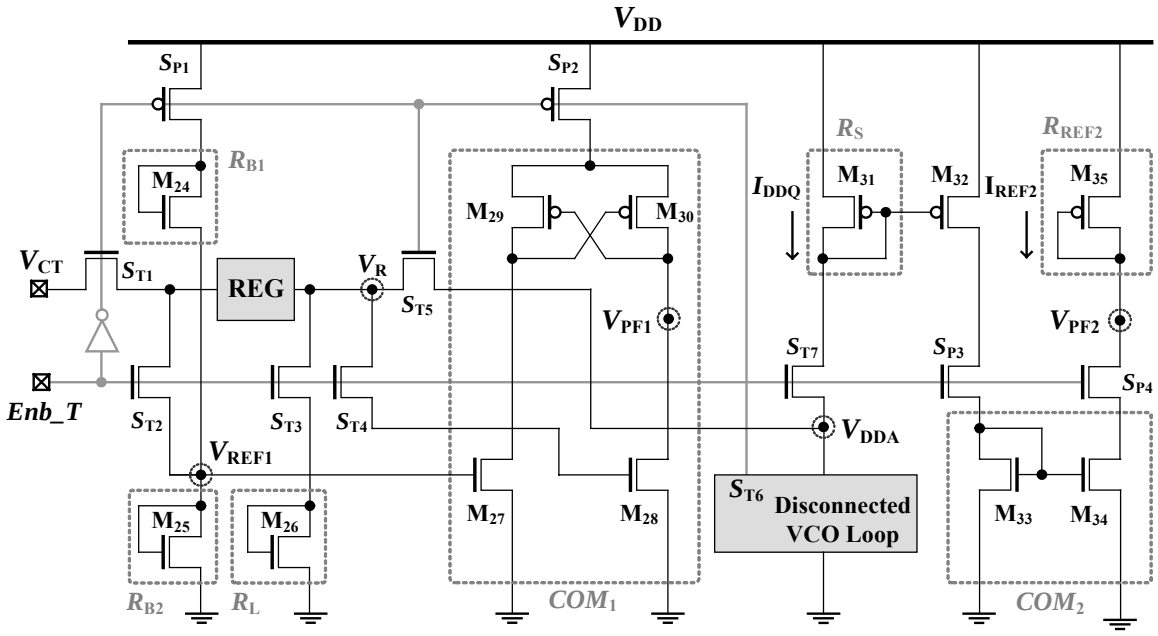



**Fig.5.12.** Circuit implementations of the built-in voltage and current sensor.

As shown in Fig.5.11 (b), the current testing method is based on the concept that faults existed in each delay stage exhibit different values of resistors, i.e. the resistance of potential shorts is 1Ω-10Ω whilst the resistance of potential opens is 1MΩ-10MΩ. This resistance changes the total equivalent resistance in each delay stage, and hence the $I_{DDQ}$ is changed correspondingly. The current sensor consists of sensing resistor $R_S$, a transistor $M_S$, a reference resistor $R_{REF2}$, and a current comparator $COM_2$. In test mode, the switch $S_{T6}$ is opened while $S_{T7}$ is closed, coupling the current sensor to the disconnected VCO loop. The resistor $R_S$ senses the total $I_{DDQ}$ of an $n$-stage VCO where the fault-free $I_{DDQ}$ is given by $I_{DDQ} = I_{D1} + I_{D2}+\ldots+ I_{Dn}$. The resistor $R_{REF2}$ provides $I_{REF2}$, which is typically equal to $I_{DDQ}$, to compare with $I_{DDQ}$ through $COM_2$ for fault detection.

Fig.5.12 shows the circuit implementations of the built-in voltage and current sensor. As the BIVCS is an extra circuit embedded into the VCO for testing purposes, the design of BIVCS realise a compact circuit implementation in order to minimize area using only MOS transistors. As shown in Fig.5.12, resistors $R_{B1}$, $R_{B2}$, and $R_L$ are implemented by diode-connected transistors $M_{24}$, $M_{25}$ and $M_{26}$ respectively. The resistors $R_S$ and $R_{REF2}$ are also implemented by diode-connected transistors $M_{31}$ and $M_{35}$, respectively. The voltage comparator $COM_1$ is a simple differential amplifier formed by $M_{27}$ to $M_{30}$. The current comparator is a simple current mirror formed by $M_{33}$ to $M_{34}$. All associated switches $S_{T1}$ to $S_{T7}$ are implemented by nMOS transistors. In addition, the design of BIVCS also realise the low power consumption issue. Four switches $S_{P1}$ to $S_{P4}$ are facilitated in order to remove the BIVCS from the power supply $V_{DD}$ during normal operation mode, resulting in very low DC power dissipations.

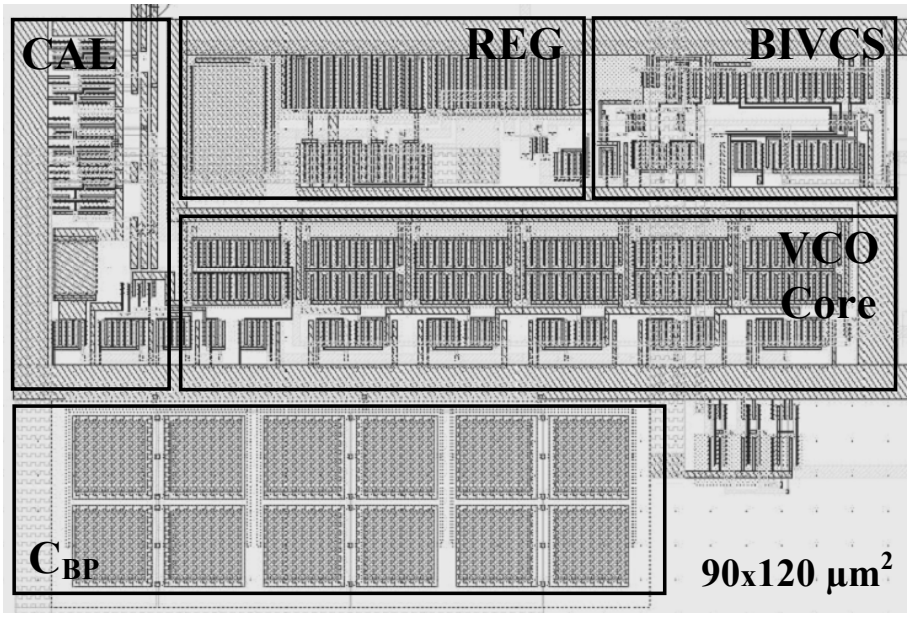



**Fig. 5.13.** Layout diagram of the regulated supply tuning current-starved ring VCO with test and calibration circuit.

## 5.4 Simulation Results and Discussions

The proposed regulated supply tunning current-starved ring VCO with test and calibration circuit was laid out using 0.18-μm CMOS technology and post-layout simulations were carried out through Hspice. Fig.5.13 shows the designed layout diagram with the effective area of 350x460 $\mu m^2$. Table 5.2 summarizes parameter settings as a particular design example. This current-starved ring VCO has 5 stages and operates at a normal supply voltage $V_{DD}$ of 1.8V. The desired frequency range is between 100MHz to 300MHz where the center frequency is 200MHz. The reference currents $I_{REF1}$ and $I_{REF2}$ were set at 10 μA and 94μA, respectively. Calibrating currents $I_{B1}$, $I_{B2,}$ and $I_{B3}$ were set at 6μA, 10μA, and 12μA, respectively. The reference voltage $V_{REF}$ was set at 1.2V.

Firstly, jitter performances during normal oscillation mode at 200 MHz were investigated. Table 5.3 summarizes and compares RMS jitter performances of the VCO with and without the inclusion of the low-pass filter in the regulator. It is seen that RMS jitters in the regulator without the low-pass filter are considerable, i.e. 21.22ps and 65.8ps when supply noises were applied. Meanwhile, RMS jitters in the regulator with the low-pass filter are less than 14.32ps for all cases, indicating the capability of noise suppression. Secondly, the voltage transfer characteristics of the regulator were investigated. Fig. 5.14 shows the simulated oscillation waveform of the VCO. Fig.5.15 shows plots of the control voltage $V_{CT}$ versus the virtual supply voltage $V_{DDA}$ of the low-dropout regulator with the integrated low-pass filter.

**Table 5.2.** Summary of parameter settings.

| Parameters | Values | Units |
|---|---|---|
| Supply Voltage ($V_{DD}$) | 1.8 | V |
| Number of Stages | 5 | Stages |
| VCO Frequency Range | 100 - 300 | MHz |
| $V_{DDA}$ Range | 0.8-1 | V |
| $I_{REF1}$, $I_{REF2}$ | 10, 94 | μA |
| $I_{B1}$ , $I_{B2}$ , $I_{B3}$ | 6,10,12 | μA |
| $V_{REF}$ | 1.2 | V |

**Table 5.3.** RMS Jitter Performance at $f_{OUT}$=200MHz.

| Conditions | Values of RMS Jitter | | Units |
|---|---|---|---|
| | (a) Without LP Filter | (b) With LP Filter | |
| No noises | 7.8 | 10.21 | ps |
| 10-mV, 1-MHz Noise | 21.22 | 13.45 | ps |
| 10-mV, 10-MHz Noise | 65.8 | 14.32 | ps |

It is seen in Fig.5.15 that the regulator yields a linear voltage transfer of $V_{CT}$ to $V_{DDA}$ in the region of 0.6V to 1.5V. Thirdly, frequency calibration was investigated. Fig.5.16 shows plots of the virtual supply voltage $V_{DDA}$ versus the oscillation frequency $f_{OSC}$, demonstrating three frequency ranges in calibration process. The center frequency is 200MHz at $V_{DDA}$ =0.9V. High and low frequency offsets were approximately equal to 22MHz and 20MHz. Lastly, faults were injected into VCO in order to investigate the fault coverage offered by the BIVCS. Faults were modelled by a resistor insertion technique in schematic level based on the extracted circuit parameters. All types of shorts were modelled by connecting a 1-Ω resistor between each pair of terminals. Drain and Source opens were modelled by inserting a parallel combination of a 10-MΩ resistor and a 0.1-pF capacitor in series into each terminal, including Drain and Source opens. Gate opens were particularly modelled by grounded resistor and capacitor at the two disconnecting terminals. Each single fault was injected into the VCO a time while other parameters were kept as normal values. Fig.5.17 shows bar graphs of numbers of injected and detected faults in the VCO core, the regulator and the calibration circuit. The total numbers of injected faults and detected faults are 190 and 159, respectively. The fault coverage is relatively high at 83.68%. It can be considered that shorts were relatively detectable compared to opens due to a small resistor potentially affects the total resistance value.

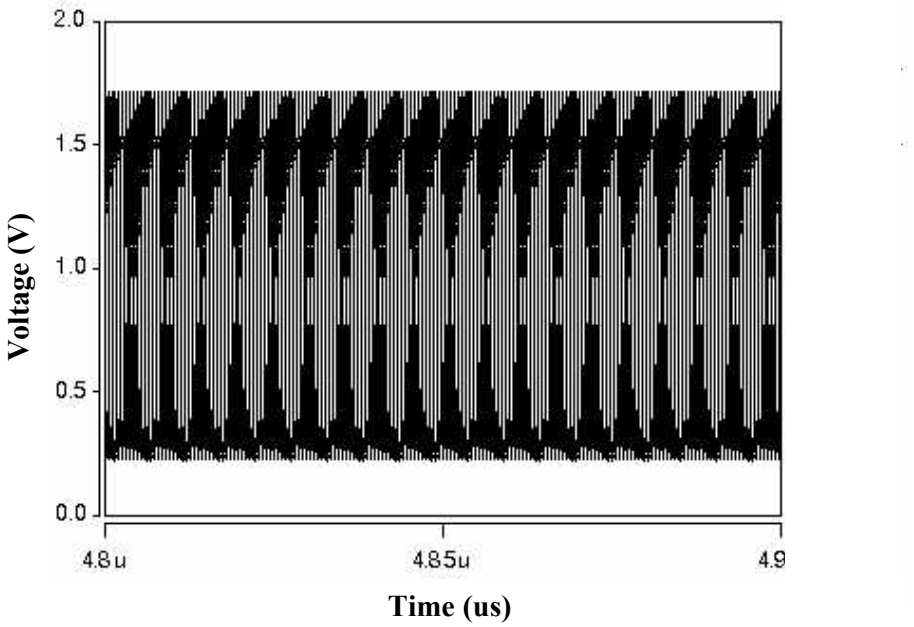



**Fig. 5.14.** The oscillation waveform of the VCO.

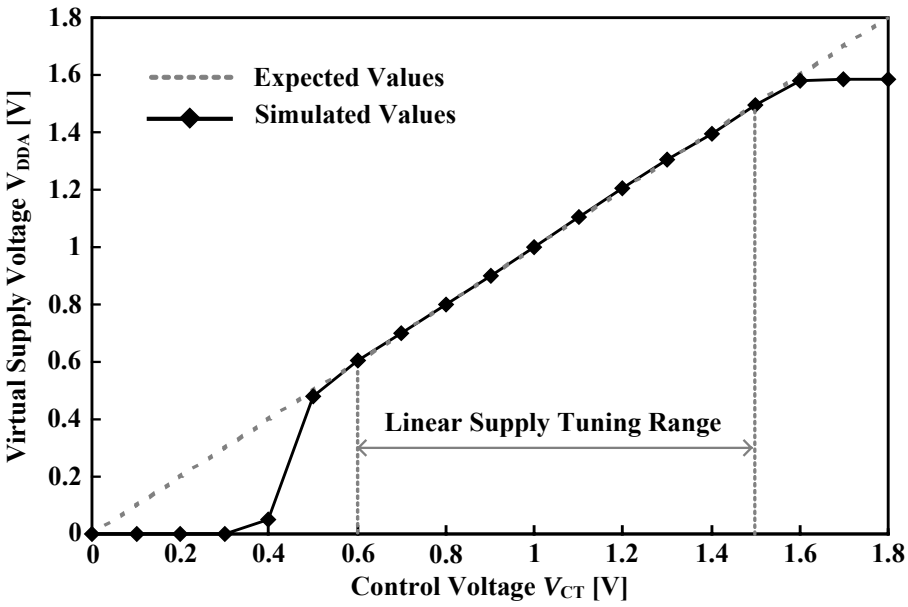



**Fig.5.15.** Plots of the control voltage $V_{CT}$ versus the virtual supply voltage $V_{DDA}$ of the low-dropout regulator.

Based on the design example and simulation results, this technique has attempted to overcome major limitations of VCO, involving the power supply noise injection at high frequency, and test and calibration techniques with low performance penalties. Unlike other calibration techniques where active filters or replica load are required, this technique

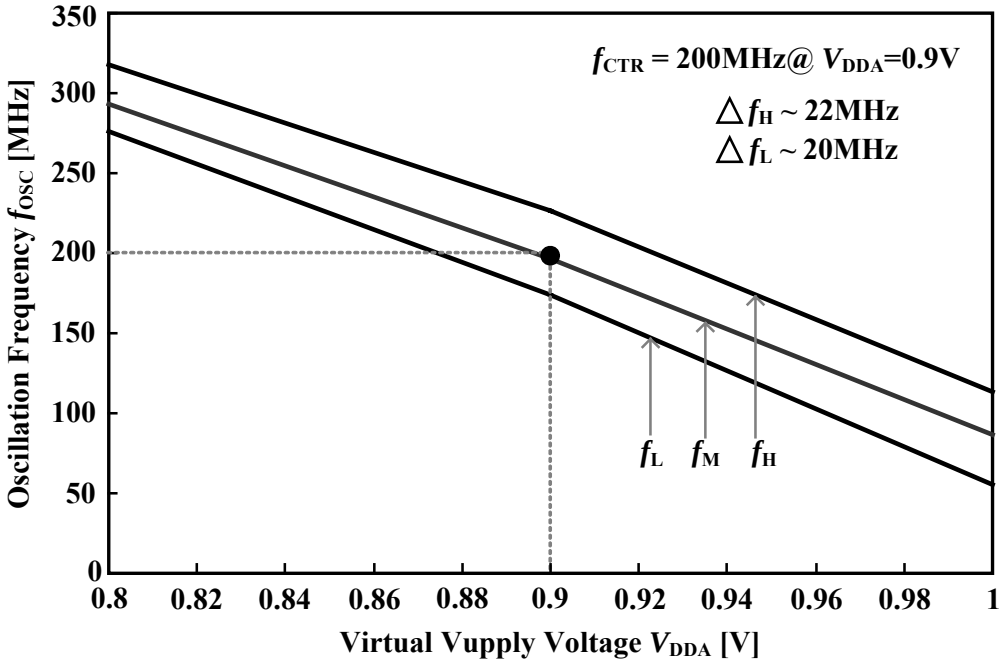



**Fig.5.16.** Plots of the virtual supply voltage $V_{DDA}$ versus the oscillation frequency $f_{OSC}$, demonstrating three frequency ranges.

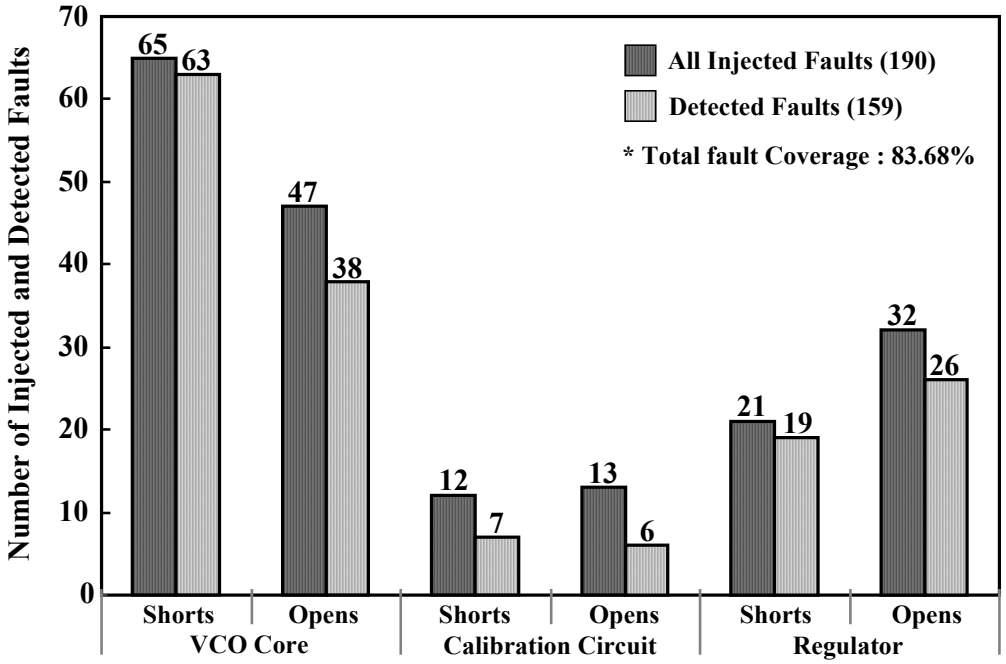



**Fig.5.17.** Numbers of injected and detected faults in the VCO core, the low-dropout regulator and the frequency calibration circuit.

employs a compact low-pass filter for suppressing high-frequency noises, saving chip area and eliminating a complex circuit analysis. The calibration circuit offers both high and low frequency ranges using only 2-bit control signals. Multi-current sources or Multi-capacitor loading are not required since the tuning through current-starved delay cell is separated for

**Table 5.4.** Comparisons of this work and other related BIST techniques for VCO; ×= not reported, SH=Short Fault, OP =Open Fault.

| **Characteristics** | **BIST Techniques** | | |
|---|---|---|---|
| | ***Azais et al.*** **(1998)** | ***Dermentzoglo et al.*** **(2005)** | **This work** |
| **Technology** | CMOS 0.5 μm | CMOS 0.18 μm | CMOS 0.18 μm |
| **Results** | Simulation | Simulation | Simulation |
| **VCO** | 5-stage inverter Ring VCO@155MHz | 8-stage differential Ring VCO@432MHz | 5-stage inverter Ring VCO@200MHz |
| **Techniques** | BIST Only: Inverter Delay Test | BIST Only: Differential output comparison. | BIST+CAL.: Modified Power Supply Regulation |
| **Jitter** | × | × | 13.45ps@10-mV, 1-MHz Noise 14.32ps@10-mV, 10-MHz Noise |
| **Test outputs** | 2 Bits (2 steps) | 1 Bit | 1 Bit |
| **Area Overhead** | 12 % | 18 % | 22 % |
| **Fault Models** | SH: × OP: × | SH: 500Ω OP: × | SH: 1Ω OP: 10MΩ |
| **Fault Coverage** | 100% | 90% | 83.68% |

the frequency tuning through $V_{DDA}$. Table 5.4 summarizes the comparisons of this work to other two obvious BIST techniques for VCOs proposed by Azais et al. (1998) and *Dermentzoglo et al.* (2005). The 5-stage inverter ring VCO at the oscillating frequency of 155MHz by *Azais et al.* (1998) has shown high fault coverage of 100% where no clear faults models were summarized. However, the delay test requires external test equipments for measuring the delay time of a cascade inverter. The 8-stage differential ring VCO at the oscillating frequency of 432MHz was proposed by *Dermentzoglo et al.* (2005). Although this technique offers relatively high fault coverage of 90%, the application is limited to only differential configuration and high area over head of 22% for additional digital circuitry. These two techniques provide only BIST for VCO, and no parametric faults were concerned. This work initially introduces a complete built-in test for oscillator where external test equipments and analysis as are not necessary, providing a pre-screening on-chip testability. The difficulties in this technique are the design of the regulator in which the error amplifier should possess high gain. In addition, the setting of bias currents in the calibration circuit should be designed carefully in order to meet the expected frequency offsets. The fault coverage for catastrophic faults was found at 83.68%. Although this fault

coverage number is lower than other techniques, the over all injected faults was relatively high at 190 faults. The cost for test and calibration facilities is the chip area of approximately 22%. The possible extension includes the application of this VCO in low-jitter PLL designs and the extension of the BVICS technique to test other types of analog circuits.

## 5.5 Conclusions

This chapter has presented the regulated supply-tuning ring VCO with built-in test and calibration. A low dropout regulator with low-pass filter offers inherent noise suppression and the oscillation frequency consequently possesses relatively low jitter performances. Frequency calibration circuit enables the adjustment of three frequency ranges, accommodating parametric faults after fabrications. Built-in voltage and current sensors offer high fault coverage of value 83.68%, verifying on-chip accessibility and observability for the pre-screening of catastrophic faults. Overall circuit designs were demonstrated using a 0.18-μm CMOS technology. This technique can be employed as a low-jitter VCO with fully built-in test and calibration in various mixed-signal circuits such as phase-locked loops and clock-and-data recovery circuits.

# Chapter 6

## Low-Jitter Supply-Regulated Charge Pump Phase-Locked Loop with Built-In Test and Calibration

## 6.1 Introduction

This chapter presents the low-jitter supply-regulated charge pump phase-locked loop (CP-PLL) with integrated BIST and calibration. The chapter initially reviews the CP-PLL architectures, and four related BIST and calibration techniques. In this chapter, the proposed technique employs two independent regulators that provide low-sensitivity supply voltages with inherent noise suppression for analog blocks, and afford multiple reference voltages for test and calibration process. The pre-screening BIST and calibration system based on the deviation of a control voltage during locking state facilitates on-chip accessibility and observability. Demonstrations through simulations and experiments of a 200-MHz CP-PLL demonstrate low-jitter and low supply sensitivity performances with test and calibration functionality.

## 6.2 Reviews on Charge Pump Phase-Locked Loops with Related BIST and Calibration Techniques

### 6.2.1 Basic CP-PLL Architecture

Charge pump phase-locked loops are widely employed as clock generators in a variety of applications including microprocessors, wireless receivers, serial link transceivers, and disk drive electronics. The major reason for the widely adopted use is due to the zero static phase offset, and effective design platforms. The CP-PLL also provides flexible design tradeoffs by decoupling various design parameters such as the loop bandwidth, damping factor, and lock range. Fig.6.1 shows the block diagram of the charge pump phase-locked loop. The block diagram consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF) , a voltage-controlled oscillator (VCO), and a frequency divider.

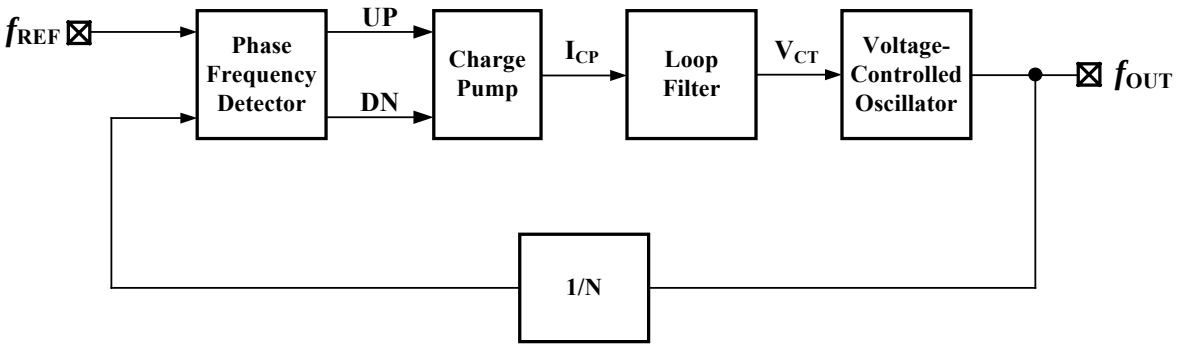



**Fig. 6.1.** Block diagram of the charge pump phase-locked loop architecture.

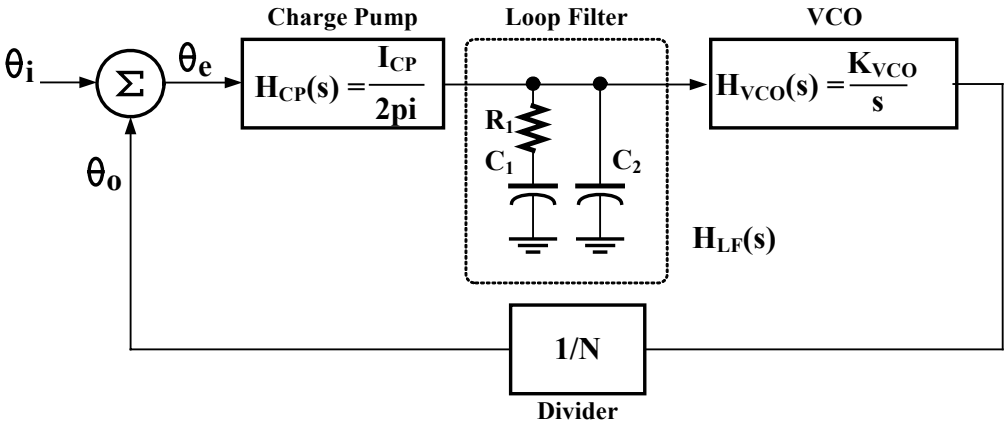



**Fig. 6.2.** Corresponding linear model of the charge pump phase-locked loop architecture.

As depicted in Fig. 6.1, the PFD initially detects the difference in phase and frequency between the reference frequency ($f_{REF}$) and feedback frequency ($f_{REF}$/N), and also generates "UP" or "DN" signals based on whether the feedback frequency is lagging or leading the reference frequency, respectively. These "up" and "down" output signals subsequently control the switches in the charge pump. In the case where the charge pump receives "UP" signal, the current from the charge pump $I_{CP}$ is driven into the loop filter. Conversely, in the case where the charge pump receives the "DN" signal, the current $I_{CP}$ is drawn from the loop filter. The loop filter converts the current $I_{CP}$ to a control voltage $V_{CT}$, which is used to control the VCO. The loop filter filters out jitter by removing glitches from the charge pump and preventing voltage overshoot. Based on this control voltage $V_{CT}$, the VCO oscillates at a higher or lower frequency, which affects the phase and frequency of the feedback frequency. If the PFD produces the UP signal, then the VCO frequency increases. The DN signal decreases the VCO frequency. The VCO stabilizes once the reference clock and the feedback clock have the same phase and frequency.

Fig. 6.2 shows the corresponding linear model of the charge pump phase-locked loop. It can be seen in Fig. 6.2 that the loop filter consists of a resistor $R_1$ in series with a capacitor $C_1$. The charge pump current source and the capacitor $C_1$ form an integrator in

the loop and the resistor introduces a stabilizing zero to improve the phase margin and hence improve the transient response of the CP-PLL. However, the resistor causes a ripple of value $I_{CP}R$ on the control voltage at the beginning of each PFD pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple modulates the VCO frequency and introduces excessive jitter in the output. To suppress the ripple, a small capacitor $C_2$ is added in parallel with the $R$ and $C_1$ network. However, this capacitor introduces a pole, thus increasing the order of the system to three. Therefore, the phase degradation due to this pole has to be accounted for by proper loop parameters.

With reference to Fig. 6.2, the gain of the PFD along with the CP can be described as $I_{CP}/2\pi N$. The transfer function of the loop filter $H_{LF}(s)$ can be derived using linear analysis and is given by

$$H_{\mathrm{LF}}(\mathrm{s}) = \frac{s + \dfrac{1}{RC_1}}{sC_2\left(s + \dfrac{1}{R\left(\dfrac{C_1C_2}{C_1 + C_2}\right)}\right)} \tag{6.1}$$

The VCO is an ideal integrator with gain $K_{VCO}$, and consequently the loop-gain is given by

$$LG(\mathrm{s}) = \frac{K_{\mathrm{VCO}}I_{\mathrm{CP}}}{2\pi\mathrm{N}} \frac{s + \dfrac{1}{RC_1}}{sC_2\left(s + \dfrac{1}{R\left(\dfrac{C_1C_2}{C_1 + C_2}\right)}\right)} \tag{6.2}$$

It can be considered from (6.1) that the system has zero and pole as follows;

$$\omega_{\mathrm{Z}} = \frac{1}{RC_1} \tag{6.3}$$

$$\omega_{\mathrm{P}} = \frac{1}{R\left(\dfrac{C_1C_2}{C_1 + C_2}\right)} \tag{6.4}$$

The phase margin degradation due to the pole is mathematically expressed by

$$\Phi_M = \arctan\left(\frac{\omega_{UGB}}{\omega_Z}\right) - \arctan\left(\frac{\omega_{UGB}}{\omega_P}\right) \tag{6.5}$$

An optimal choice of the capacitor ratio $C_1/C_2$ leads to a phase margin that is relatively immune to process variations. The maximum phase margin can be calculated by equating the first derivative of $\Phi_M$ to zero. It can be shown that the maximum phase margin occurs when

$$\omega_{UGB} = \omega_Z\sqrt{\frac{C_1}{C_2}+1} \tag{6.6}$$

Substituting (6.6) into (6.5) yields

$$\Phi_M = \arctan\left(\sqrt{\frac{C_1}{C_2}+1}\right) - \arctan\left(\frac{1}{\sqrt{\frac{C_1}{C_2}+1}}\right) \tag{6.7}$$

$$C_1 = 2C_2(\tan^2\Phi_M - \tan\Phi_M\sqrt{\tan^2\Phi_M+1} \tag{6.8}$$

Equation (6.8) describes the relationship between the two capacitors that place the zero and the pole so as to yield a robust phase margin. The loop bandwidth and phase margin are mandated by the application. For example, in the case of clock generators with a poor phase noise VCO and a pure low-frequency reference, a relatively high bandwidth is required, while some optical standards require a low loop bandwidth and a large phase margin to avoid any jitter peaking. For a given loop bandwidth and phase margin, the three variables $C_1$, $C_2$, and $I_{CP}$ can be calculated using (6.5)–(6.8) while noting unity loop-gain. The loop filter resistance is typically chosen based on noise and area constraints. The closed-loop transfer function for typical CP-PLL design is finally given by

$$\frac{\theta_O(s)}{\theta_i(s)} = \frac{K_{VCO}I_{CP}}{2\pi C_2}\left(\frac{s+\frac{1}{RC_1}}{s^3+\left(\frac{1}{R\frac{C_1C_2}{C_1+C_2}}\right)s^2+\frac{K_{VCO}I_{CP}}{2\pi C_2}s+\frac{K_{VCO}I_{CP}}{2\pi RC_1C_2}}\right) \tag{6.9}$$

**Table 6.1.** Summary of related BIST and calibration techniques for CP-PLLs.

| Authors | Years | CUTs | BIST and Calibration Techniques |
|---|---|---|---|
| (a) *Burbridge et al.* | 2003 | CP-PLL | Digital only ramp-based BIST technique |
| (b) *Lung Hsu et al.* | 2005 | CP-PLL | Re-configuration PLL BIST technique |
| (c) *Lin and Lai* | 2007 | CP-PLL | Period measurement calibration technique |
| (d) *Hsu and Su* | 2008 | CP-PLL | Time-to-digital based BIST technique |

### 6.2.2 Related BIST and Calibration Techniques for CP-PLLs

With reference to the design of CP-PLL described in Section 6.2.1, a number of the extension of CP-PLL with BIST and calibration has recently been proposed. As for purpose of demonstrations, Table 6.1 summarizes four particularly related BIST and calibration techniques for CP-PLLs, involving *Burbridge et al.* (2003)*, Lung Hsu et al.* (2005)*, Lin and Lai* (2007)*,* and *Hsu and Su* (2008)*.*

As shown in Table 6.1(a), *Burbridge et al.* (2003) proposed the digital only ramp-based BIST technique for CP-PLL. This technique employs a ramp output response to detect faults in analog path through the frequency counting in accordance to the acceptable frequency tolerance band. Fig. 6.3 shows the test architecture in which the most important part of the Input MUX design is ensuring that delays are matched for the signal paths in operational mode and test mode. Careful matching of the delays will help to mitigate any constant offset errors that will affect measurement accuracy, and most importantly will ensure that test circuitry does not adversely effect the PLL operation. As shown in Fig.6.3, there are three input ports (A, B, C) and two output ports (D, E) of the input multiplexer. Using the MUX connections in conjunction with suitable sequencing will allow comparison of counted output frequencies ($F_1$–$F_4$) against expected results. The test procedures are performed in five steps. Firstly, the test step 1 connects D and B ports as well as E and C ports. This step 1, if the feedback divider is set to its maximum setting, $F_{out}$ will be at a maximum. Enforcing this requirement for the test will ensure that all of the PLL components are exercised at maximum operational speed, after this, simple functional tests will be adequate for feedback divider testing. Secondly, the test step 2 is a “Ramp Down” test mode that connects D and A ports as well as E and B ports. This step 2 allows the measurement for the nonlinearity of the Gain of forward path. Thirdly, the test step 3 is a “Hold Mode” that connects D and B ports as well as E and B ports. This step allows the CP-PLL to be ready for the text in the next step and no measurement is performed. Fourthly, the test step 4 is a “Ramp Up” Mode that connects D and B ports as well as E and A ports. This step 4 provides a multi-functional test including, the gain of the forward path,

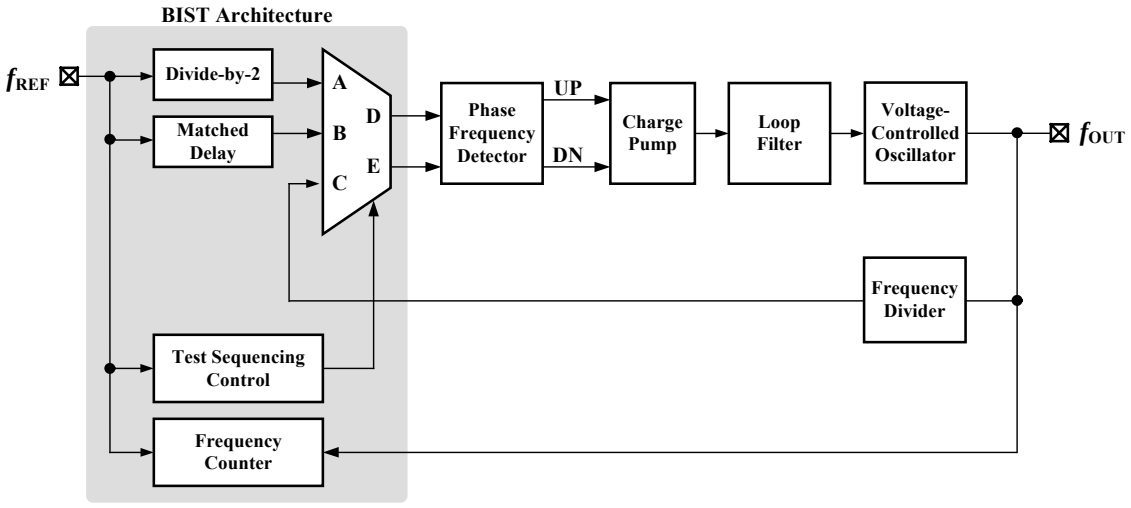



**Fig. 6.3.** BIST architecture for CP-PLL proposed by *Burbridge et al.* (2003).

VCO nonlinearity, and charge pump mismatch. Finally, the test step 5 is another "Hold Mode" that connects D and B ports as well as E and B ports. This mode also allows possibility to test the loop filter leakage, charge pump leakage, and excessive phase offsets in the forward path. This technique is relatively simple with digital only, minimally invasive and fully automated test approach for high performance CP-PLL that can be used to provide more information about the CP-PLL function

As shown in Table 6.1(b), *Lung Hsu et al.* (2005) alternatively proposed the BIST structure of a CP-PLL that can identify possible faults in all blocks such as the phase detector, charge pump, loop filter, voltage-controlled oscillator and divide-by-N blocks. The key idea of this approach is the use of all existing blocks in PLL for measuring and testing, which reduce the chip area overhead. The proposed approach does not alter any existing analog circuits, but only adds some small circuits to the PLL and requires a slight modification of the digital part. Fig. 6.4 shows the BIST architecture for CP-PLL proposed by *Lung Hsu et al.* (2005) where two multiplexers (MUXs), and three delay cells are added to an existing PLL. When the BIST system is active, the control unit controls the MUXs to provide appropriate stimulus for the PLL. The control unit comprises two blocks, i.e. the test-control and fault-evaluation circuits. The test-control circuit provides two signals; Enable Test (ENT) and Charge-Discharge Test (CDT). The fault-evaluation circuit utilizes digital outputs from the DBN at the rising edge of the fault-evaluation clock, and evaluates the fault at the test output. This BIST structure has two operating modes normal and test. In the normal mode, the MUXs are set to bypass the input and feedback signals. However, the MUX provide test patterns from the input of the PLL during the test mode. In the test mode, the BIST structure employs the charge pump as a stimulus generator and employs the VCO and DBN as measuring devices for testing. The MUXs provide test signals generated by

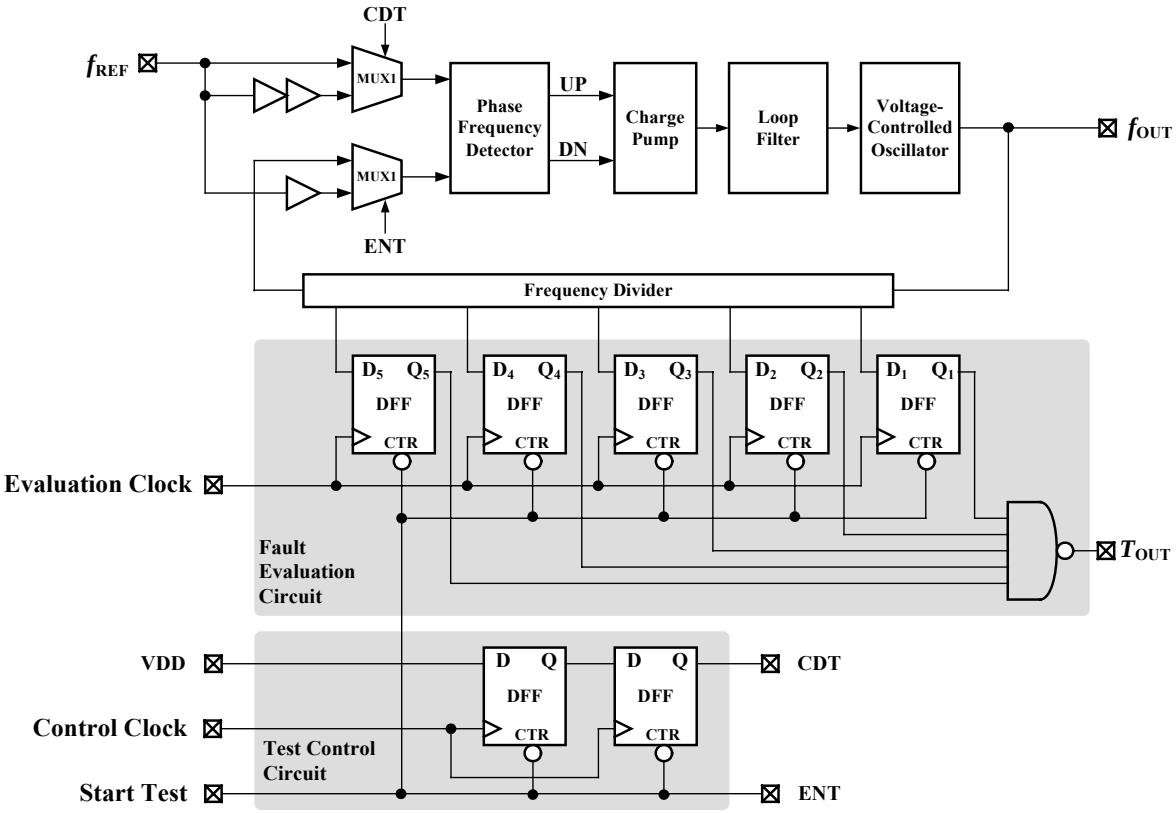



**Fig. 6.4.** BIST architecture for CP-PLL proposed by *Lung Hsu et al.* (2005).

the test-control circuit to the phase-detector input, and the VCO subsequently oscillates depending on the output voltage of the loop-filter. The oscillation frequency reflects faults in each PLL block. The deviation of the oscillation frequency from its nominal value indicates a faulty circuit in the loop. Additionally, the oscillation frequency is measured on-chip using the existing divider block, which operates as a counter and does not need any external clock. The output is a pure digital value, increasing the reliability of outputs.

As shown in Table 6.1(c), *Lin and Lai* (2007) proposed the calibration method that accomplishes efficient search for an optimum VCO discrete tuning curve among a group of frequency sub-bands. The agility is attributed to this proposed frequency comparison technique, which is based on measuring the period difference between two signals. Fig. 6.5 shows the calibration architecture for CP-PLL proposed by *Lin and Lai* (2007). As shown in Fig.6.5, the reference frequency is divided into 8 phases, i.e. 45-degree difference, through three divide-by-2 internal sub blocks. These 8-phase signals are subsequently sent to the phase selector. The phase selector improves voltage comparison precision, thereby also improving the frequency calibration accuracy. The phase difference must not be too small to drive the charge pump working near the dead-zone region. Since the initial phase relationship (lead or lag) and the amount of phase difference between two inputs are not known, this phase selector circuit ensure both conditions are properly determined. The dual

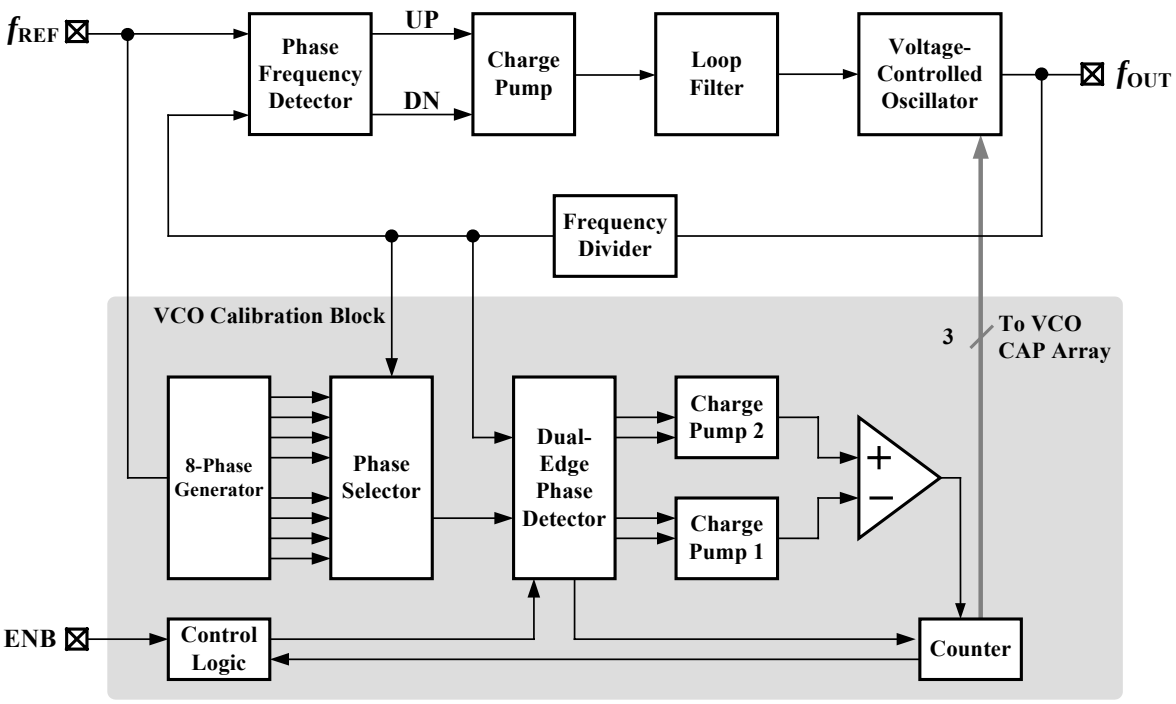



**Fig. 6.5.** Calibration architecture for CP-PLL proposed by *Lin and Lai* (2007).

phase detector, consisting of two phase-frequency detectors, performs frequency comparison by examining only one pair of rising edges and one pair of falling edges between two signals. For a large frequency difference, the phase relationship may deviate from the typical performances. The deviation is subsequently transferred to two charge pumps. The reason for adding this charge pump is due to the switching activities of the charge pump circuit, i.e. alternating UP and DN currents, and therefore the voltage has an undesired switching component superimposed on top of the desired charging and discharging currents. Duplicating the same charge pump in the path essentially forms a pseudo-differential topology, such that these dynamic switching non-idealities can be suppressed. Similarly, the effects of power supply noise coupling or substrate noise pickup are also reduced. Time to voltage conversion is performed through the comparator. The output is a 3-bit signal, which is subsequently sent to calibrate the capacitor values in the VCO with switchable triode transistor array. This proposed relative-period-based calibration technique method requires only a few signal cycles to complete one frequency comparison, and therefore calibration time is relatively fast.

As shown in Table 6.1(d), *Hsu and Su* (2008) proposed the time-to-digital based BIST technique that measures the clock jitter of the CP-PLL. The jitter-measurement structure is based on a novel time-to-digital converter (TDC), which has a high resolution. A small area overhead is also achieved using the voltage-controlled oscillator and the loop filter of the PLL under test as parts of the TDC. The TDC detects each phase difference

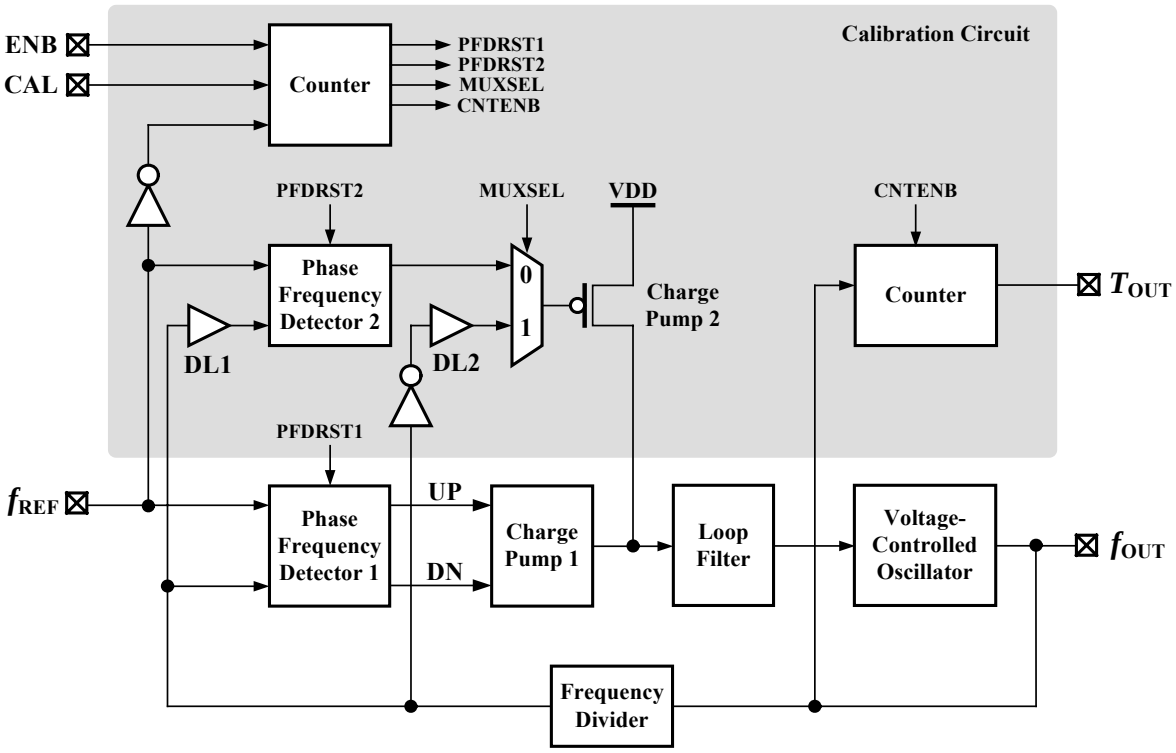



**Fig. 6.6.** BIST architecture for CP-PLL proposed by *Hsu and Su* (2008).

between the reference clock and the clock under test to obtain the histogram of the jitter. Fig. 6.6 shows the BIST architecture for CP-PLL proposed by *Hsu and Su* (2008). It is seen in Fig. 6.6 that the BIST circuit comprises three main parts, including TDC, control unit, and calibration circuit. The TDC is composed of delay buffer1, PFD2, MUX, CP2, loop filter, VCO, and DIV. The loop filter, VCO, and DIV are also parts of the PLL under test. The TDC structure is modified to simplify the calibration process and to enlarge the current capacity. The CP2 is designed as a single switch that is controlled using the signal. The control unit is the finite-state machine using CLK0 as its clocking signal. The calibration circuit calibrates the coefficient of the measurement resolution, which is determined by the parameters of the charge pump current of the CP2, the equivalent capacitance of the loop filter, and the VCO gain. The calibration circuit is composed of the VCO, DIV, delay buffer2 (DL2), MUX, CP2, and loop filter. Using the clock period of VCO as the reference yields an accurate pulse width to calibrate the TDC. The DIV is modified to yield a pulse width that equals the clock period of the VCO. In the calibration mode, the control signal MUXSEL changes to a logic high to allow the DIV output signal to pass through the MUX. The pulse signal is input to CP2, and changes the voltage of the loop filter and hence the frequency of the VCO. The pulse width is the clock period of the VCO, and the counted frequency value of the counter can be obtained. The clock period of the VCO varies, which is known as the period jitter. Repeating the calibration process a particular number of times produces a histogram for BIST results.

## 6.3 Proposed Supply-Regulated Charge Pump PLL with Test and Calibration System

Power supply regulation techniques have recently been suggested to PLLs for suppressing power supply noises. The techniques proposed by *Ingino et al.* (2001) and *Sun* et al. (2008) employ regulators to provide power supply voltages for both charge pump circuit and VCO. These techniques minimize power supply noises with the expense of a complex frequency compensation circuit. Alternatively, the technique by *Alon et al.* (2006) inserts a regulator into PLL closed-loop as a frequency control element. The oscillation frequency is varied corresponding to a regulated supply voltage, and supply noises are inherently minimized. However, the insertion of a regulator into a closed-loop may lead to design complexity due to a critical stability of the overall loop. As particularly described in Section 6.2.2, BIST and calibration techniques for CP-PLLs have gained attention to detect catastrophic faults and to accommodate parametric variations, especially in scaling CMOS technology. However, those techniques require much additional hardware and the operations are relatively complicated.

Consideration of these supply regulation, BIST and calibration techniques points to the possible exploitation of a power supply regulation system that offers both power supply noise suppression, test and calibration purposes. This section therefore alternatively presents an integrated power supply regulation system in a CP- PLL that offers power supply noise suppression and facilitates built-in test and calibration system. The key idea is the use of two independent regulators for charge pump circuit and the VCO. One regulator used in charge pump circuit filters out low-frequency supply noises, and provides reference voltages for charge pump power supply, charge pump current setting, and voltage references in test and calibration system. Another regulator used in VCO filters out high-frequency supply noises, and provides reference voltages for VCO power supply and frequency tuning operations.

### 6.3.1 System Descriptions

Fig.6.7 shows the proposed supply-regulated charge pump PLL with the built-in test and calibration system. The typical configuration comprises five components; phase-frequency detector (PFD), CP circuit, loop filter (LF), VCO, and frequency divider (DIV). This work implements an integrated power supply regulation with test and calibration system by adding four components, i.e. the voltage reference generator, two regulators $REG_1$ and $REG_2$, and the test and calibration circuit. First, the voltage reference generator provides precise and stable voltages $V_{REF}$ for use in $REG_1$ and $REG_2$. Second, $REG_1$ provides separated DC voltages $V_{CP}$ and $V_{DDA}$ for the CP circuit, and also affords

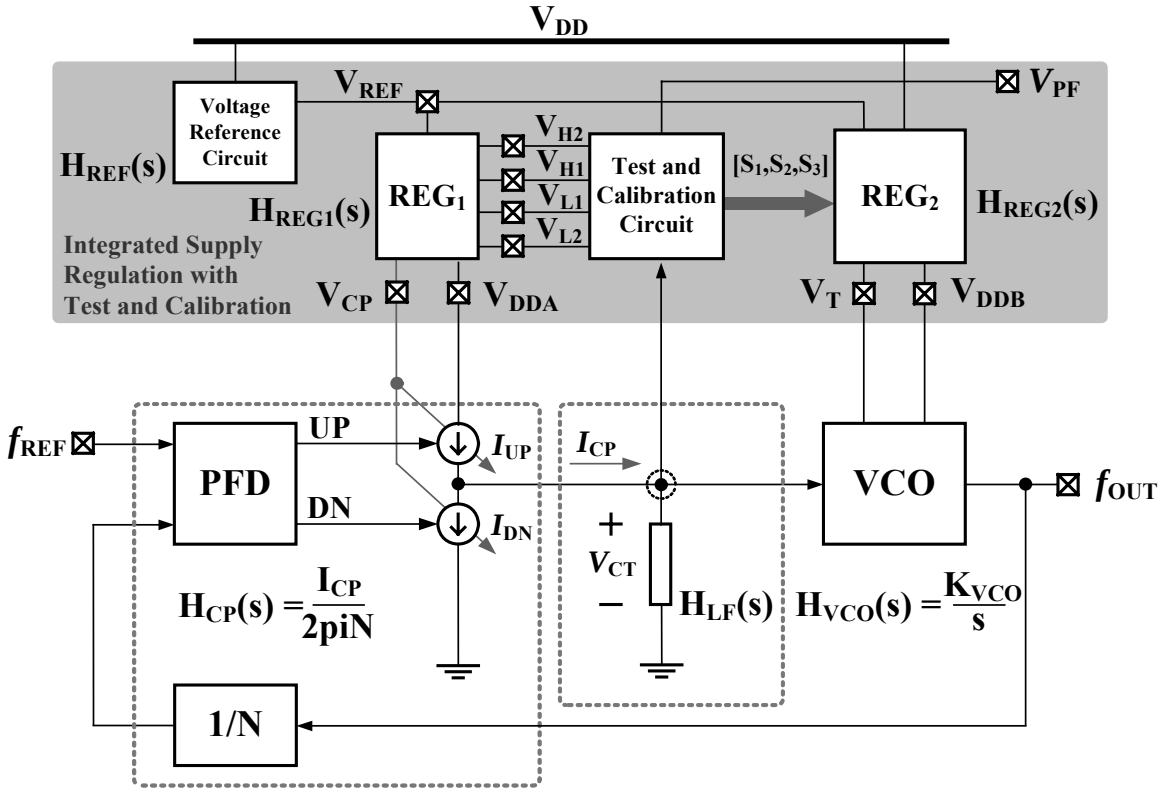



**Fig.6.7.** Block diagram of the proposed supply-regulated charge pump PLL with built-in test and calibration system.

four reference voltages $V_{L1}$, $V_{L2}$, $V_{H1}$, and $V_{H2}$ for the test and calibration circuit. The closed loop transfer function of the output phase to the power supply noises contributed through the CP circuit can be expressed as

$$\Phi_{CP}(s) = \left( \frac{I_{CP} H_{LF}(s) H_{VCO}(s)}{1 + LG(s)} \right) H_{REG1}(s) V_{DD}(s) \tag{6.10}$$

where $LG(s) = H_{CP}(s)H_{LF}(s)H_{VCO}(s)$ is an open-loop gain. It is seen in (6.10) that both transfer functions of CP and LF circuits, which exhibit low-pass characteristics (*Ring and khrishnan*, 2008), are involved, allowing low-frequency noises to be appeared at the output phase. Therefore, the power supply rejection (PSR) characteristic of $H_{REG1}(s)$ assists low-frequency noise suppression. Third, the regulator $REG_2$ provides DC voltages $V_T$ and $V_{DDB}$ for the VCO. The closed loop transfer function of the output phase to the power supply noises contributed through the VCO can also be expressed as

$$\Phi_{VCO}(s) = \left( \frac{H_{VCO}(s)}{1 + LG(s)} \right) H_{REG2}(s) V_{DD}(s) \tag{6.11}$$

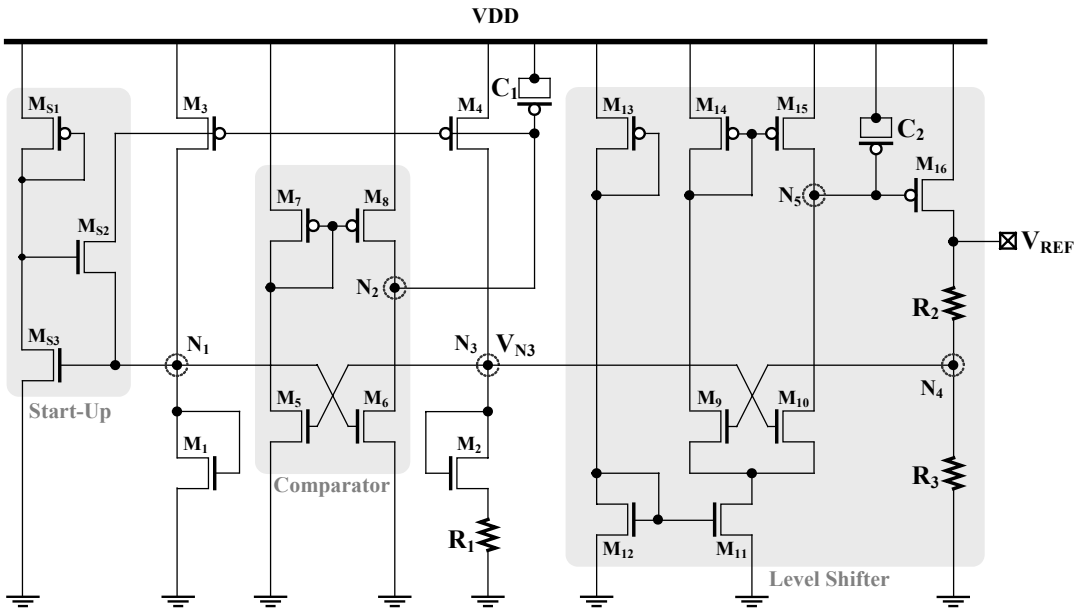



**Fig.6.8.** Beta-multiplier-based CMOS voltage reference generator.

It is seen in (6.11) that $H_{VCO}(s)$ exhibits a high-pass characteristic and dominates the transfer function, allowing high-frequency noises to be appeared at the output phase. Consequently, $H_{REG1}(s)$ can be designed in order to suppress high-frequency noises.

### 6.3.2 On-Chip CMOS Voltage Reference Generator

Fig.6.8 shows the circuit configuration of the Beta-multiplier-based voltage reference circuit. Basically, the Beta-multiplier-based voltage reference circuit consists of two diode-connected transistors $M_1$ and $M_2$, where the transistor $M_2$ has a resistor $R_1$ at the source terminal and a larger effective width compared to $M_1$ in order to provide a constant voltage at node $N_3$. The start-up circuit, comprising transistors $M_{S1}$ to $M_{S3}$, is also necessary for sustaining optimal initial and normal operating states. However, two major difficulties of this typical configuration include high power supply sensitivity caused by output resistances of $M_2$ and $M_4$, and a small value of reference voltage, i.e. $V_{REF1} \leq V_{DD}/2$. In order to reduce the poser supply sensitivity, the comparator, consisting of $M_5$ to $M_8$, was therefore included. This comparator compares and regulates two voltages at nodes $N_1$ and $N_2$ to be equal, resulting in better power supply sensitivity. As the comparator introduces the positive feed back loop, the PMOS capacitance $C_1$ was necessarily included for enhancing the stability and avoiding undesirable oscillation of drain currents. In addition to the power supply sensitivity reduction, a level shifter, i.e. a non-inverting amplifier formed by transistors $M_9$ to $M_{15}$ and a pass transistor $M_{16}$, was included for adjusting $V_{REF}$ to the desired value. The output reference voltage $V_{REF}$ can be achieved by setting the value of resistors $R_2$ and $R_3$ through voltage division.

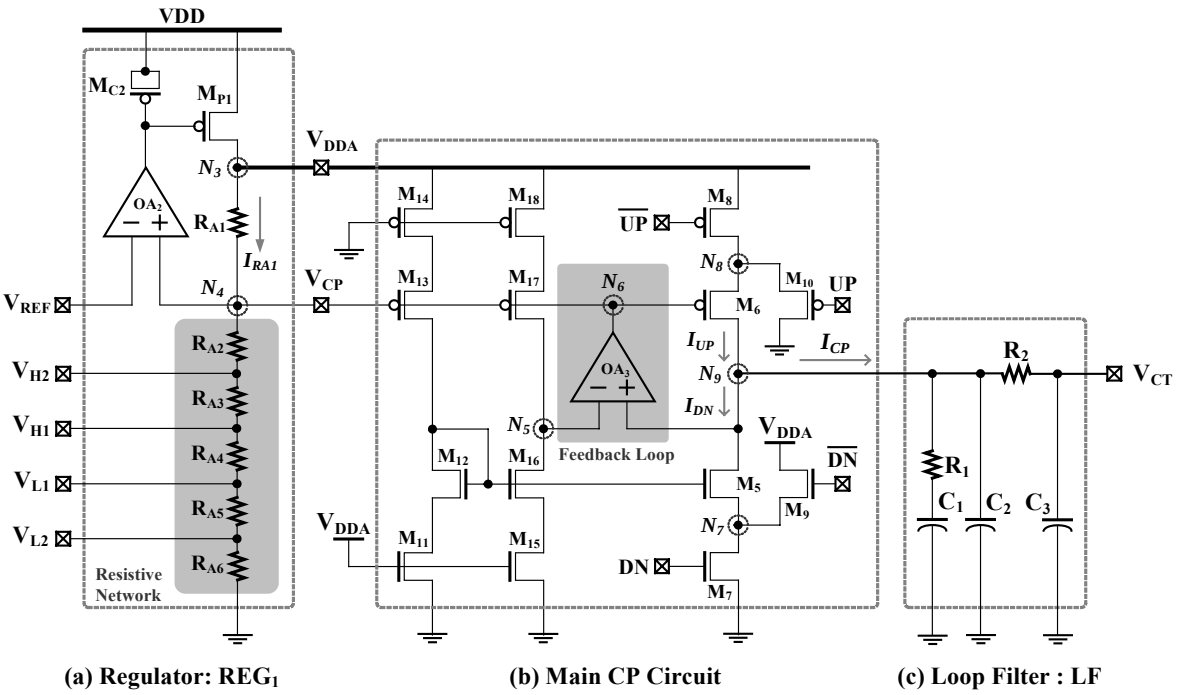



**Fig.6.9.** Circuit configuration of the supply-regulated CP and LF circuits.

### 6.3.3 Supply-Regulated Charge Pump Circuit and Loop Filter

A charge pump circuit converts the outputs of the PFD into a current signal. Fig. 6.9 shows the supply-regulated CP circuit, comprising $REG_1$, the main CP circuit, and the loop filter. As shown in Fig.6.9 (a), $REG_1$ consists of an amplifier $OA_2$, a pass transistor $M_{P1}$, a capacitance $M_{C2}$, and six resistors $R_{A1}$ to $R_{A6}$. The DC and AC characteristics of $REG_1$ afford four particular functions. First, $REG_1$ provides an independent power supply voltage $V_{DDA}$ at node $N_3$. Since the feedback loop regulates the voltage at node $N_4$ to be equal to $V_{REF}$, a current $I_{RA1}$ is constant at steady state. Therefore, the constant $V_{DDA}$, which is greater than the limited value of $V_{REF}$, is equal to $V_{DDA} = R_{A1}I_{RA1}+V_{REF}$, and can be set through the appropriate value of $R_{A1}$. Second, $REG_1$ also provides a biasing voltage $V_{CP}$ that sets the operating charge pump currents $I_{UP}$ and $I_{DN}$, and hence no additional biasing circuit is required. Third, four reference voltages $V_{L1}$, $V_{L2}$, $V_{H1}$and $V_{H2}$, which are exploited for the test and calibration circuit, can be obtained through voltage division in the resistive network formed by $R_{A2}$ to $R_{A6}$. Last, the AC characteristic of $REG_1$ suppresses low-frequency power supply noises when the moderate frequency of the PSR is greater than corner frequencies of those low-pass transfer functions of CP and LF circuits.

As shown in Fig. 6.9 (b), the main CP circuit consists mainly of two current sources $M_5$ and $M_6$, and two main switches $M_7$ and $M_8$, which are shifted to ground and power supply, respectively, in order to reduce direct charge injection at the output node $N_9$.

Additional switches $M_9$ and $M_{10}$ are included for eliminating remaining channel charges that transfer to nodes $N_7$ and $N_8$ when the main switches change from saturation mode to cut-off mode. Nonetheless, most CP circuits generally suffer from a current mismatch caused by channel length modulation effects. The current mismatch causes control voltage fluctuations in the locking state, resulting in a large amount of phase noises with spurs. The current mismatch compensation using a feedback loop through the amplifier $OA_3$ was therefore included in order to regulate the voltages between nodes $N_5$ and $N_9$ to be equal, yielding nearly matched currents $I_{UP}$ and $I_{DN}$. In this circuit, the main biasing branch is formed by $M_{11}$ to $M_{14}$, and biasing branch for current mismatch compensation is formed by $M_{15}$ to $M_{18}$. The loop filter shown in Fig. 6.9 (c) converts a charge pump current into a control voltage with noise filtering. This LF is a cascade connection of the 2$^{nd}$-order and 1$^{st}$-order sections. The low-frequency pole formed by $R_1$ and $C_1$ sustains the PLL loop stability. The capacitor $C_2$ prevents voltage jumps caused by $I_{CP}R_1$ at the input of the VCO. The high-frequency pole set by $R_2$ and $C_3$ reduces the spurs caused by control voltage fluctuations.

### 6.3.4 Supply-Regulated Current-Starved Ring VCO with Frequency Tuning Technique

The VCO typically provides an output oscillation frequency $f_{OUT}$ corresponding to the input control voltage $V_{CT}$. Fig.6.10 shows the supply-regulated current-starved ring oscillator with frequency tuning transistors. As shown in Fig. 6.10 (a), $REG_2$ was exploited for reducing power supply sensitivity and suppressing high-frequency power supply noises. This $REG_2$ consists of an amplifier $OA_2$, a pass transistor $M_{P2}$, a capacitance $M_{C3}$, and five resistors $R_{B1}$ to $R_{B5}$. The DC and AC characteristics of $REG_2$ offer two functions. First, $REG_2$ provides an independent power supply voltage $V_{DDB}$ at node $N_{10}$ for the VCO in the similar manner to $REG_1$. A low-pass filter, consisting of $R_B$ and $C_B$, are included in order to filter high-frequency noises contributing from $V_{DD}$ to $V_{DDB}$. As mentioned earlier, this additional low-pass filter is necessary since the VCO transfer function possesses a high-pass characteristic, allowing high-frequency noises to be appeared at the output phase. Second, $REG_2$ also provides reference voltages $V_{TN1}$, $V_{TN2}$ and $V_{TN3}$ for the VCO through voltage division in the resistive network formed by $R_{B2}$ to $R_{B5}$. As particularly demonstrated in Fig. 6.10 (b), a typical current-starved delay stage consists mainly of an inverter formed by $M_{25}$ and $M_{26}$. The transistor $M_{19}$ performs voltage-to-current conversion, supplying bias currents $I_N$ and $I_P$ for the inverters through $M_{20}$ to $M_{24}$. The output frequency for $n$ of identical stages is given by $f_{OUT} = I_{CT}/(nC_TV_{DDB})$ where $I_{CT}$ is a common bias current, i.e. $I_{CT} = I_N = I_P$, and $C_T$ is a total intrinsic capacitance at the output node $N_{13}$. With a given number of $n$ stages, it can be considered that $f_{OUT}$ can be tunned through three

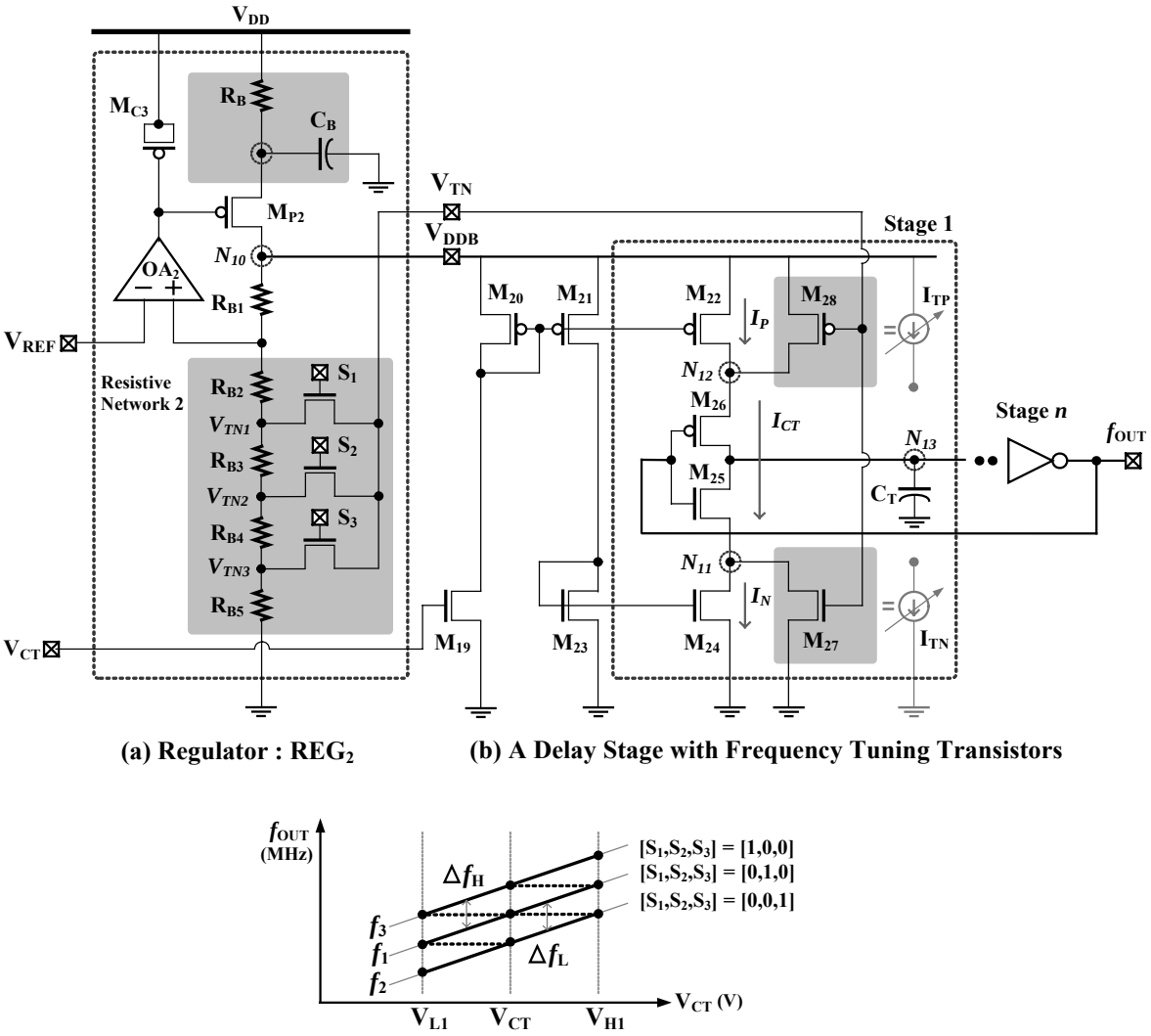
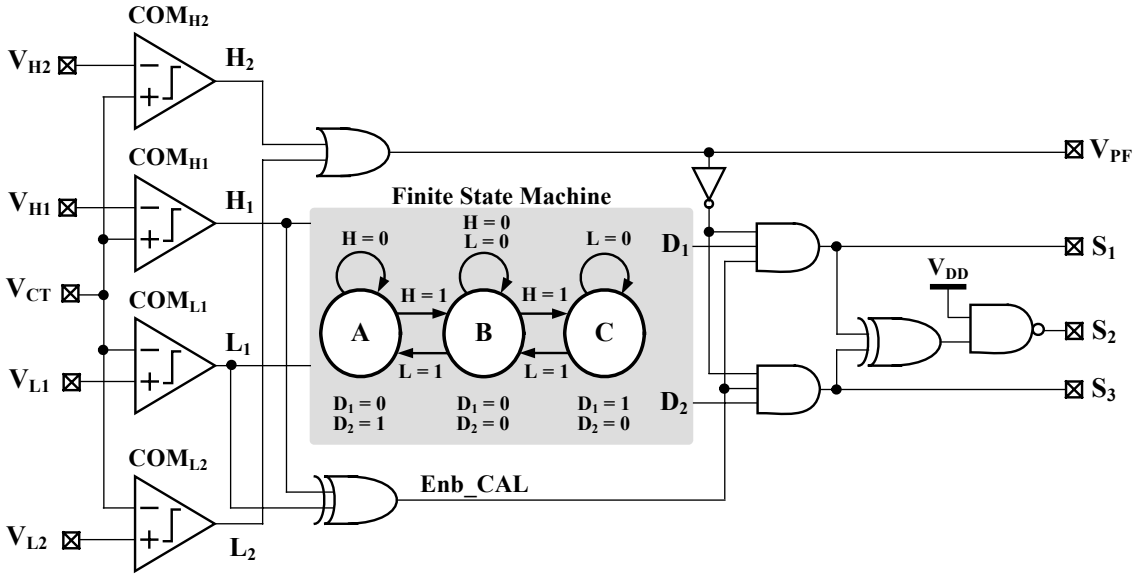
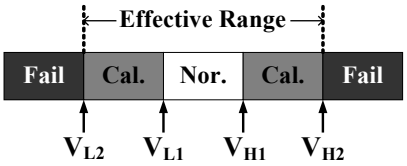



**Fig.6.10.** Circuit configuration of supply-regulated current-starved ring oscillator with the frequency tuning transistors.

parameters, i.e. $C_T$, $V_{DDB}$ and $I_{CT}$. Avoiding additional capacitances and changes in $V_{DDB}$, tunning the *VCO* through $I_{CT}$ was realised by introducing two current sources formed by $M_{28}$ and $M_{27}$ in parallel to $M_{22}$ and $M_{24}$, respectively. Upon setting appropriate transistor widths of $M_{27}$ and $M_{28}$, the additional currents $I_{TP}$ and $I_{TN}$, which are controlled by a single voltage $V_T$, are nearly identical. Consequently, the new oscillation frequency can be described as $f_{OUT}=I'_{CT}/(nC_TV_{DDB})$ where $I'_{CT}= I_P+I_{TP}= I_N+I_{TN}$. Changing $V_T$ results in the change in $I'_{CT}$, and hence tunning oscillation frequency is attainable. Three different values of $V_T$ can be obtained from $REG_2$ through an analog multiplexer. Linear frequency offset ranges are achievable with low current variations since $V_T$ is stable.




**(b) Block diagrams of Test and Calibration Circuit**




**(a) Voltage Margins for Test and Calibration**

**Fig.6.11.** Circuit diagram of the test and calibration circuit.

Fig. 6.10 (c) illustrates a zigzag-tuning characteristic of the VCO using three control bits $S_1$, $S_2$ and $S_3$. Low and high voltage margins, i.e. $V_{L1}$ and $V_{H1}$, determine three resulting frequency ranges. First, the middle frequency range $f_1$ is the expected frequency range, indicating a proper operation of the PLL and no calibration is required. The control bits of this frequency range $f_1$ are [$S_1$, $S_2$, $S_3$] = [0,1,0], maintaining the voltage $V_T$ to connect to $V_{TN2}$. Second, the frequency range $f_2$ is lower than the range $f_1$ by the frequency offset $\Delta f_L$. Therefore, the calibration is proceeded where the control bits are changed to [$S_1$, $S_2$, $S_3$] = [0,0,1], switching $V_T$ to connect to $V_{TN3}$ in order to increase the oscillation frequency. Last, the frequency range $f_3$ is higher than the range $f_1$ by the frequency offset $\Delta f_H$. The calibration is also proceeded where the control bits are changed to [$S_1$, $S_2$, $S_3$] = [1,0,0], switching $V_T$ to connect to $V_{TN1}$ in order to decrease the oscillation frequency.

Fig.6.11 shows voltage margins and block diagram of the test and calibration circuit. The combined built-in test and calibration system is based on the deviation of $V_{CT}$ during locking state with respect to the pre-defined voltage margins. Four voltage margins are introduced, and determined by pre-simulation of process and temperature variation

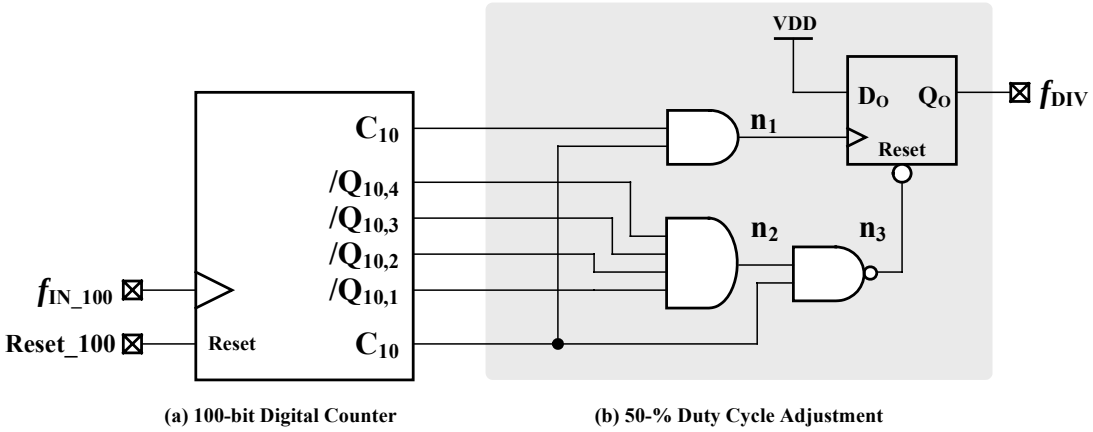



**Fig.6.12.** Circuit diagram of the divide-by-100 with a 50% duty cycle.

conditions. The expected value of $V_{CT}$ in the range of $V_{L1}<V_{CT}<V_{L2}$ indicates a proper operation, and therefore no calibration is performed. In the case where $V_{L2}<V_{CT}<V_{L1}$ and $V_{H1}<V_{CT}<V_{H2}$, the calibration process is proceeded and the test output is reported as "pass" status. The calibration is facilitated for accommodating parametric variations, resulting in low yield loss. In the case where $V_{CT}>V_{H2}$ and $V_{CT}<V_{L2}$, the CP-PLL operations fail catastrophically. No calibration is performed and the test output is reported as "fail" status. This test strategy is the pre-screening of catastrophic faults such as shorts and opens. Monitoring via $V_{CT}$ may not offer high fault coverage. However, tremendous changes such as stuck-at ground and stuck-at-$V_{DD}$ faults are easily detected, offering observability and accessibility when the PLL is in mixed-signal systems.

As shown in Fig. 6.11(b), $V_{CT}$ is initially digitized against four voltage margins by means of four comparators, providing four digitized signals $L_1$, $L_2$, $H_1$ and $H_2$. On the one hand, two signals $L_1$ and $H_1$ are employed for calibration process through the finite state machine, which has three states and provides two output signals $D_1$ and $D_2$. These signals $D_1$ and $D_2$ are subsequently contributed to the digital logics for encoding to the three signals $S_1$ to $S_3$. On the other hand, two signals $L_2$ and $H_2$ are test outputs. A single test output $V_{PF}$ can be obtained from OR gate, which reports pass and fail status in digital forms as "0" and "1", respectively. This $V_{PF}$ also enables calibration process when $V_{PF} = 0$.

### 6.3.5 Supply-Regulated Ring VCO with Frequency Tuning

In general, the digital section of CP- PLLs involves DIV and PFD circuits. The DIV circuit divides the output frequency $f_{OUT}$, providing a divided frequency $f_{DIV}$. The PFD circuit subsequently compares phase-frequency differences between $f_{DIV}$ and the reference frequency $f_{REF}$, generating *UP* and *DN* signals for the CP circuit. Noted that these DIV and PFD circuits are operating under the common power supply $V_{DD}$. Fig.6.12 shows circuit

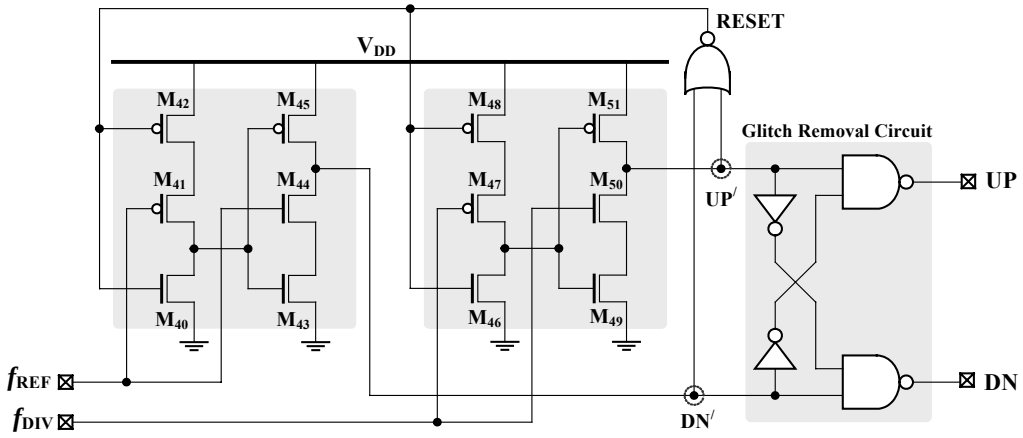



**Fig.6.13.** Circuit diagram of the dynamic PFD with glitch removal circuit.

diagrams of the divide-by-100 with a 50% duty cycle by *Baker* (2007). The circuit consists of a 100-bit digital counter. However, the divided output does not have 50% duty cycle, and therefore a digital logic with DFF is added to adjust the duty cycle to 50%. Fig. 6.13 particularly shows the circuit configuration of the PFD circuit. The dynamic PDF in (*Deng and Kiang*, 2009), consisting of two identical logics formed by transistors $M_{40}$ to $M_{51}$, was chosen for high-speed operations with a small dead zone. Nonetheless, a large transient glitch is generated at the direct outputs $UP^{/}$ and $DN^{/}$. A glitch removal circuit implemented by simple inverters and NAND gates was therefore included in order to remove transient glitches.

## 6.4 Results and Discussions

### 6.4.1 Post-Layout Simulation Results

The proposed supply-regulated CP-PLL with test and calibration system was laid out using 0.18-μm CMOS technology and post-layout simulations were carried out through Hspice. Fig.6.14 demonstrates the designed layout diagram where the effective area was measured at 350x460 $\mu m^2$. Initially, AC and DC characteristics of reference voltages were determined based on a common $V_{DD}$ = 1.8V. Fig.6.15 shows a constant $V_{REF}$ of 0.8V over the entire $V_{DD}$ range of 1V to 2.5V. The regulators $REG_1$ and $REG_2$ provide $V_{DDA}$=$V_{DDB}$=1.2V with PSR of –48dB and –78dB at 200MHz, respectively. Stable reference voltages against changes in $V_{DD}$ were therefore readily obtainable with high PSR performances. Secondly, a 200-MHz CP-PLL was designed as a particular example. Table 6.2 summarizes parameter setting and simulated performances. Fig.6.16 depicts plots of voltage-to-frequency characteristics of the VCO where $K_{VCO}$=6.28x$10^9$ rad/sV. The expected center frequency on the frequency range $f_1$ was 200MHz at the input control

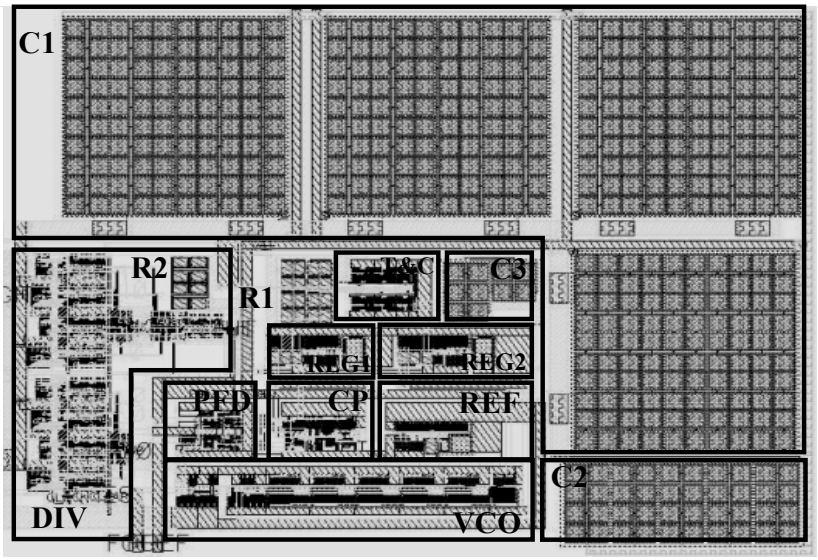



**Fig.6.14.** Layout design of the proposed regulated charge pump PLL.

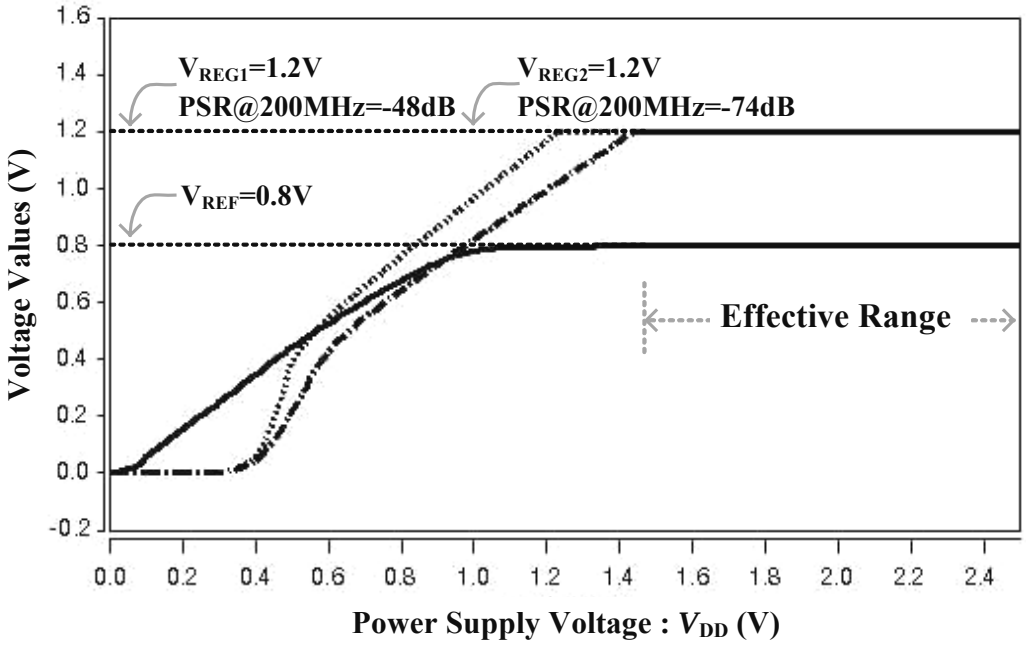



**Fig. 6.15.** Characteristics of the reference generator and the regulators.

voltage of 0.65V. Fig.6.17 shows the overall operations of the PLL of the resulting control voltage $V_{CT}$, showing locking time of 4μs. Thirdly, RMS jitters in three noise conditions were summarized in Table 6.3. The values of RMS jitters in PLL with no supply regulation are relatively considerable, i.e. 14.33ps and 40.30ps. Meanwhile, the proposed supply regulated PLL produces smaller RMS jitters of approximately 12ps for all cases, indicating the capability of supply noise suppression by the regulators. Fourthly, three frequency ranges shown in Fig. 6.16 with frequency offset of 20MHz, determined by

**Table1 6.2.** Parameter setting for simulations and performances.

| Parameter | | Values | Units |
|---|---|---|---|
| (a) Parameter Setting | Frequency range | 150 - 250 | MHz |
| | Division ratio | 100 | - |
| | Measured VCO gain: $K_{VCO}$ | $6.28 \times 10^9$ | Rad/sV |
| | Charge pump current: $I_{CP}$ | 8 | μA |
| | $R_1$, $R_2$ | 5, 20 | kΩ |
| | $C_1$, $C_2$, $C_3$ | 40, 4, 2 | pF |
| (b) Performances | VCO operating frequency | 200 | MHz |
| | Locking time@200MHz | 4 | μs |
| | Calibration time | $f_2$=2.1, $f_3$=2.6 | μs |

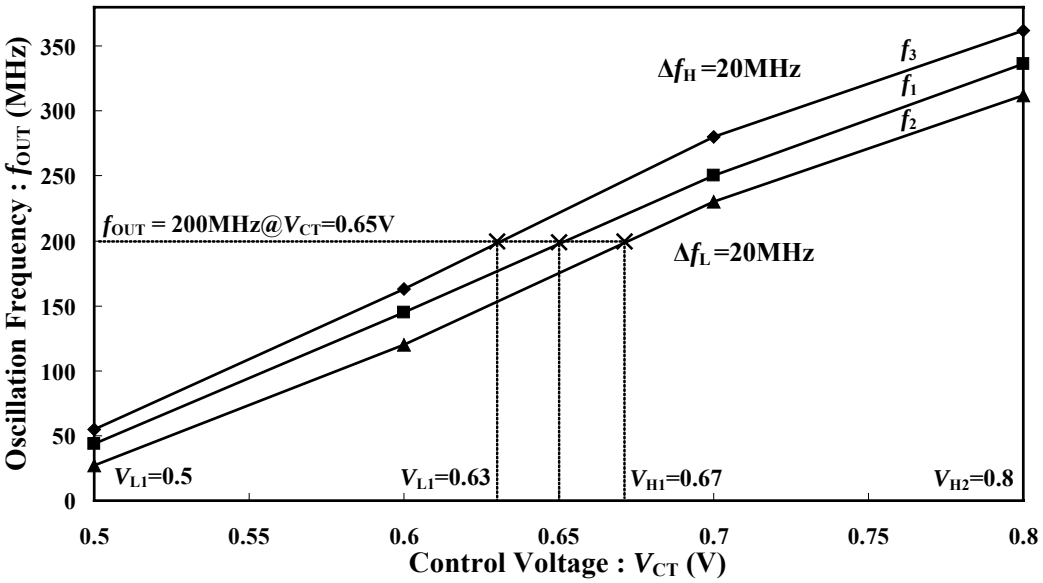



**Fig. 6.16.** Plots of simulated voltage-to-frequency characteristics of the VCO.

pre-simulation of process variation, were realized for calibrations process. The voltage margins $V_{L1}$, $V_{L2}$, $V_{H1}$ and $V_{H2}$ were set at 0.5V, 0.63V, 0.67V and 0.8V, respectively. The calibration time employed for switching from $f_1$ to $f_2$ and $f_3$ were measured at 2.1μs and 2.6μs, respectively. Finally, test operations were investigated through realistic shorts and opens catastrophic faults. Table 6.4 summarizes four examples of fault injections. Potential shorts and opens existed in VCO and CP circuit caused stuck-at-1.2V faults and therefore the test output $V_{PF}$ reports failure status for all cases.

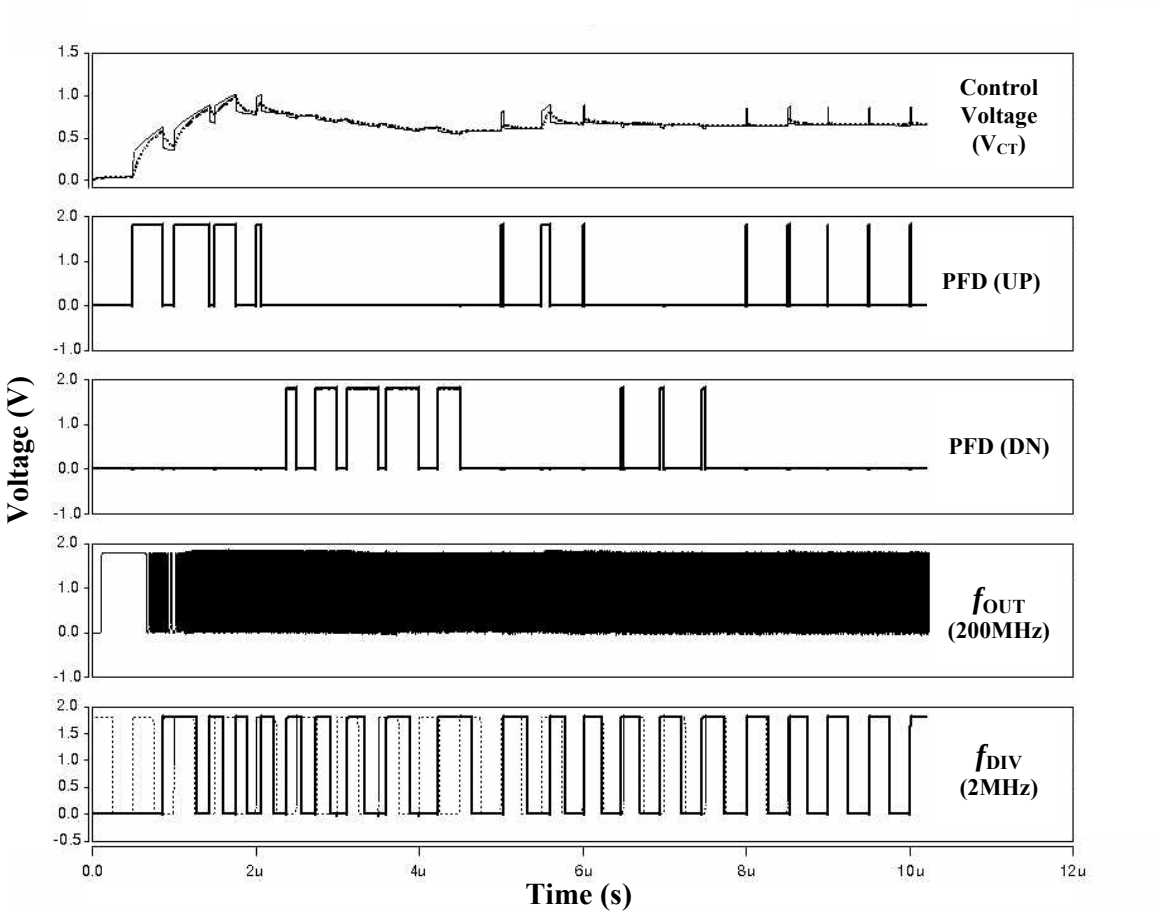



**Fig.6.17.** Simulated operating signals of the CP-PLL.

**Table 6.3.** Simulated jitter performance at $F_{OUT}$=200MHz.

| Conditions | Values of RMS Jitter | | Units |
|---|---|---|---|
| | No Regulation | Regulated Supply | |
| No noises | 9.84 | 11.42 | ps |
| 10-mV, 1-MHz Noise | 14.33 | 11.68 | ps |
| 10-mV, 10-MHz Noise | 40.30 | 12.02 | ps |

**Table 6.4.** Examples of catastrophic fault injections.

| Injected Faults | Locations | $V_{CT}$ | $V_{PF}$ | Detection |
|---|---|---|---|---|
| Short | VCO | 1.2 | High | Detected |
| Open | VCO | 1.2 | High | Detected |
| Short | CP Circuit | 1.2 | High | Detected |
| Open | CP Circuit | 1.2 | High | Detected |

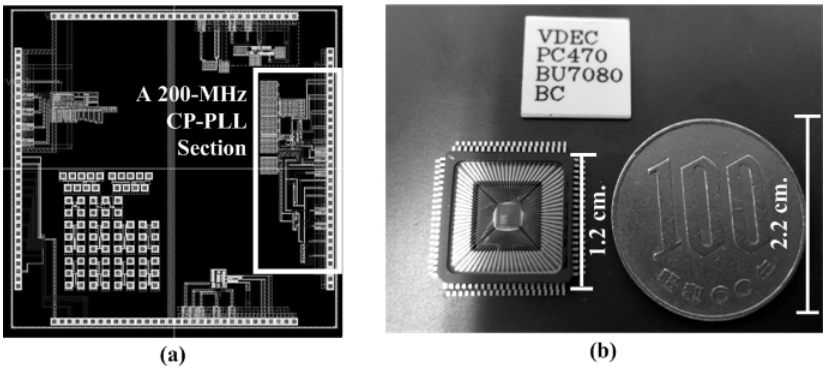



**Fig.6.18.** Photographs of (a) the top-cell layout design and (b) the fabricated chip.

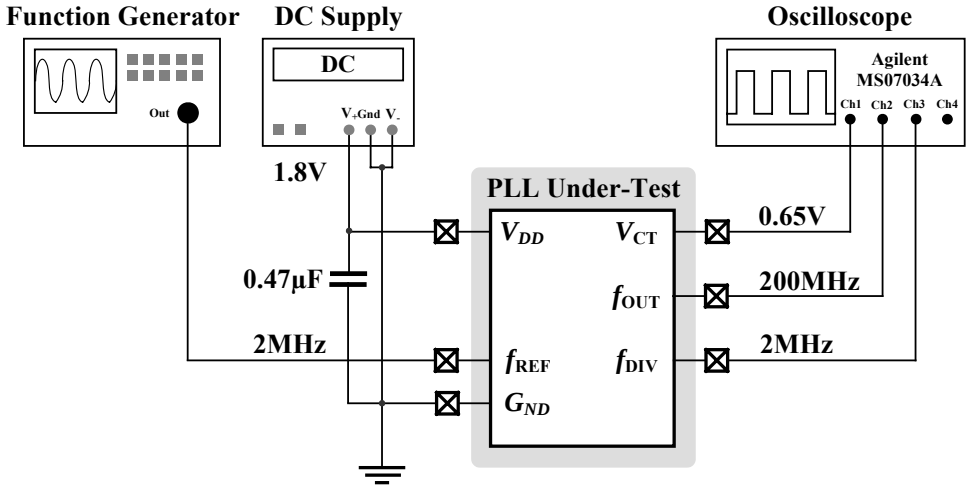



**Fig.6.19.** Diagram of experimental setup for the 200-MHz CP PLL.

### 6.4.2 Experimental Results

The experimental results were carried out through the fabricated chip model VDEC-PC470-BU7078-BC. Fig. 6.18 (a) and (b) show the photographs of the top-cell layout and the fabricated chip, respectively. It should be noted that this chip also contains other digital circuits as for academic proposes. Fig.6.19 shows the diagram of experimental setup for the 200-MHz CP-PLL. It can be seen that the power supply was set at 1.8V. The reference frequency was set at 2MHz. Fig. 6.20 shows the photograph of the corresponding experiments. Firstly, characteristics of the voltage reference and regulator circuits were investigated. Fig.6.21 shows plots of voltage transfer characteristics of the voltage regulator $REG_1$. It can be seen in Fig.6.21 that the effective range of simulated values, as previously depicted in Fig. 6.15, is in the region beyond 1.4V. The effective range of the experimentally measured values is also found in the similar region. There are some voltage deviations and the percentage of error was found at 12.5%. This deviation may be considered as a result of the variation in voltage threshold and bias current values of the

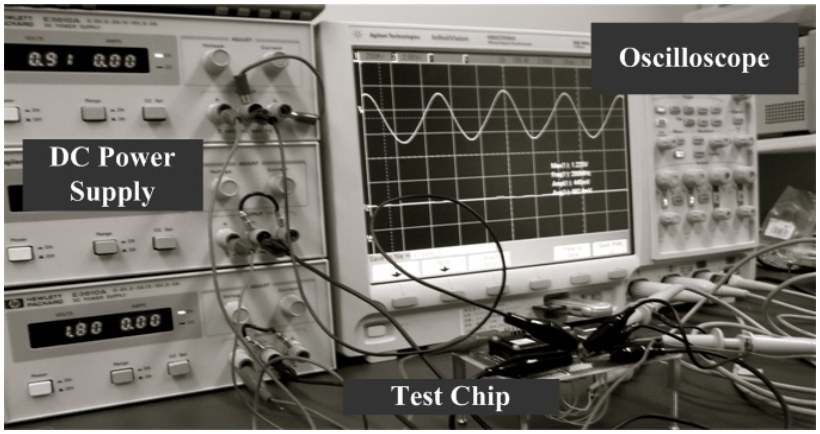



**Fig.6.20.** Photograph of the experiments.

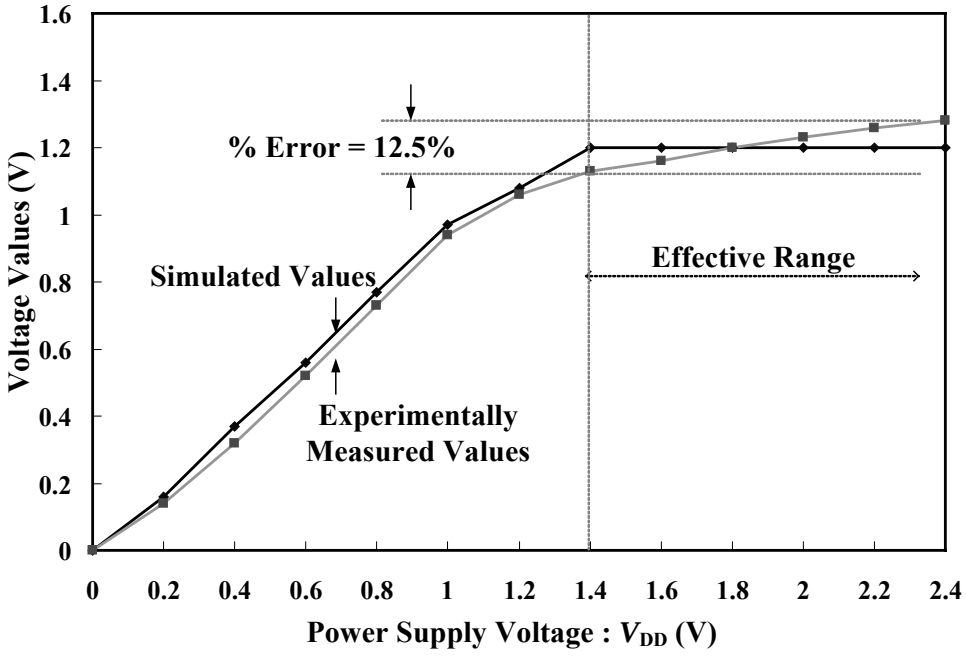



**Fig.6.21.** Plots of voltage transfer characteristics of the voltage regulator $REG_1$.

transistors. However, it is acceptable for this application since the great variation to from 1.4V to 2.4V variation in power supply voltage can greatly be reduced to the region of 1.3V to 1.28V. Secondly, Fig.6.22 shows plots of voltage-to-frequency transfer characteristics of the VCO. The transfer curve is relatively linear where the error percentage of center frequency was calculated at 5%. The variation in voltage-to-frequency transfer characteristics is relatively common for VCO as variations in transistor parameters potentially cause changes in the output frequency. However, this work has relatively low variations. Fig.6.23 shows the waveform of the VCO output signal. The frequency was measured at 200MHz at the control voltage $V_{CT}$ of 0.69V. The peak-to-peak voltage and the offset voltage were measured at 0.445V and 0.98V, respectively. The VCO was operating correctly and ready for the CP-PLL with a jitter of 25ps.

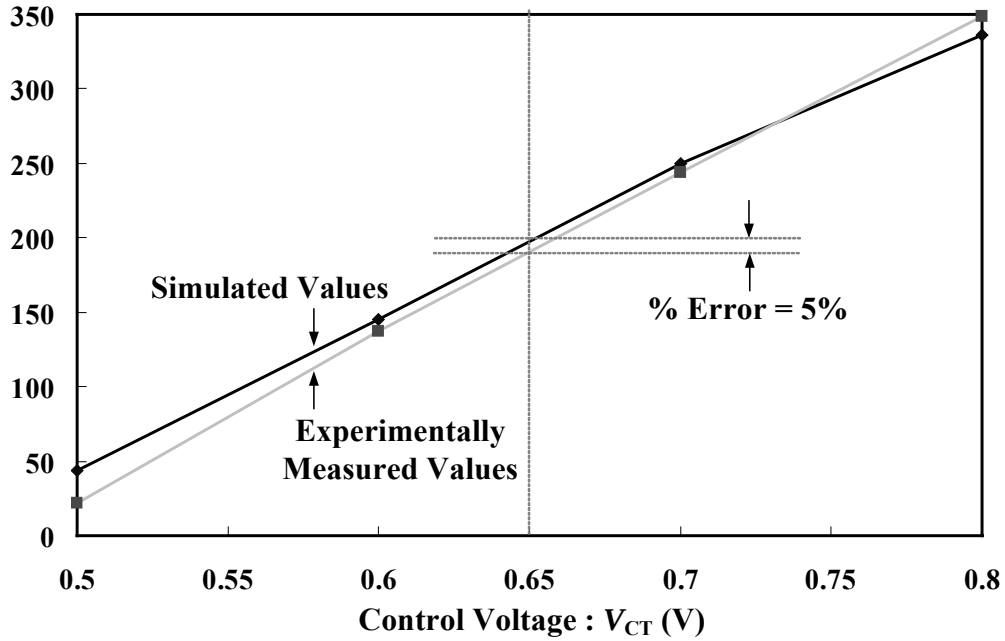



**Fig.6.22.** Plots of frequency-to-voltage characteristics of the VCO.

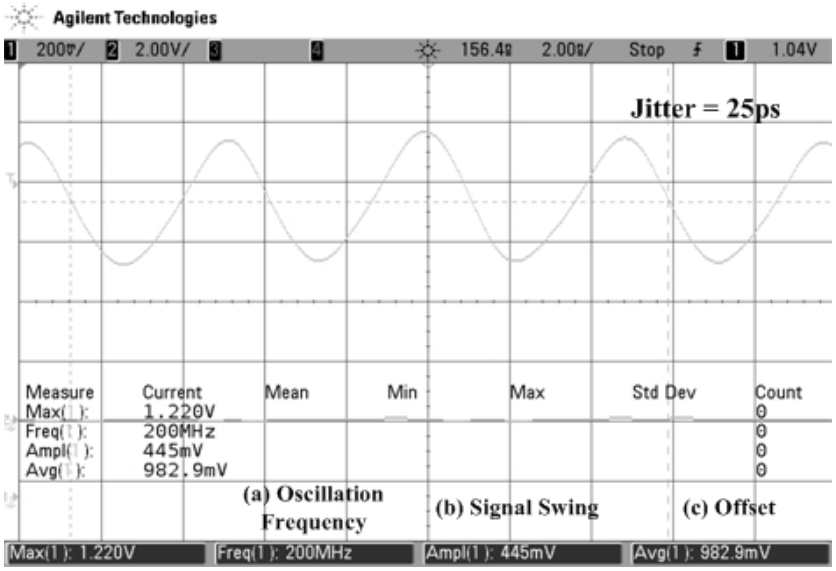



**Fig.6.23.** The transient waveform of the VCO output signal.

Finally, the operation of the CP-PLL was investigated. As depicted in Fig 6.19, the reference frequency was set at 2MHz and the output frequency was 200MHz. Fig.6.24 shows waveforms of the reference frequency and the divided frequency. It can be seen that the divided frequency was 2.02MHz. This value is deviated from 2-MHz reference frequency due to time-domain jitters. Fig.6.25 demonstrates the waveform of the control voltage $V_{CT}$ at RMS value of 0.643V, which is relatively close to the simulated voltage at 0.65V. This CP-PLL has no fault, and therefore the test output is "0" and no calibration is required.

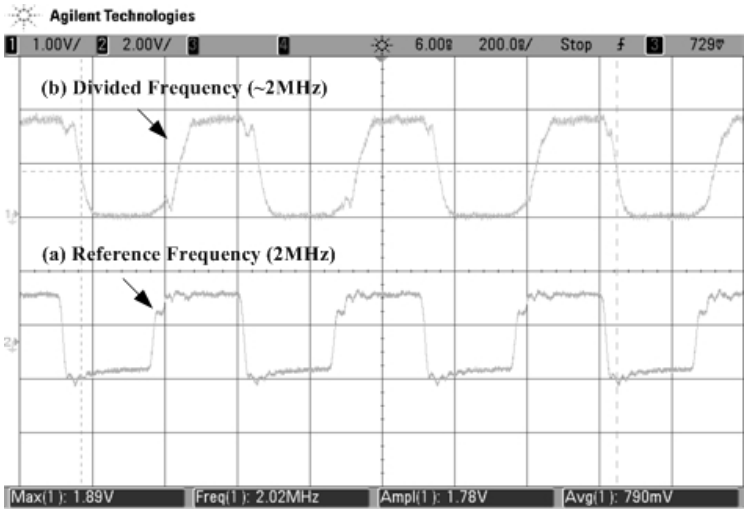



**Fig.6.24.** Waveforms of the reference frequency and the divided frequency.

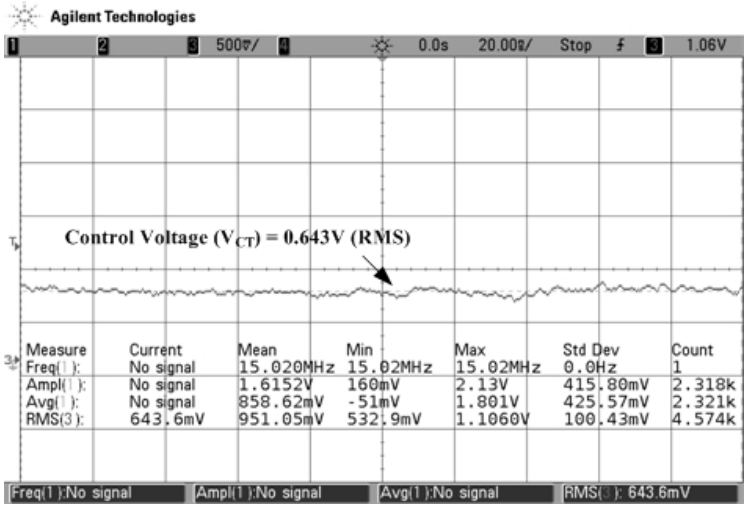



**Fig.6.25.** Waveform of the control voltage $V_{CT}$ at RMS value of 0.643V.

## 6.5 Conclusions

This chapter has presented a supply-regulated CP phase-locked loop with integrated BIST and calibration. The CP-PLL architectures, and four related BIST and calibration techniques were initially reviewed. The proposed technique employs two independent regulators that provide low-sensitivity supply voltages with inherent noise suppression for analog blocks, and afford multiple reference voltages for test and calibration process. The built-in pre-screening BIST and calibration system based on the deviation of a control voltage during locking state facilitates on-chip accessibility and observability. Demonstrations through simulations and experiments of a 200-MHz CP-PLL demonstrate low-jitter and low supply sensitivity performances. This work has offered a potential alternative to a high performance CP-PLL in LSI system with test and calibration functionality.

# Chapter 7

## Conclusions

This dissertation has presented new BIST and calibration techniques for catastrophic failures and parameter variations for analog mixed-signal LSI systems. Chapter 1 has summarized the background, viewpoint, perspective reviews and classifications of existing BIST techniques. Two investigating physical defects in integrated circuits involve catastrophic faults, which are commonly referred to potential shorts and opens, and parametric faults, which represent the parameter variations of the nominal value, which exceeds the attributed tolerance band. The major objective has set to develop new BIST techniques for catastrophic fault detection and parametric fault calibration. The designed BIST techniques are expected to be versatile for specific type of analog and mixed-signal circuits, and capable of yielding high fault coverage. The implemented BIST system in CMOS technology has expected to yield low area overhead, low power consumption, and low performance degradation. The recent BIST test strategy in which each analog and mixed-signal functional block is tested independently through different test techniques was realized. These independent tests yield not only higher fault coverage as each specific circuit is tested based on its functions, but also offer accessibility capability to each individual circuit. The scope of developed BIST techniques has emphasized on most common CUT types encountered in LSI systems. Such CUTs were ranged from a simple analog building block, which comprises only CMOS transistor, to more complicated mixed-signal circuits composed by various analog and digital building blocks.

As for a particular investigation on a compact CMOS-only analog circuit as a simple building block in most LSI systems, Chapter 2 has presented the BIST technique based on two-step testing mechanisms for catastrophic fault detection in the pre-screening process of defective analog integrated circuits. This technique monitors fault signatures through amplitude and offset of output voltages consecutively, and detects faults through acceptable tolerance bands. Normal operation and test modes are selectable through the mode-selecting switch. The BIST circuit employs only two comparators, two inverters, and seven switches. Demonstrations of the embedded BIST circuit for a common two-stage differential amplifier, containing a total injected fault of 40 faults, have shown the

percentage of fault coverage and the area overhead of 95.45% and 15%, respectively. While maintaining a high percentage of fault coverage and occupying a small chip area, there is no additional requirement for multiple sensing nodes, flip-flops, a voltage regulator and a capacitor-based peak detector. This BIST technique offers non-intrusiveness of the testing approach, which does not require the CUT configuration changes, and affordability of digital test outputs.

Chapter 3 has presented the BIST technique with cost-effective test process in analog domain based on a pulse input stimulus and a single voltage sample obtained on a pulse response. Since the variation in capacitor and resistor in integrated circuits is relatively large, the targeting CUTs particularly involve RC-based LTI analog building blocks in LSI circuits such as higher-order filters, which contain a number of capacitors and resistors. This technique employs a pulse generator, which concurrently provides two short pulses for stimulating a CUT and controlling the sampling process. The pulse generation is based on the phase detection through XOR gate, which compares phase difference at low-to-high state transition time between the input clock and its delayed counter part. A single effective voltage on a transient pulse response is sampled using a S/H circuit and subsequently employed for fault detection through a window comparator. The S/H circuit was designed based on a unity-gain sampler, consisting of a sampling switch with charge-injection error reduction, a holding linear capacitor, and a buffer amplifier. The voltage comparator comprises two simple differential amplifiers and a single NAND gate, reporting Pass/Fail test output in digital form. This BIST system implementation alleviates the need for fault-free bit streams, high-precision on-chip analog stimuli, and synchronization processes. Demonstrations of BIST system for Sallen-Key low-pass filter with a cut-off frequency of 500kHz, containing the total number of 67 faults, show high percentage of fault coverage at 95.5%. Experimental results show an area overhead of approximately 12% and low degradation on existing CUT performances. Complete BIST operation on-chip of four CUT examples and comparisons of other related techniques are also included. This proposed pulse response based-BIST technique has offered a potential alternative to low-cost and high-speed BIST system for defective analog integrated LTI circuits in mixed-signal systems.

No complete on-chip and off-chip testing capability compliant to IEEE 1149.4 analog boundary scan standard has been investigated. Chapter 4 has presented the BIST technique based on fault signature characterization for those embedded analog circuits in mixed-signal LSI core with available IEEE1149.4 boundary scan standard. The testing technique is a sinusoidal fault signature characterization, involving the measurement of DC offset, amplitude, frequency and phase shift, and the realization of two crossing level voltages. Fault detection process is performed consecutively in three steps, i.e. digitization, comparison and summation. Fault detection circuit employs only four window comparators,

two XOR gates, and a single NAND gate. The testing system is an extension of the IEEE 1149.4 standard through the modification of an analog boundary module, affording functionalities for both on-chip testing capability, and accessibility to internal components for off-chip testing. Four operating modes are as follows; a typical digital boundary scans mode, a typical external analog test mode, an extended external analog test mode, and an extended on-chip testing mode. Demonstrations of IEEE 1149.4 standard based BIST system has been performed for a $4^{th}$-order Gm-C low-pass filter. Both catastrophic and parametric faults are potentially detectable at the minimum parameter variation of 0.5%. The fault coverage associated with CMOS transconductance operational amplifiers and capacitors are at 94.16% and 100%, respectively. Low performance degradation has been verified through low deviation of the DC gain and the linearity of values 0.0025% and 0.895%, respectively. This technique offers the enhancement of standardizing test approach, which reduces the complexity of testing circuit and provides non-intrusive analog circuit testing.

As a self-oscillating circuit with no applied input signal is one of a critical building in mixed-signal LSI systems, no complete BIST technique has been studied due to the aware of output sensitivity, noises and performance degradation. Chapter 5 has therefore presented a regulated supply tuning voltage-controlled oscillator with built-in test and calibration. A low-dropout regulator with an integrated low-pass filter operates as a frequency-tuning element with inherent noise suppression. Frequency calibration employs a bias current tuning in three frequency ranges for adjusting an oscillation frequency shift caused by parametric faults. This frequency calibration circuit employs current-starved inverters instead of simple inverters, enabling the separation of the tuning through a control voltage and bias currents, incorporating a logic control circuit that performs the switching to both high and low frequency ranges through two-bit control signals. Built-In Voltage and Current Sensor (BIVCS) facilitates on-chip accessibility and testability for catastrophic fault injection. This BIVCS implemented by MOS-resistors and two comparators performs voltage comparison for testing the regulator, and current comparison for testing the oscillator. Circuit implementation demonstrates low jitter performance of less than 14.32ps at the oscillation frequency of 200MHz. High and low frequency ranges can be calibrated with the offset frequencies of 22MHz and 20MHz, respectively, through two-bit control signals. Tests for potential shorts and opens show the detected faults of 159 from all 190 faults, resulting in a high percentage of fault coverage at 83.68%. This proposed technique can be employed as a low-jitter VCO with fully built-in test and calibration in various mixed-signal circuits such as phase-locked loops and clock-and-data recovery circuits in receiver front-ends.

Finally, Chapter 6 has presented the a charge pump phase-locked loop (PLL), which is a significant mixed-signal circuit in a variety of applications. This technique is the

integration of power supply regulation system in a charge pump PLL that offers power supply noise suppression and facilitates built-in test and calibration system. Two independent regulators are employed in order to provide low-sensitivity supply voltages with inherent noise suppression for analog blocks, and to afford multiple reference voltages for test and calibration process through a 3-frequency-range VCO. The built-in pre-screening test and calibration system based on the deviation of a control voltage during locking state facilitates on-chip accessibility and observability. Demonstrations were performed for a 200-MHz charge pump PLL. Stable reference voltages against changes in the supply voltage were therefore readily obtainable at 1.2V with high PSR performances of –78dB. This supply regulated PLL consequently produces smaller RMS jitters of approximately 12ps for all cases, indicating the capability of supply noise suppression. The expected center frequency was 200MHz at the input control voltage of 0.65V, and three frequency ranges are adjustable with frequency offset of 20MHz, i.e. ranging from 180MHz to 220 MHz. Potential shorts and opens were detectable and test output correctly reports failure status for all cases. This technique has offered an alternative design of charge pump PLLs that cooperates power supply sensitivity reduction, and built-in test and calibration system.

All proposed techniques have demonstrated a compact implementation using a few number of compact components while maintaining high average fault coverage of greater than 80%, which is sufficient for cost-effective on-chip prescreening process. Unlike other BIST approaches in which the CUT has to be modified in order to facilitate test features, these proposed BIST techniques do not modify the existing CUT since particular types of input stimulus and output response characterization were employed for specific types of CUT, resulting in low performance degradation. Moreover, all proposed BIST circuits are designed as switchable circuitries, i.e. normal operation and test modes are selectable, in order to avoid loading effects and reduce extra power consumption in normal operation mode. The five techniques proposed in this dissertation have a potential of being further improved to meet the future demands in both academia and industries.

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# Lists of Publications

## Accepted International Journals

[1] Wimol San-Um, Tachibana Masayoshi, "*Built-In Self Test for Analog Integrated Circuits Using Single Pulse Stimulation and Response Capturing*", accepted for the publication in IEEJ Transactions on Electrical and Electronic Engineering.

[2] Wimol San-Um, Tachibana Masayoshi, "*A Low-Cost High-Speed Pulse Response Based Built-In Self Test For Analog Integrated Circuits*", Accepted for the Publication in ECTI Transaction on Electrical Engineering, Electronics, and Communications, Scheduled to be published in Vol 9, No. 2, August 2010.

[3] Wimol San-Um, Tachibana Masayoshi, "*An On-Chip Analog Mixed-Signal Testing Compliant with IEEE 1149.4 Standard Using Fault Signature Characterization Technique*", Published in ECTI Transaction on Electrical Engineering, Electronics, and Communications, Vol 8, No. 1, pp.85-92, February 2010.

[4] Wimol San-Um, Tachibana Masayoshi, "*A Fault Signature Characterization Based Analog Circuit Testing Scheme and the Extension of IEEE 1149.4 Standard*", Published in IEICE Transactions on Information and Systems, Special Section on Test, Diagnosis and Verification of SOCs, Vol.E93-D, No.1 pp.33-42, January 2009.

## In Preparation for International Journal Submission

[5] Wimol San-Um and Tachibana Masayoshi, "*Built-In Test and Calibration Technique for Charge Pump Phase-Locked Loops with Reduced Power Supply Noise using Adaptive Supply Regulation System*", In preparation to be submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Scheduled to be submitted in End of June 2010.

**International Conferences**

[6] Wimol San-Um and Tachibana Masayoshi, "*A Low-Jitter Supply-Regulated Charge Pump Phase-Locked Loop with Built-in Test and Calibration*", Proceeding of The IEEE International Symposium on Circuits and Systems (ISCAS), Oral Presentation in Paris, FRANCE, 2010.

[7] Wimol San-Um and Tachibana Masayoshi, "*A Regulated Supply Tuning Voltage-Controlled Oscillator with Built-In Test and Calibration*", Proceeding of the 7th Annual Conference of Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology Association of Thailand (ECTI-CON), Oral Presentation Chiang-Mai, THAILAND, 2010.

[8] Wimol San-Um and Tachibana Masayoshi, "*Impulse Response Based Built-In Self Test for Analog Integrated Circuits in Mixed-Signal Systems*", Proceeding of The 2nd Thailand-Japan International Academic Conference (TJIA), Oral Presentation Kyoto, JAPAN, 2009.

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**Wimol San-Um**, 29, was born in Nan Province, Thailand. He received B.E. in Electrical Engineering and M.Sc. in Telecommunications in 2003 and 2006, respectively, from Sirindhorn International Institute of Technology, Thammasat University, Bangkok, Thailand. In 2007, he was a research student at University of Applied Science Ravensburg-Weingarten, Germany. Since 2008, He has been working towards his Ph.D. at the Department of Electronic and Photonic System Engineering, Kochi University of Technology, Japan. His areas of research interests are analog circuit designs, involving chaotic oscillators and switched-current circuits, and on-chip built-in self test.