Built-In Self-Test (BIST) Techniques for Data Converter in Analog and Mixed-Signal Circuits

Jun YUAN

A dissertation submitted to
Kochi University of Technology
in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy

Graduate School of Engineering
Kochi University of Technology
Kochi, Japan

September 2012

Abstract

The rapid development of Integrated Circuits (IC) fabrication technology and the advance of System-on-a-Chip (SoC) design technology have made it possible to integrate millions of transistors on a single chip including digital and analog components. These mixed-signal solutions are widely used in modern mobile and multimedia devices. However, the high integration density has limited the accessibility and observability of the internal components since the limited I/O pins. As a result, the traditional off-chip testing has become a major challenge for analog and mixed-signal circuits, especially for the analog blocks, which have a large number of performance parameters with a fluctuation range.

As a tool for digital verification and production testing, Built-In Self-Test (BIST) has attracted a lot of research attention for analog circuit testing by implementing both stimulus generator and response analyzer entirely on-chip. It reduces the tester complexity, eliminates the need for off-chip interfacing, and allows the device to be tested many times during the manufacturing cycle of the product. Conventionally, performance parameters were measured on-chip to test analog blocks, but this specification-based BIST techniques result in high-test costs due to the complex testing circuits and test time. Therefore, another structural test technique, fault-based BIST was proposed to detect the possible physical defects caused by the IC manufacturing process.

In a typical application of the mixed-signal system, the external analog signals are sensed and changed to digital representations by Analog-to-Digital Converter (ADC), after the digital signal processing, the digital data are translated to our inherently analog world again by Digital-to-Analog Converter (DAC). ADC and DAC are at the systems level, and they typically contain amplifiers, sample-and-hold circuits, low-pass filters, etc. This dissertation aims to design fault-based BIST techniques for the data converter system based on the divide-and-conquer strategy. Firstly, the data converter system is broken into different kinds of sub-circuits based on the structure. Then, for each sub-circuit, one or more unusual signals are employed as test stimuli to excite the faults injected into this circuit, meanwhile, one or more parameters of the circuit are observed

to determine the test result by comparing with their fault-free values. As a result, each sub-circuit can be tested by its own independent BIST technique based on its structure. Finally, these self-testable subsystems are combined to re-constitute the data converter system, but it is not a simple assembling process. On the same chip, the BIST circuits for one sub-circuit can be shared with other sub-circuit, and some BIST circuits can be replaced to only one circuit with the same functions. In addition, some fault-free original sub-circuits under test in the data converter can be used as BIST circuit for other sub-circuits. As a result, the BIST circuits for the whole data converter can be simplified and the test controlling of the sub-circuits is transferred to the high level test controller/bus generated by the digital block in the mixed-signal system. The high level test bus controls the whole testing procedure, and enables the BIST circuits to test some sub-circuits in their idle time in the system operation of the data converter.

Based on the above-mentioned divide-and-conquer strategies, this thesis presents three BIST techniques. The first proposed BIST technique is to test Operational Amplifiers (Op Amps) by checking the stable output of the transient response, then to improve the fault coverage for Op Amp testing, a two-step BIST scheme and its implementation were also proposed. The second proposed BIST technique is the resistance-matching based BIST technique for current-mode R-2R DAC. This is a re-constructing example of the divide-and-conquer strategy. The third proposed technique is the Common-Mode (CM) BIST technique for Fully-Differential (FD) Sample-and-Hold (S/H) circuits.

The proposed BIST techniques shows that based on the exciting of the unusual signals like transient signal and pulse, the fault-based BIST technique can be achieved by checking the outputs of the Circuit under Test (CUT). Then, the existing BIST techniques can be integrated into a compact test technique for the whole data converter through simplification and reconfiguration, and every sub-circuit can be well tested with their acceptable fault coverage. Also, the proposed BIST techniques do not cause significantly performance degradation by disconnecting the BIST circuits to the CUT when the data converter is under its normal operation.

Acknowledgements

Firstly, the author would like to express his deepest gratitude to his advisor, Prof. Dr. Masayoshi TACHIBANA, for his valuable supervision, supports and encouragements throughout the past nearly three years, and to Prof. Dr. Seiken YANO, Katsushi IWASHITA, Dr. Yukio MITSUYMA, Prof. Dr. Keiichi SAKAI and Koji NONAKA for their valuable suggestions and discussions.

Then, the author wishes to acknowledge Prof. Lawrie HUNTER for his useful research writing classes and two-page system, and to Prof. Mikiko BAN, Ms. Sonoko FUKUDOME, Ms. Kimiko SAKAMOTO, Ms. Mari YAMSAKI, Ms. Rika FUKII, Ms. Mariko KUBO, Mr. Motoi YOSHIDA and Ms. Kimi KIYOOKA, members of International Relation Center, for their kind helps. The author also wishes to thank Kochi University of Technology for its Special Scholarship Program for PhD study, and to Prof. Katsuki MATSUMURA for his hospitality and financial support under Flying-Fish Scholarship.

Especially, the author would like to thank Prof. Chaoyang LI and Prof. Yongdong TAN for her encouraging and helping in research and life in Japan, and also tanks Ms. Yumi TAKEMURA, colleagues in LSI laboratory and all friends in Kochi for their useful technique sharing and assistance.

Finally, the author wishes to sincerely appreciate his parents and younger sister for their endless love, sacrifices and supports for past years, and all the persons who helped to finish this thesis.

Table of Contents

List of Figures ..... **VIII**

List of Tables ..... **XI**

Chapter 1. Introduction **1**

1.1. IC Testing 1

1.2. DFT and BIST Techniques 3

1.2.1. Digital DFT and BIST Techniques 3

1.2.2. Analog and Mixed-Signal DFT and BIST Techniques 5

1.2.3. Existing BIST Approaches for Analog Circuits 7

1.3. Fault Modeling for Analog Circuits 8

1.4. Dissertation Developments and Organizations 11

1.4.1. Motivation and Objectives of This Work 11

1.4.2. Thesis Organizations 13

Chapter 2. BIST Techniques for Operational Amplifier **15**

2.1. Reviews on Op Amp Testing 15

2.2. The Stable Output Value (SOV) Checking based BIST 16

2.2.1. Test Strategy and Technique 17

2.2.2. The SOV Checking based Test System Implementation 19

2.2.3. Simulation Results 21

2.2.4. Conclusions 26

2.3. A Two-Step BIST Technique for Op Amp 26

2.3.1. The Two-Step Test Strategy 26

2.3.2. The Two-Step Testing System and Its Implementation 28

2.3.3. Simulation Results 35

2.3.4. Conclusion 38

2.4. Conclusions and Discussions 38

Chapter 3. A Resistance-Matching based BIST Technique for Current-Mode R-2R DAC **40**

3.1. Introduction to DAC Testing 40

3.1.1. DAC Testing 40

3.1.2. BIST Techniques for DAC 41

3.2. Resistance-Matching Based Test Strategy 43

3.3. The Current-Mode R-2R DAC with DFT Circuits 45

3.4. Test System Implementation 49
3.4.1. The Proposed BIST System 49
3.4.2. Output Response Analyzer 50
3.4.3. Control Logic 52
3.5. Simulation Results 53
3.5.1. Fault Modeling for R-2R DAC 53
3.5.2. The Simulation Results and Discussion of the 8-bit R-2R DAC 53
3.6. Conclusions 60
Chapter 4. A CM BIST Technique for FD S/H Circuits **62**
4.1. Introduction to S/H Circuit and Its Test 62
4.1.1. Charge Injection and Clock Feedthrough in Analog Switch 62
4.1.2. S/H Circuits 64
4.1.3. Overviews on S/H Circuit Testing 68
4.2. The CM Test Strategy 70
4.2.1. FD Op Amp with CMFB 70
4.2.2. CM Test for FD S/H Circuit 76
4.3. The CM Test System Implementation 79
4.4. Simulation Results 83
4.4.1. Fault Models for S/H Circuits 83
4.4.2. The Simulation Results of the Flip-Around FD S/H Circuit 83
4.5. Conclusions 86
Chapter 5. Conclusions and Discussions **88**
Reference **91**
List of Publications **101**

List of Figures

Figure 1.1 Major steps in IC manufacturing flow [3]. 2
Figure 1.2 Basic BIST architecture [2]. 5
Figure 1.3 Fault models for transistor: (a) GDS, (b) GSS, (c) DSS, (d) DO, (e) SO, (f) GO. .11
Figure 1.4 Architectures of system-level BIST and sub-circuit based BIST....12
Figure 1.5 The expected simplified sub-circuit-based BIST in this dissertation....13
Figure 2.1 Transient responses of a voltage follower configured from the Op Amp. 18
Figure 2.2 Voltage follower configuration of an Op Amp. 19
Figure 2.3 The proposed SOV checking based BIST architecture: (a) The single Op Amp case. (b) The multi-Op Amp case....20
Figure 2.4 The BIST circuit configuration: (a) A step signal generator. (b) A SOV checker. ..20
Figure 2.5 (a) The checking regions of *WC1* and *WC2*. (b) Control and data signals settings for test. 21
Figure 2.6 The circuit configuration of the two-stage Op Amp. 23
Figure 2.7 The circuit configuration of the folded-cascode Op Amp. 23
Figure 2.8 The circuit configuration of the buffered Op Amp. 23
Figure 2.9 The layout pattern of the three Op Amps with the BIST circuits. 24
Figure 2.10 The offset compensation for an Op Amp.....27
Figure 2.11 The output responses of the Op Amp under current-based comparator, voltage follower and comparator configurations. 28
Figure 2.12 The proposed two-step BIST architecture. 29
Figure 2.13 Output responses of the proposed two-step test scheme.....29
Figure 2.14 The test procedure of the proposed two-step test scheme.....30
Figure 2.15 The circuit configuration of the stimulus generators. 31
Figure 2.16 Block diagram of the designed response analyzer. 31
Figure 2.17 The checking band of the two comparators. 32
Figure 2.18 Timing waveforms of the BIST system operations. 33
Figure 2.19 The slop detection in the current-based test stage. 34
Figure 2.20 The circuit configuration of the two-stage Op Amp under test with inclusion of design for test.....35
Figure 2.21 The layout pattern of the two-stage Op Amps with the BIST circuits. 36
Figure 2.22 Faults simulation results. 37
Figure 3.1 Basic setup for DAC testing. 41
Figure 3.2 The R-2R ladder network. 44

Figure 3.3 The circuit configuration of the current-mode R-2R DAC with *DFT*s.....46
Figure 3.4 The circuit configuration of the switches S_{ti} and S_i.....47
Figure 3.5 Two test types of R-2R network test mode: (a) Test configuration when the binary input is set as "10···0". (b) Test configuration when the binary input is set as "01···1".....48
Figure 3.6 Test configuration for Op Amp used in the DAC under test.....48
Figure 3.7 Block diagram of the BIST system for: (a) R-2R network test mode. (b)Op Amp test mode. 49
Figure 3.8 Output response analyzer: (a) The block diagram of the output response analyzer. (b) Circuit configuration of the window comparator. 51
Figure 3.9 The internal test logic controller. 52
Figure 3.10 The controlling logic of the high level test bus. 53
Figure 3.11 The circuit configuration of a buffered Op Amp. 54
Figure 3.12 Fault simulation results under R-2R network test mode.....56
Figure 3.13 Fault simulation results under Op Amp test mode.....57
Figure 3.14 Layout patterns of the DUT with the BIST circuits.....57
Figure 3.15 INL and DNL comparisons of the general R-2R DAC, analog switches injected/calibrated R-2R DAC and the proposed R-2R DAC with the BIST circuits.....59
Figure 4.1 Illustration of charge injection and clock feedthrough using an nMOS switch [102]. 63
Figure 4.2 Conventional S/H architectures. 65
Figure 4.3 S/H circuit using Miller capacitance [120]. 66
Figure 4.4 Basic differential S/H circuit [110]. 66
Figure 4.5 Switched-capacitor S/H circuit [80]. 67
Figure 4.6 Bottom plate sampling [102]. 67
Figure 4.7 Test setup for S/H circuit [110]: (a) Testing DC characteristics. (b) Dynamic measurements. 68
Figure 4.8 The general structure of self-checking [140, 141]. 69
Figure 4.9 The typical architecture of the FD Op Amp. 70
Figure 4.10 The basic structure of a FD Op Amp with CMFB [77]. 72
Figure 4.11 Gain paths in the FD Op Amp with CMFB [150]. 73
Figure 4.12 A two-stage balanced FD Op Amp [148]. 74
Figure 4.13 A folded-cascode FD Op Amp. 74
Figure 4.14 The CM input to CM output relationship of the two Op Amps. 76
Figure 4.15 A flip-around S/H circuit and its operation modes. 76
Figure 4.16 A non-overlapping two-phase clock generator and its timing waveforms.....77
Figure 4.17 The CM simulation results of a FD S/H circuit. 78

Figure 4.18 The CM BIST setup for FD S/H circuit.....80
Figure 4.19 The timing waveforms for the CM test controlling signals. 80
Figure 4.20 The designed BIST circuits for FD S/H circuit CM test.....81
Figure 4.21 Voltage-transfer curves of the differential amplifier. 82
Figure 4.22 Two different layout patterns for the folded-cascode FD Op Amp.....84
Figure 4.23 The layout pattern of the flip-around FD S/H circuit with the CM BIST circuits. 84
Figure 4.24 Fault-free CM simulation of the flip-around FD S/H circuit in schematic-level..85
Figure 4.25 The fault-free CM simulation of the flip-around FD S/H circuit after the parasitic extraction form the physical design. 85

List of Tables

Table 2.1 Existing test techniques for Op Amp.....15
Table 2.2 Summary of elements parameters in the SOV checker shown in Fig. 2.4(b).....20
Table 2.3 Summary of elements parameters of the three Op Amps. 24
Table 2.4 Performance parameters of the original two-stage Op Amp and the two-stage Op Amp with inclusion of the BIST circuit. 25
Table 2.5 Performance parameters of the original folded-cascode Op Amp and the folded-cascode Op Amp with inclusion of the BIST circuit. 25
Table 2.6 Performance parameters of the original buffered Op Amp and the buffered Op Amp with inclusion of the BIST circuit. 25
Table 2.7 The design of inverters used in window comparators. 32
Table 2.8 Summary of elements parameters for the two-stage Op Amp shown in Fig. 2.20. ..35
Table 2.9 Performance parameters of the original Op Amp and the Op Amp with BIST circuits. 38
Table 3.1 Switch settings under different test modes. 48
Table 3.2 Summary of the elements parameters of the buffered Op Amp. 54
Table 3.3 Summary of the elements parameters of the stimuli generators.....55
Table 3.4 Summary of Elements Parameters in the output response analyzer and the thresholds of the three *WCs*. 55
Table 3.5 Comparisons of the BIST technique in this work with other related BIST. 60
Table 4.1 Summary of the elements parameters of the two FD Op Amps. 75
Table 4.2 The element size settings and performances of CM BIST circuits. 82
Table 4.3 Comparisons of this work and other proposed test techniques for FD S/H circuits. 87

Chapter 1. Introduction

The rapid development of IC fabrication technology and the advance of SoC design techniques have made it possible to integrate millions of transistors on a single chip including digital and analog components. As a result, the high integration density and the increasing complexity have limited the accessibility and observability to the internal component because of the limited I/O pins. Thus, the traditional off-chip test techniques have become more challenging for modern IC testing, and so new test techniques are required. Particularly, the analog part need be carefully tested.

This chapter begins with the introduction to IC testing during the production cycle. Then, the Built-In Self-Test (BIST) technique is described, and some hot issues are also presented for its application in the mixed-signal LSI systems. The existing BIST techniques are also reviewed. After this, the objective of this dissertation is included. Finally, the thesis structure is given.

1.1. IC Testing

The typical IC design begins with the specification definition from the customers' requirements including the functionality, the input/output pins, technology, etc. The next step is to decide the architecture of the design by the architecture engineers, and the whole system is usually constituted by several sub-systems. Then, the design engineers implement the sub systems from the system level to the gate level or transistor level base on the possible technology and constrains. After this, the IC layout engineers finish the physical implementation, converting the design into geometric representation, which is also called layout patterns. Following the layout mask extracted from the physical design, the IC design is finally fabricated on a silicon ship, packaged and shipped to market.

The testing is involved in the IC product life-cycle including the IC design phase, IC manufacturing phase and the system operation phase [1,2]. The initial testing is performed within the Computer-Aided Design (CAD) environment [3], during the design phase. The design can be described into different levels, such as architecture level, gate level, transistor level, and layout pattern, so the design verification is

performed to ensure every refined implementation of the design would perform the intended function described in its specification by removing the design errors [2].

Next, the IC manufacturing testing is to detect the possible defects caused by the random process instabilities and contaminations during the IC manufacturing process. It mainly consists of wafer test, package test, and burn-in test, as illustrated in Fig. 1.1. First, the wafer test is to identify the faulty designs by probing sites on the wafer after the wafer processing. The test machine marks the faulty chips at the end of the wafer processing, and this information will be used in the next manufacturing step. Then, the wafer is cut apart, and the wafer test passed chips are selected for packaging. After the chips are packaged, testing is performed again to discard the faulty chips damaged during the packaging process. Wafer test and the package test seek to detect any defects that could have been sustained during the fabrication or packaging process. Finally, another important test step is burn-in or stress testing [2-4], where the ICs that passed the package testing are subjected to the high temperature and voltage to find the ICs that have marginal defects that will lead to "infant mortality" and low reliability [5]. Conventionally, additional testing is employed to assure the final quality before shipping to market or customers.

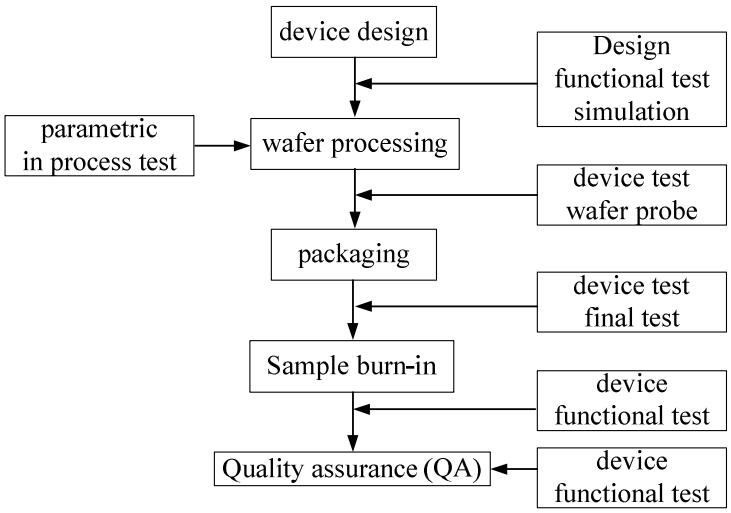


Figure 1.1 Major steps in IC manufacturing flow [3].

Finally, the "good" ICs are shipped to market and to be assembled on a Printed Circuit Board (PCB). The PCB fabrication process is a photolithographic process

similar some ways to the VLSI fabrication process [1], so the fabricated PCB should be tested as the IC manufacturing testing to discard the faulty ones. Then, the PCB are assembled with the ICs and retested to ensure it can perform as the requirement. The test about the PCB is usually called PCB test or board test. A general electronic system consists of more than one PCB, so the electronic system should be test again after the system is constituted. The electronic system passed the system test can finally put into service. During the system manufacturing process from the PCB to the final system in service, the IC chip would also be tested and the faulty ICs can be replaced by others.

IC testing addresses different issues at different phases. At the design verification phase, the test is to find the design errors in different design level, and then to modify the design to meet the specification. At the manufacturing phase, the test is to detect the physical defects that would happen during the manufacturing process, and discard the defective ICs. Also, the information like happening reason and lactation of the defects would be diagnosed and sent back to the design and production engineers to improve the IC design. At the system manufacturing and in the field service phase, the IC testing is to find the faulty ICs on the PCBs.

In the left part of this dissertation, the mentioned circuit test mainly indicates the IC testing in the IC manufacturing process and the fundamental objective of the testing is to distinguish between good and faulty ICs [6] during the manufacturing flow.

1.2. DFT and BIST Techniques

1.2.1. Digital DFT and BIST Techniques

In the past, the design and test engineers were regarded as separate functions, and responsible for different parts of the IC products. The design engineers were to implement the ICs' required functions, and did not care about the ICs testing. After the IC manufacturing process, the test engineers controlled test devices to realize the IC testing. However, with rapid development of the fabrication technology, millions of transistors can be integrated in a single chip, so the limited controllability and observability of the ICs have become a bottleneck to test. As a result, the old approach can not keep up with the high integrality and complexity of modern ICs. Therefore, test engineers wish to bring the test thought and considerations into the design phase, to

improve the testability through some modifications. These modifications for test in the design phase are so-called Design-for-Testability (DFT, also DfT) [1,2,7,8] techniques, which were described as

"The collection of techniques that comprise design for testability are, in some cases, general guidelines; in other cases, they are hard and fast design rules. Together they can be regarded as essentially as a menu of techniques, each with its associated cost of implementation and return on investment" by Williams and Parker [8].

DFT techniques are widely used in modern digital circuits and generally fall into one of the following three categories:

- (1) Ad-hoc techniques, *are usually done by incorporating multiplexers internal to the CUT to create one or more test modes of operation in which the primary inputs and outputs provide access to/from the internal difficult-to-test circuits via the multiplexers [2].*
- (2) Scan design techniques, *are implemented by connecting selected storage elements of a design in multiple shift registers, called scan chain, to provide them with external access. Scan design accomplishes this task by replacing all selected storage elements with scan cells, each having one additional Scan Inputs (SI) port and on shared/additional Scan Output (SO) port. By connecting the SO port of one scan cell to the SI port of the next scan cell, one or more chains are created [1].*
- (3) Built-In Self-Test (BIST) techniques. *The basic ideal of BIST, in its most form, is to design a circuit so that the circuit can test itself and determine whether it is fault-free or faulty, respectively[2].*

Testing typically consists of applying a set of test stimuli to the inputs of the Circuit under Test (CUT) while analyzing the output responses [1]. In the BIST application, the stimulus generation and output response analysis, implemented by the external test devices in the traditional off-chip test, are implemented by the BIST circuits incorporated into the CUT as shown in Fig. 1.2, so the circuit on-chip can access the internal signals much easier than the external tester, and the testability of the CUT can be improved using on-chip testing circuits. As it is shown in the blue parts in Fig. 1.2, the BIST circuits consist of three essential functions to facilitate the execution of the self-testing. The Test Pattern Generator (TPG) produces a set of test pattern to the

inputs of the CUT, and the outputs of the CUT are observed and analyzed by the Output Response Analyzer (ORA) to generate the test result of pass/fail indication. The test controller controls the whole test procedure with the BIST start and done signals to the high level test bus. Under the normal operation mode, the CUT performs the required functions described in the specification. Under test mode, the test controller or high test bus connects the BIST circuits to the CUT through the isolation circuits, and then execute the test.

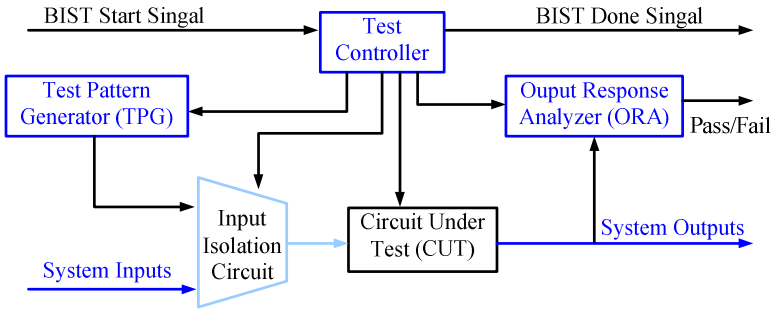


Figure 1.2 Basic BIST architecture [2].

1.2.2. Analog and Mixed-Signal DFT and BIST Techniques

With the testability improvement, modern digital circuits with high density and complexity can be well tested. However, another challenge has appeared with development of analog and mixed-signal circuits, the smaller analog blocks make these chips more sensitive to fabrication variations and tolerance accumulations [9], and the cost to produce mixed-signal devices is being dominated by their analog test costs [10]. Therefore, the design of analog blocks is often the bottleneck in the development of mixed analog-digital systems. While the analog section is usually limited to 5-10% of the mixed chip area, its design for test can take 80-90% of the develop time [7]. The test complexity and difference between analog and digital circuits described in [1,3,6,7,9-19] can be summarized as follow:

- **Analog/Digital signals**: analog signals are continuous in time and amplitude, while digital signals are discrete in both domains. Due to the continuous characteristic of analog signals, high accurate instruments are required to measure them, but the accuracy of analog instruments is limited by component variations over temperature changes, random differences between replaced

components, and components drift over extended periods of time [3]. Also, the time and voltage continuous nature of their operation make them further susceptible to defects. Therefore, test procedures are needed to discriminate between various faulty conditions and the non-faulty condition [6]. As a result, for the analog circuit test, the measurement and analysis of the continuous signals make the fault signature be a main challenge. The simple comparing of digital outputs for fault signature can not be used in analog circuit testing.

- **Input/Output relationships**: in digital circuits, the relationship between input and output signals is Boolean in nature [6]. However, the input/output relationship of analog circuit is not simple Boolean, but complicated cause-effect relationship. To describe the performances of any analog circuit, many algebraic formulas are needed, so that the test simplification techniques in digital circuits can not be extended to analog circuits, and the traditional functional testing in analog circuit is costly. Also, the analytical techniques of Automatic Test Pattern Generation (ATPG) is difficult to applied to analog circuit testing, because the fault propagation and topological boundaries of the fault influence in analog circuits can not be well-defined as that in digital circuits.
- **Sensitivity**: the performance of analog circuit is sensitive to any changes like process variation and temperature, and also heavily depends on circuit parameters due to the nonlinearity of the analog devices. This property caused several problems for analog circuit testing. First, any modification to apply DFT technique would significantly degrade the performances of the CUT. Second, in digital case, its logic function is mainly susceptible to the defects causing catastrophic failures, and is essentially independent of device mismatches [10]. However, analog circuit is susceptible to all types of manufacturing errors and the main concern when using CMOS for an analog design is matching [20], so other defects that cause parametric change should also be considered in analog circuit. Limited functional verification does not ensure that the circuit is defect-free and escaped defects pose quality and reliability problems [6]. Additionally, the test quality would be decreased by the noise caused by the test devices in analog testing. The external cables between the tester and the chip introduce parasitic that affects test quality, expensive mixed-signal testers are

required to minimize circuit noise and improve on the measurement techniques [13].

Based on the above mentioned challenges and differences between analog and digital circuits testing, the DFT techniques proposed for the digital circuits can not be directly applied to the analog circuits, some modifications need be made. In some cases, the ad-hoc technique used in digital circuit have been replaced by the CUT reconfiguration strategies [15,16,21-25] for testability improvement, because the direct replacement in analog would significantly degrade the performance of the CUT. The scan based DFT techniques used in digital circuits have also been changed to the mixed-signal test bus [26,27] by inserting data converting sections of ADC and DAC, and then the digital TPG and ORA can be used to implement analog circuit testing. The data converting sections should also be added in the analog BIST techniques for reusing the existing digital BIST techniques as shown in [2]. Another analog BIST technique has been proposed for the specific type of analog circuit. The analog test signals [28-30] are created by the on-chip stimuli generators to excite the CUT, and the analog ORA can directly observe the output response of the CUT and generate a digital test result. As a result, the data converting sections are no longer included in the BIST circuits, and that would eliminate the area overhead and design complexity. For specific analog circuit, specific test strategy is required to simplify the BIST circuits design, and this is the target that that will be reported in this dissertation.

1.2.3. Existing BIST Approaches for Analog Circuits

About analog circuit testing, there are two kinds of approaches: the first is specification-based testing, also called specification-oriented or functional testing, the functional specifications of CUT are measured and if any of the specification is violated, the circuit is declared faulty [31]. The specification-oriented testing tests every specification presented in the data sheet to determine the pass/failure of the circuit [1]. However, the specification-oriented testing has many drawbacks [32,33]. Typically, the specifications of analog circuits are insensitive to fluctuations in the manufacturing process, so the measurement errors would mask the effects of process variations. Also, the specifications of a circuit can be very complex, and so measuring them at various design corners to thoroughly test the circuit can lead to large testing times. The test hardware needed to measure the performance parameters of different circuits can be

quite different, forcing manufacturers to acquire different test equipment for different products [34].

The most basic analog functional measurement setup consists of a signal generator exciting the circuit-under-test with a known signal and an instrument to extract an appropriate parameter from the circuit's output response [10]. For BIST application, the analog test signal generator and the extract parameter extraction device should be replaced by on-chip circuits, and that would cause high area overhead. For this reason, according to the major cause of manufacturing defects, another test approach has been proposed, fault-based testing [15,35,36], is aimed at detecting manufacturing defects, which are modeled as faults. Unlike the specification parameters measurement in the specification-based testing, the fault-based testing approach is to analyze the structure of the CUT, and simulate it to determine the possible fault is existed or not. If any fault can be ascertained the CUT is faulty circuit. Conventionally, unusual signals are feed to excite the defects existing in the CUT, and the outputs are observed and compared with the expected outputs to determine the test result. According to the fault list, test engineers generates effective test signals to activate the fault in the circuit and the effect of the fault is propagated to the output, and outputs are observed and analyzed to determine the fault exists or not.

The performance measuring can also be used in fault-based testing. In this case, one or some of the performance parameters of the CUT is selected as measuring objective. If the change of the selected parameter caused by the injected faults into the CUT would be captured by the tester or on-chip test circuit, and that means the injected faults can be detected.

In fault-based testing, the fault coverage, which is the ration of the number of detected faults to the number of all faults, is commonly used to evaluate the proposed test technique or BIST technique.

1.3. Fault Modeling for Analog Circuits

For IC test, test engineers would not do research on real chip on the wafer or after package on which the real faults exist, because they cannot get the chip at the test design phase, and another reason is that they must predict the possible fault that may happen on the real chip and find test approach to test the possible faults before the

circuit is manufactured. After the circuits are fabricated on a wafer, the design for test is used to determine the possible fault happened or not, and the fault model is the equivalent circuit of the real faulty part that may happen through the process line. Through the fault simulation, test engineers inject these equivalent circuits into the CUT, and then to evaluate the test patterns are effective or not. That is to say, fault models are used to represent the behaviors of the realistic fault in the circuit on wafer, and test engineers use fault simulation to measure the efficiency of their proposed test strategy, test pattern, test equipment or DFT techniques.

A fault is a representation of a defect reflecting a physical condition that causes a circuit to fail to perform in a required manner [1], and the abstraction process of the physical defects is also called as fault modeling, which is to find appropriate equivalent circuit to manifest the effect of the faults. Along the IC production line, photomasks are firstly extracted from the layout information of the circuit, and then the circuit is built on a wafer through the fabrication process according to the masks. Over the physical implementation process, physical defects may happen at every step. At photomask making step, a small localized region or spot is examined as point defect or spot defect which is the process less defect [34].The point defect represents the material presence or absence that result in realistic physical defect at the structure level. Stacking faults, oxide pinholes, and extra or missing pieces of a conductor or semiconductor layer are all considered to be spot defects [37]. Another kind of defects that changes and degrades the performance parameter of the circuit would result from the fluctuation and variation of fabrication process, such as the diffusion time, temperature and so on. Some other examples of physical defects can be found in many works, such as high-resistive short in a metallization layer [15,38], gate oxide short [39], bridging defects, gate-oxide defects and open defects [40]. During the fault modeling the electrical effect of the physical defects are extracted and abstracted to a higher level to manifest the effect of the physical defect.

Based on the previous comment of physical defect, it is common practice to classify analog faults into two categories: catastrophic and parametric faults. Catastrophic faults, also referred to hard faults, are caused by random defects and cause short or open circuits or large-scale deviations of design parameters, like the aspect ratio of the MOS transistor [41]. If defects are sufficient to change the circuit schematics,

then they are classified as hard faults. If defects are too minor to cause hard faults, they are classified as parametric faults, also called soft fault. Soft faults can be further classified into parametric faults and deviation faults. Parametric faults are used to model the variation in the parameter that governs a device in the circuit of interest. Deviation faults refer to changes in the overall performance of the entire circuit of interest [1]. Hard faults and soft faults are not mutually exclusive. One fault may be classified as both a hard fault and a soft fault [1].

Many approaches have been proposed for fault modelling. According to modelling level, approximately three categories can be classified: schematic-based fault modelling, structural fault modelling and behavioural fault modelling. In [36], four levels of abstraction of the circuit are presented: process level, structure level, circuit level and logical level, so a defect can be translated to four levels. In process level, the mask is examined. In structural level, the fault modelling is based on the layout and the technology information of the fabrication process. After the effect extraction in structural level, defects can be mapped to circuit level based on the electrical effect. Finally, the behavior of the CUT with the defects can be simulated to create the behavior fault models based on the effect in the circuit level. This fault modelling process can be implemented by VLASIC [42] and the fault modeling approaches in [43-45] proposed based on the IFA [36]. However, this IFA based fault modelling is a time cost process, a circuit would have different fault lists due to the different layout patterns. Therefore the schematic-based [47-49] fault modelling was proposed to decrease the complexity and time cost of the defect-based fault modelling. The fault list can be directly created based on the schematic analysis of the CUT. In additional, sensitivity computation [50-52] was widely used in parametric fault modelling for analog and mixed-signal circuit.

In this dissertation, due to catastrophic faults cover a wide range of realistic failures [53], so they are mainly considered including shorts and opens in MOS transistors, resistors and capacitors. Shorts were modeled by connecting a small resistor between each pair of terminals [54], including Gate-Drain Short (GDS), Gate-Source Short (GSS), Drain-Source Short (DSS), Resistor Short (RS) and Capacitor Short (CS). Opens were modeled by inserting a parallel combination of a large resistor and a small capacitor in series into each terminal [54], including Drain Open (DO), Source Open

(SO), Resistor Open (RO) and Capacitor Open (CO). Particularly, Gate Open (GO) was modeled by means of grounded parallel combination of a large resistor and a small capacitor at the two disconnecting terminals [54]. These catastrophic faults for an nMOS transistor are illustrated in Fig. 1.3. The injected short small and open large resistors were respectively set to 100Ω and 100MΩ with reference to case in [47], and the small capacitor injected in the open cases was set to 10fF. These values can be changed according to their characteristics, for example the small resistor injected in the short cases, were set to 1Ω in [55,56].

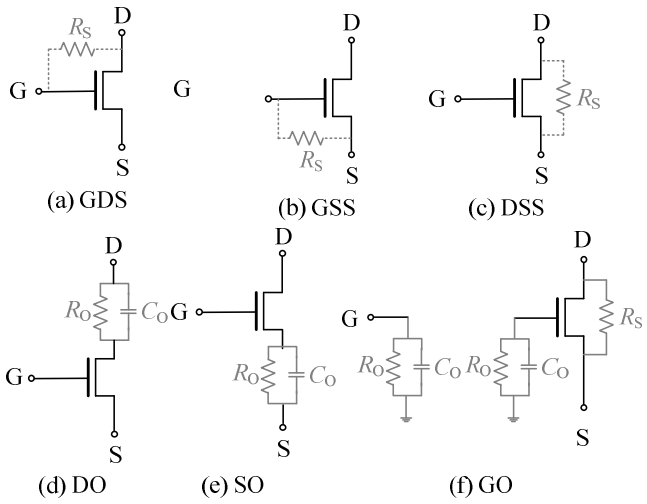


Figure 1.3 Fault models for transistor: (a) GDS, (b) GSS, (c) DSS, (d) DO, (e) SO, (f) GO.

1.4. Dissertation Developments and Organizations

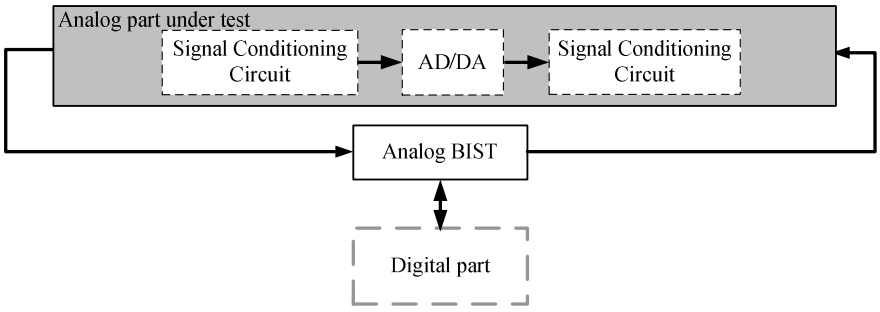
1.4.1. Motivation and Objectives of This Work

The above-mentioned BIST techniques in IC testing have led to the research and development of this dissertation. Although a large number of BIST techniques for circuits have been proposed, only a few of them have been implemented in real chip due the complicated on-chip test circuits, so the simple and compact BIST techniques with low cost are still needed, especially for recent advanced analog and mixed-signal circuits.

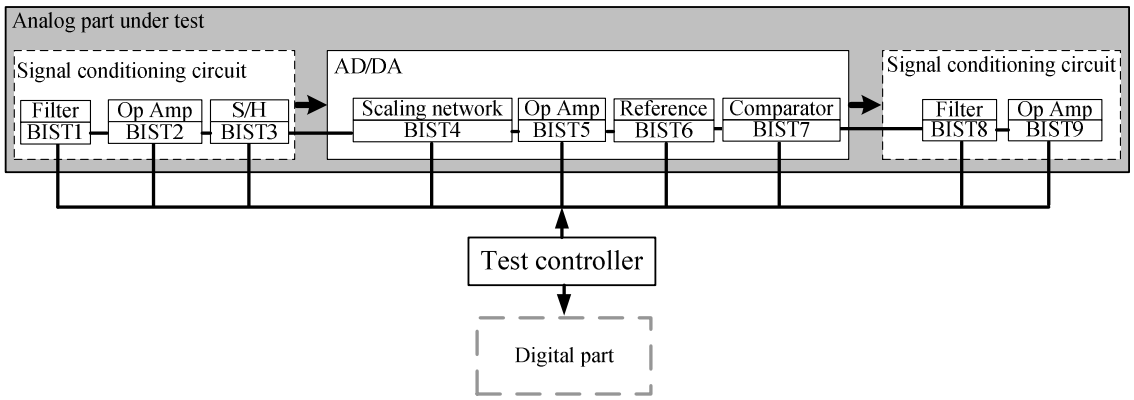
Most existing BIST techniques for analog and mixed-signal circuits are based on the specification measurement, which caused high design complexity of the BIST circuits and long test time. In the analog and mixed-signal testing, many techniques can

not been directly extended to different analog and mixed-signal circuits since they have different structures and different performances, and specific analog circuit requires specific technique. Therefore, this dissertation is aim to get an insight into the fault-based BIST application in analog and mixed-signal systems with the referred fault models in Sect. 1.3, to the proposed effective feasible techniques for data converting systems based on their structural analysis.

For the data converting circuit, the widely used BIST strategy is to test the data converting system like a back-box as it is shown in Fig. 1.4(a), even though the data converting system consists of many circuits with different characteristics and functions. The analog BIST circuit generates test stimuli to the data converting circuit, and observes the outputs to determine the test result. However, this functional BIST strategy would cause low fault coverage due to the limited accessibility and observability, and mask some faults in the internal sub-circuits of the data converting circuit. Hence, the sub-circuit based BIST strategy was proposed and it is illustrated in Fig. 1.4(b). To improve the testability, the data converting circuit is broken into several sub-circuits like



(a) System level test archtechure.



(b) Subcircuit-based test archtechure.

Figure 1.4 Architectures of system-level BIST and sub-circuit based BIST.

filter, Op Amp, scaling network, S/H circuit, comparator or reference. Then, BIST strategies are proposed for each sub-circuit, so all sub-circuit can be tested by its own BIST circuit. However, this kind of divide-and-conquer would cause some problems like performance degradation and area over head, so this sub-circuit based BIST strategy need be improved with the benefit of high testability.

Some BIST circuits for different sub-circuits can be combined to decrease the cost as it is shown in Fig. 1.5, the *BIST1-BIST3* were combined to a new on-chip circuit *BIST_n1*, which can also test the sub-circuits tested by *BIST1-BIST3*. Other new BIST circuits can be created in the same way. Similarly, the new BIST circuit can be recombined, and some sub-circuit under test can also be used to test other sub-circuit. The simplified analog BIST circuit is controlled by the designed internal controller to test all the sub-circuits in the data converting system, the sub-circuits used in Fig. 1.4(a) and Fig. 1.5 are just some examples, not the real configuration of the data converting system.

Additionally, all the designs in this work were implemented using Rohm 0.18 μm CMOS technology provided by VLSI Design and Education Center (VDEC), which is located in the University of Tokyo and shared by users all over Japan.

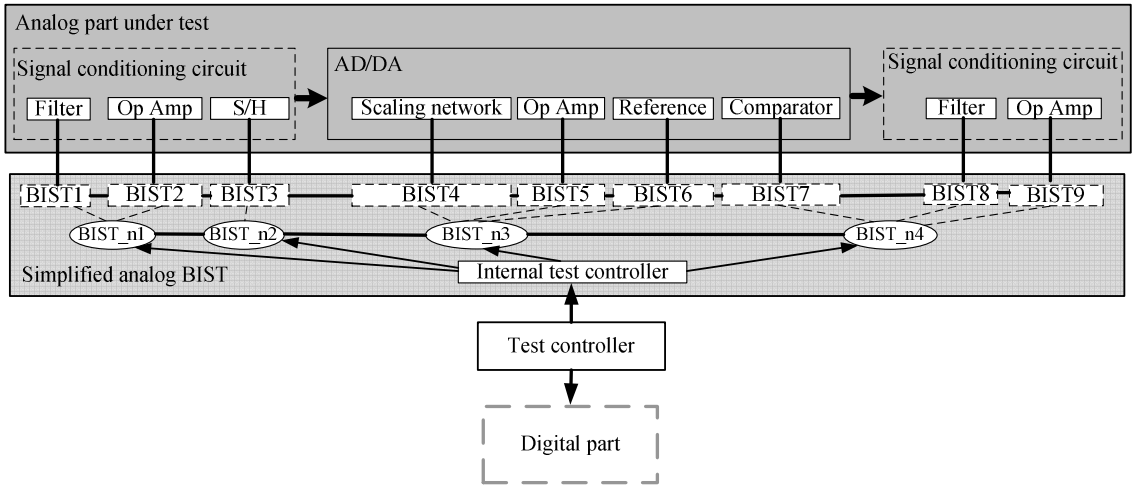


Figure 1.5 The expected simplified sub-circuit-based BIST in this dissertation.

1.4.2. Thesis Organizations

The left of this thesis is organized into four chapters. The following chapter 2 gives the proposed two BIST techniques for Operational Amplifiers (Op Amps). In the first approach, the Op Amp is reconfigured as a voltage follower to excite the possible

defects and the stable (desired) output voltage (SOV) of the transient response is analyzed by SOV checker to determine the test result. Then, In order to improve the fault coverage in Op Amp testing, a two-step BIST scheme and its implementation have also been proposed.

Chapter 3 presents a resistance-matching based BIST technique for current-mode R-2R DAC. This is a re-constructing example of the divide-and-conquer strategy. The SOV checking based test technique proposed in the first chapter was used to test the Op Amp in the R-2R network DAC, and then the resistance-matching based test strategy was employed to test the R-2R network based on the tested Op Amp.

Chapter 4 presents the Common-Mode (CM) BIST technique for Fully-Differential (FD) Sample-and-Hold (S/H) circuits, due to the FD topologies are commonly used to eliminate the clock feedthrough and charge injection to a first order in S/H circuits. The performance of the small CM gain in FD Op Amps is employed to test FD S/H circuits based on the CM setup in this study.

Chapter 5 finally gives the summarization of proposed BIST techniques for data converting circuits and discussions. In addition, the following research will be mentioned for the unfinished parts in the data converting systems.

Chapter 2. BIST Techniques for Operational Amplifier

This chapter presents two fault-based BIST techniques for Op Amps, which are most frequently encountered parts in analog and mixed-signal LSI systems. Without any parameters modification, the BIST techniques based on the stable output value checking of the transient response can be applied to test all the Op Amps in the same analog and mixed-signal system, even the Op Amps are designed with different architectures. Then, to improve the fault coverage, a two-step BIST scheme and its implementation for Op Amp is presented. In addition to the catastrophic faults, the proposed technique can particularly detect the capacitance variation in the compensation capacitor by combining the current-based test with the offset-based test.

Firstly, the overviews of the existing test techniques for Op Amps are given. Then, the BIST techniques based on the stable output value checking of the transient response and the two-step scheme are presented. Finally, the conclusion is drawn.

2.1. Reviews on Op Amp Testing

A variety of test techniques have been proposed for Op Amps, and they are summarized in Table 2.1.

Table 2.1 Existing test techniques for Op Amp.

	Test Strategy	***Works***	***BIST Implemented***
Specification-based	Specification measurement	[57-59]	N/A
Fault-based	Specification measurement	[52,60-65]	[52,60]
	Oscillation-based	[66-70]	[69]
	Electronic variables of Op Amp	[71-74]	[71-73]

The widely utilized scheme is based on the specification measurement [57-59]. In these cases, all the functional parameters of the Op Amp under test are measured and compared with the expected values to determine the test result. However, these specification-based BIST techniques require complex on-chip circuits to implement the

specifications measurement that would cause high test cost, and also result in either excessive or insufficient testing.

The fault-based testing is widely accepted as an alternative to functional testing, and the proposed fault-based techniques for Op Amps can be classified into three categories. First, some functional parameters [52, 60-65] are still used in fault-based testing approaches to detect the possible faults. For example, the Op Amp under test was converted into a voltage follower in [60-62], and the transient response of the voltage follower was analyzed in order to measure the overshoot and slew rate deviation with respect to the fault-free response. However, the parameters of overshoot and slew rate vary among different Op Amps with different architectures, so the designed system must be modified to test other Op Amps, even in the same chip. In [52], an AC and DC compacted testing technique was presented by monitoring the amplitude and offset of voltage signals. However, a sinusoidal wave was employed as test stimulus, which made this technique infeasible for on-chip test since the complex sinusoidal wave generator.

Second, in the oscillation-based test techniques [66-70], the Op Amps under test were converted into an oscillator, and the reconfigured circuit parameters like oscillation frequency and power supply currents were evaluated to detect the possible faults in the Op Amps without any test stimulus. However, the measuring and analyzing circuits of oscillation frequency would be too complex.

Third, some electronic variables related to the Op Amp under test were monitored for fault signature signals. In I_{DDQ} testing techniques [71], the power supply current of the Op Amp under test was monitored by a current sensor in order to determine the current deviation caused by the defects, but it is hard to design a current sensor without performance degradation to the original amplifier. In [72] current signals were employed as test stimuli and injected in two nodes at the output stage of the Op Amp. In [73,74], the built-in DC test signals from the internal nodes were employed to detect the hard-detect fault to the voltage-based test, but the AC analysis on-chip circuit would cause complex circuit design for BIST application.

2.2. The Stable Output Value (SOV) Checking based BIST

Some above-mentioned test techniques have been partially implemented in BIST application, and in some cases, extra test device is still needed to assist the AC analysis

or complex signal generation. Additionally, every Op Amp under test requires a specialized external testing circuit with respect to its parameters, even using the same BIST scheme. Thus, the Stable Output Value (SOV) checking based BIST is presented, and it can test all the Op Amps in a complex analog and mixed-signal system using only one fixed BIST circuit.

2.2.1. Test Strategy and Technique

When a step signal inputs to the voltage follower converted from an Op Amp under test, the output of the voltage follower is called as transient response and it can be observed to measure the performance parameters [75,76] like slew rate, setting time, and phase margin.

The voltage follower configuration of an Op Amp is useful, and many parameters can be captured and calculated from the transient response. Therefore, transient response can be chosen as a monitoring subject to test Op Amp for its high information containing. As a fault happened, the parameter deviations of slew rate, setting time or phase margin can be reflected from the transient response distortion. Hence, the fault can be detected by observing the transient response.

Figure 2.1 shows some examples of transient responses deviation with reference to the fault-free response. If the distortions of transient response can be extracted, the existing faults in the Op Amp under test can be easily detected. In work [60-62], parameters of slew rate and overshoot were chosen as test variables of deviation reflection to declare the transient response distortion. However, the faults, which caused transient response distortion like the faulty response-6, can not be detected by measuring slew rate and overshoot because the slew rate and overshoot variables did not deviate or was changed a little, but it can be detected by observing the SOV of the transient response.

The transient response finally rose or fell to a stable voltage value with a little propagation delay according to the input step signal, which skipped from an initial voltage to another stable voltage. For a fault-free Op Amp, the SOV should be equal to the final stable voltage of the input step signal. For this reason, the SOV is considered as an alterative test variable to test the Op Amp.

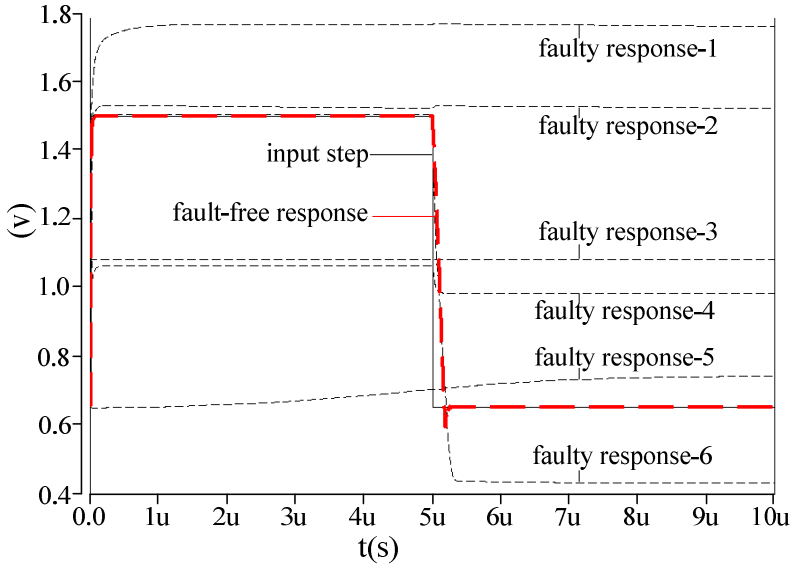


Figure 2.1 Transient responses of a voltage follower configured from the Op Amp.

With reasonable accuracy assuming, most Op Amps configurations can be modeled as a second-order system. The general second-order system in the frequency domain can be described as Eq. 2.1 [75]

$$A(S)=V_o(s)\Big/V_{in}(s)=\pm\frac{A_0\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}=\pm\frac{A_0\omega_0^2}{s^2+\left(\omega_0\Big/Q\right)s+\omega_0^2} \tag{2.1}$$

where

A_0 is the low-frequency gain,

$\omega_n=\omega_0$ is the pole frequency in radians per second,

ζ is the damping factor $1/(2Q)$, and Q is the pole.

Then, the Op Amp under test is converted to a voltage follower shown in Fig. 2.2, the general response to the step signal V_i in time domain can be written as

$$V_o(t)=A_{CL}\left[1-\frac{1}{\sqrt{1-\zeta^2}}e^{-\zeta\omega_n t}\sin\left(\sqrt{1-\zeta^2}\,\omega_n t+\phi\right)\right]\bullet V_i(t) \tag{2.2}$$

where $A_{CL}=A_0\Big/(A_0+1)$ is the closed-loop gain.

Since the gain A_0 is large enough for Op Amps and the term $e^{-\zeta\omega_n t}$ would become

approximately zero with the time increase. After the transient response stabilized, Eq. 2.2 can be simplified as $V_o(t) \approx V_i(t)$, so the SOV is almost determined by the step input for a fault-free Op Amp, so only one fixed SOV observation BIST circuit can test all Op Amps in an analog and mixed-signal system using a single step input.

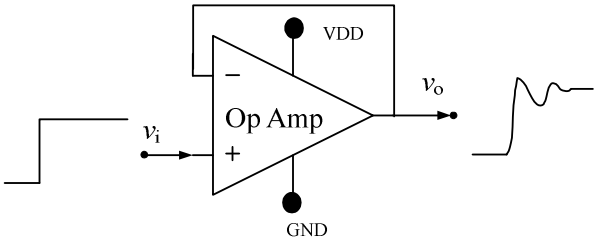


Figure 2.2 Voltage follower configuration of an Op Amp.

2.2.2. The SOV Checking based Test System Implementation

Figure 2.3(a) depicts the BIST system architecture of the proposed SOV checking based test scheme, and the proposed BIST circuit is composed of a step signal generator, a SOV checker and logic control signals. During the test, the Op Amp under test is converted into a voltage follower by setting V_{TM} to logic '1', and then positive or negative step signal, generated by a on-chip stimulus generator, is input to the voltage follower. After this, the SOV checker observes the transient response V_{tr}, checks the SOV and generates a digital test result $V_{p/f}$. If $V_{p/f}$ is logic '0', the CUT is determined as a faulty circuit, otherwise a fault-free circuit. The whole testing process is controlled by V_{TM} and the *Control Signals*. In the multi-Op Amp system shown in Fig. 2.3(b), the control signal *Op_s* was added to choose Op Amp to be tested.

Figure 2.4(a) shows a step signal generator including two parallel pMOS transistors M1 of 3.4/0.4 μm (W/L) and M2 of 2/0.4 μm (W/L), and a resistor of 3.35kΩ. When input signal V_{tin} is set to logic '1', M2 is off, only M1 works, and the output V_{tout} is about 0.606V. On the other hand, when V_{tin} is set to logic '0', not only M1 but also M2 works, so the output V_{tout} changes to 1.202V. As a consequence, a step signal can be generated by switching the input of V_{tin}.

Figure 2.4(b) shows the circuit configuration of a SOV checker, which consists of two window comparators, two *NAND* gates and a *XOR* gate. Table 2.2 lists the aspect

ratio (W/L) settings of all transistors in the SOV checker.

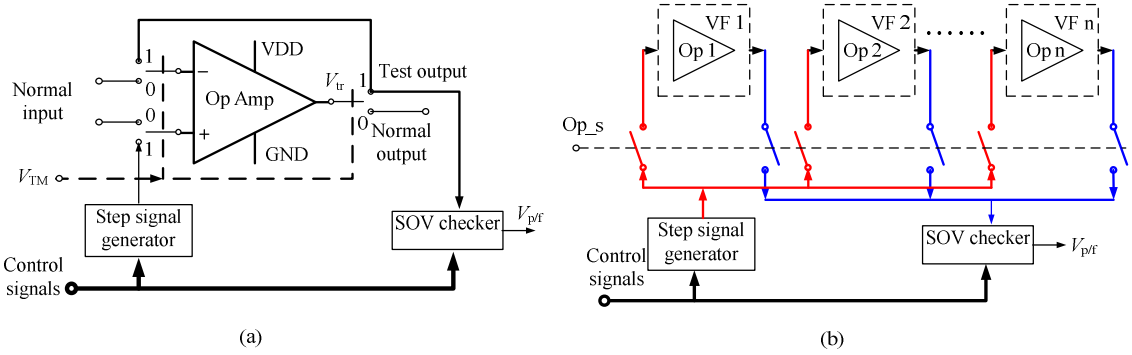


Figure 2.3 The proposed SOV checking based BIST architecture: (a) The single Op Amp case. (b) The multi-Op Amp case.

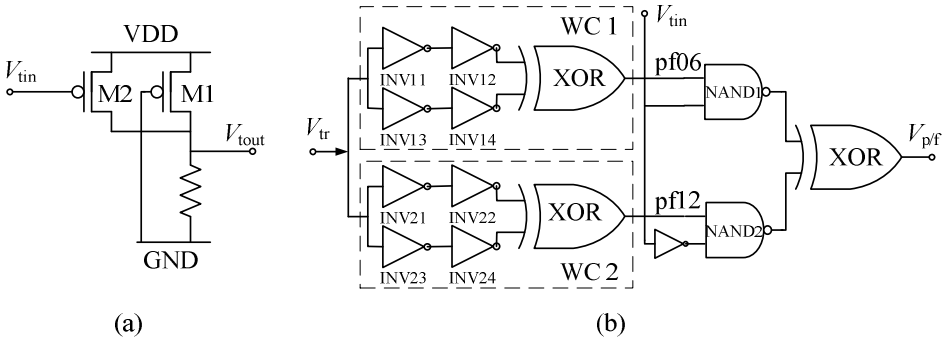


Figure 2.4 The BIST circuit configuration: (a) A step signal generator. (b) A SOV checker.

Table 2.2 Summary of elements parameters in the SOV checker shown in Fig. 2.4(b).

Elements	***W/L (μm)***	***Elements***	***W/L (μm)***
pMOS in INV11, INV12	0.6/0.4	pMOS in INV21, INV22	36 /0.4
nMOS in INV11,INV12	4 /0.4	nMOS in INV21, INV22	0.6/0.4
pMOS in INV13,INV14	0.6/0.4	pMOS in INV23, INV24	33 /0.4
nMOS in INV13, INV14	2.4/0.4	nMOS in INV23, INV24	0.6/0.8
Others in Fig. 2.4(b)	0.54/0.18	--	--

Owning to the process variation, the SOV cannot be exactly constant but fluctuates within a range according to the input step signal. Hence, the SOV checker checks the SOV in a range not a single value based on the Monte Carlo simulation results with

transistor size variation of a maximum fluctuation of 5%.

Under test mode, firstly the transient response V_{tr} shown in Fig. 2.4 (b) is simultaneously transmitted to two parallel window comparators of *WC1* and *WC2*. As it can be seen from Fig. 2.5, If V_{tr} is in the checking region from 0.59V to 0.626V, *WC1* outputs a logic high voltage, otherwise outputs a logical low voltage. In the same way, *WC2*'s checking region is from 1.188V to 1.219V. In a word, when the V_{tr} is within the reference checking regions, the window comparator will output a logical high voltage.

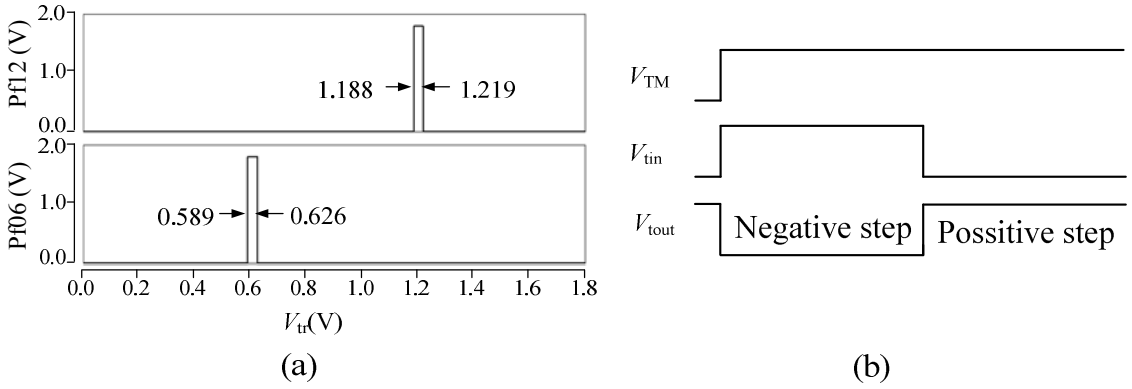


Figure 2.5 (a) The checking regions of *WC1* and *WC2*. (b) Control and data signals settings for test.

Then, the outputs of the two window comparators are separately transmitted to two *NAND* gates controlled by V_{tin}. When V_{tin} is logic '1', the output of *WC1* is valid and transmitted to the *XOR* gate to finally generate the test result $V_{p/f}$ through *NAND1*, while the output of the *WC2* is blocked by *NAND2*. On the other hand, the output of *WC2* is valid and alternatively transmitted to the *XOR* gate.

As it was previously stated, the operation of the step signal generator and the SOV checker are controlled by V_{TM} and V_{tin}. V_{TM} converters the Op Amp under test into test mode and reconfigures it as a voltage follower, and then V_{tin} controls the step generator to form a step signal shown in Fig. 2.5(b) and the SOV checker to generate a valid test result $V_{p/f}$. Additionally, to simplify the test circuit, time delay element wasn't applied in this work to generate step signal, but a step generation controlling signal V_{tin} was added.

2.2.3. Simulation Results

To evaluate the proposed SOV checking based BIST architecture, three Op Amps

have been considered as test vehicles with different architectures. They are two-stage Op Amp, folded-cascode Op Amp and buffered Op Amp [75], and shown in Fig. 2.6, Fig. 2.7 and Fig. 2.8. The element sizes of the three Op Amps are listed in Table 2.3. In order to focus on the basic architecture of the Op Amps under test, the current biasing circuits were simplified to a pMOS transistor. In the case of complicated biasing circuit, the biasing circuit should be tested by the designed BIST circuits, even though the faulty biasing pMOS would reflect some faulty behaviors of other complicated biasing circuits.

Those three Op Amps with the proposed BIST system were laid out using Rohm CMOS 0.18-μm technology in Cadence environments and simulated by HSpice. As it is shown in Fig. 2.9, the proposed BIST circuit caused extra approximately 6.2% area overhead to the original three Op Amps.

With reference to the listed catastrophic fault models for transistor, resistor and capacitor in Sect. 1.3, the faults were injected into the each Op Amp under test to evaluate the proposed BIST technique. In the case of two-stage Op Amp, 49 faults were detected in the total 52 faults, with fault coverage of approximately 94.2%. The undetected faults are the short faults in the compensation resistor R_C and capacitor C_C, and the GO in M8 shown in Fig. 2.6. Although the GO in the current biasing pMOS M8 changed the bias current that would degrade gain, it did not significantly change the SOV of the transient based on the voltage follower configuration of the two-stage Op Amp under test.

In the cases of the folded-cascode Op Amp, 80 faults of the total 93 injected faults were detected with the coverage of approximately 86%. In the cases of the buffered Op Amp, 131 faults were injected in the circuit, and 119 faults were finally detected with the fault coverage of approximately 91%. In the folded-cascode and buffered Op Amps, the main hard-detected faults exist in the cascode current mirrors, since they still can provide an almost constant current, even the faults happened. In addition, the GO of the current biasing pMOS and the faults in the compensation circuit were not detected by the checking the SOV of the transient response, since they change the Op Amp's characteristics in frequency domain.

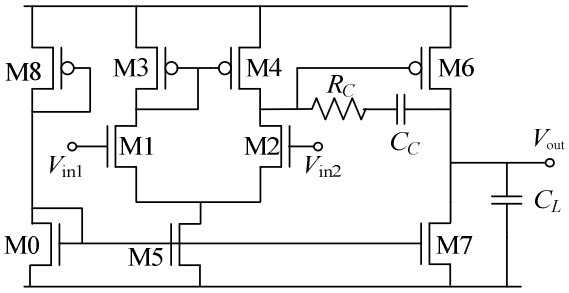


Figure 2.6 The circuit configuration of the two-stage Op Amp.

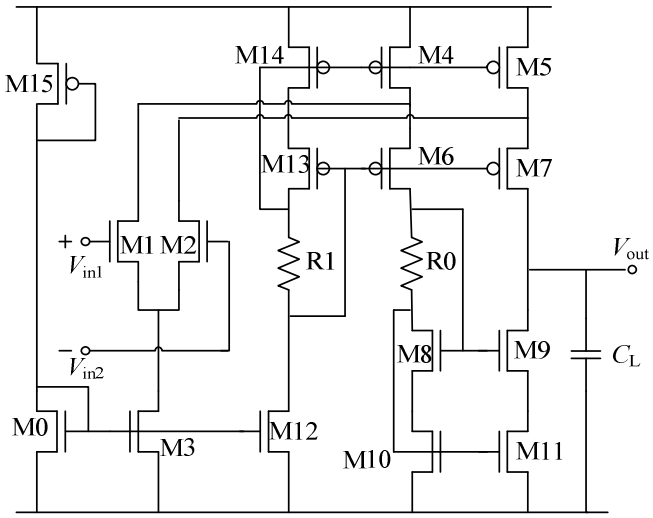


Figure 2.7 The circuit configuration of the folded-cascode Op Amp.

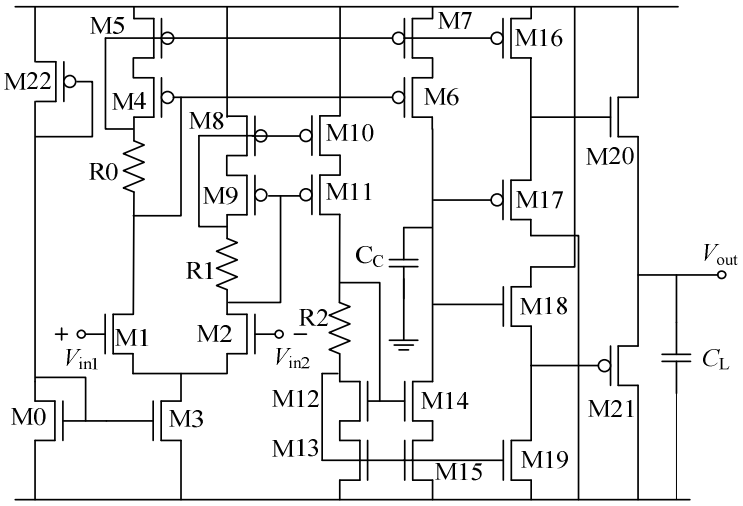


Figure 2.8 The circuit configuration of the buffered Op Amp.

Table 2.3 Summary of elements parameters of the three Op Amps.

Op Amp	*Elements*	*Size (unit)*	*Elements*	*Size (unit)*
Two-stage Op Amp Shown in Fig. 2.6	M0, M5	5.4/0.4 W/L(μm)	M1, M2	12/0.4 W/L (μm)
	M3, M4	10.2/0.4 W/L(μm)	M6	34/0.4 W/L (μm)
	M7	9/0.4 W/L(μm)	M8	0.8/0.4 W/L (μm)
	R_C	18 kΩ	C_C	0.8 pF
	C_L	10 pF	--	--
Cascode Op Amp Shown in Fig. 2.7	M0, M3	12/0.4 W/L(μm)	M1, M2	39.8/0.4 W/L (μm)
	M4-M7, M13, M14	38.8/0.4 W/L(μm)	M8-M11	12.8/0.4 W/L (μm)
	M12	10/0.4 W/L(μm)	M15	4/0.4 W/L (μm)
	R0, R1	5 kΩ	C_L	10 pF
Buffered Op Amp Shown in Fig. 2.8	M0, M3	5.4/0.4 W/L(μm)	M1, M2	32/0.4 W/L (μm)
	M4-M11, M17	36/0.4 W/L(μm)	M12-M15	16.8/0.4 W/L (μm)
	M16	12/0.4 W/L(μm)	M18, M21	40/0.4 W/L (μm)
	M19	5.6/0.4 W/L(μm)	M20	14/0.4 W/L (μm)
	M22	4/0.4 W/L(μm)	C_C	1.4 pF
	C_L	1 pF	--	--

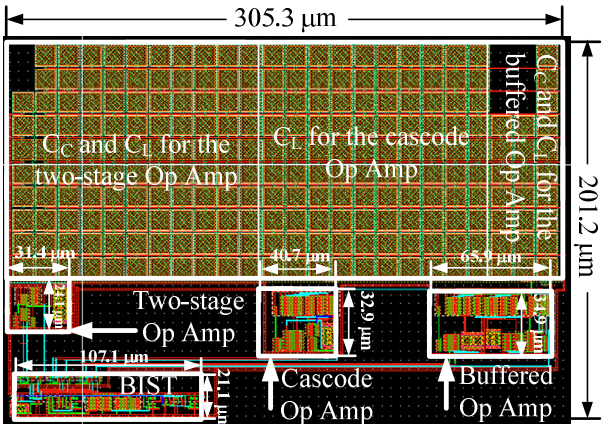


Figure 2.9 The layout pattern of the three Op Amps with the BIST circuits.

The comparisons of performances between the three original Op Amps and them with the BIST circuit shown from Table 2.4 to Table 2.6 indicate that the on-chip test circuits did not cause significant performance degradation, because the BIST circuit

would be disconnected to the CUTs by turning off the analog switches.

Table 2.4 Performance parameters of the original two-stage Op Amp and the two-stage Op Amp with inclusion of the BIST circuit.

Two-stage Op Amp	***Simulated Values***	
Performances	***Original Op Amp***	***Op Amp with BIST***
Offset Voltage	-80 μV	-80 μV
DC Gain	74.218 dB	74.205 dB
Unity Gain Bandwidth	25.336 MHz	25.254 MHz
Phase Margin	66.34 Degree	65.154 Degree
Slew Rate	+60.12/-4.83(V/μS)	+56.2/-4.9 (V/μS)
|Power Supply Rejection Ratio+/-|	96.94 dB /99.74 dB	96.937 dB /99.746 dB

Table 2.5 Performance parameters of the original folded-cascode Op Amp and the folded-cascode Op Amp with inclusion of the BIST circuit.

Folded-cascode Op Amp	***Simulated Values***	
Performances	***Original Op Amp***	***Op Amp with BIST***
Offset Voltage	-0.4 mV	-0.4 mV
DC Gain	70.492 dB	70.492 dB
Unity Gain Bandwidth	9.187 MHz	9.183 MHz
Phase Margin	87.667 Degree	86.617 Degree
Slew Rate	+6.59/-7.77 (V/μS)	+6.22/-7.56 (V/μS)
|Power Supply Rejection Ratio+/-|	95.65 dB /96.49 dB	96.646 dB /96.32 dB

Table 2.6 Performance parameters of the original buffered Op Amp and the buffered Op Amp with inclusion of the BIST circuit.

Buffered Op Amp	***Simulated Values***	
Performances	***Original Op Amp***	***Op Amp with BIST***
Offset Voltage	60 μV	60 μV
DC Gain	45.37 dB	45.374 dB
Unity Gain Bandwidth	36.314 MHz	36.137 MHz
Phase Margin	74.8 Degree	71.247 Degree
Slew Rate	+44.98/-42.58 (V/μS)	+44.37/-41.1 (V/μS)
|Power Supply Rejection Ratio+/-|	68.904 dB /76.586 dB	68.904 dB /76.586 dB

2.2.4. Conclusions

This section has proposed a BIST scheme for Op Amp, and it can test all the Op Amps in the same chip, even these Op Amps are designed with different architectures. Throughout the test procedure, the possible faults can be detected by checking the SOV of transient response. Seen from the simulation results of the three test vehicles, the proposed test BIST system with fixed parameters setting can test the Op Amps with high fault coverage. Therefore, the proposed scheme can be an alternative and effective test approach for Op Amps in the same analog and mixed-signal system.

2.3. A Two-Step BIST Technique for Op Amp

The transient response analysis based test techniques are the most feasible for BIST technique, but some slight performance parameters deviations are still hard to be captured because of the feedback network, that is to say the difference between faulty response and fault-free responses is too small to distinguish the faulty responses from the fault-free response by the on-chip test circuits. Thus, another feasible two-step BIST technique for Op Amp was proposed to improve the fault coverage, specifically for the compensation circuit. At the first offset-based test stage, a DC voltage is employed as test stimulus to the Op Amp configured as comparator. Then, at the second current-based test stage, a step current is injected to the compensation circuit to mainly excite the faults in the compensation circuit. In addition to the catastrophic faults, the proposed technique can particularly detect the capacitance variation in the compensation capacitor by combining the current-based test with the offset-based test. The circuit-level simulation results of the proposed BIST scheme are presented to demonstrate the feasibility of the proposed BIST scheme with high fault coverage of 98%.

2.3.1. The Two-Step Test Strategy

The input offset voltage of an Op Amps with differential inputs and single-ended output is defined as the differential input voltage for which the DC output voltage is midway between the supplies. The offset voltage of an Op Amp is composed of two components: the systematic offset and the random offset. The former results from the design of the circuit and is present even when all the matched devices in the circuit are identical, the latter results from mismatches in supposedly identical pairs of devices [77].

It can be seen from Fig. 2.10, an offset compensation voltage V_{os} must be added to compensate the output value to the approximate midway between the supplies due to the impact of the mismatches in the Op Amp; otherwise the DC value of V_{out} might be driven to the positive or negative power supply. In fact, in order to meet the acceptable offset voltage in some applications and also to make the transistors operate in saturation region, the DC output V_{out} should be located between power supplies even without the external offset compensation. Therefore, the offset-based test can be employed, the V_{out} is considered as test variable to monitor the mismatch changes caused by physical defects when the inputs of Op Amp are connected to a test reference voltage V_t at approximate midway between the supplies.

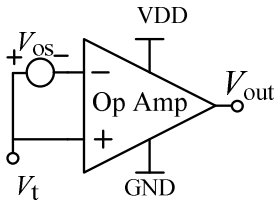


Figure 2.10 The offset compensation for an Op Amp.

At the offset-based test stage, some faults are still hard-detected, especially for the compensation circuit. These faults can be detected by checking the frequency-domain parameters like open loop gain, phase margin and unity-gain bandwidth, but on-chip test circuits for measuring frequency-domain parameters would be difficult to implement due the complexity, and also lead to unacceptable area overhead. Therefore, an alterative transforming test [75] is employed to measure the overshoot in transient response to reflect phase margin deviation. However, some faults just cause a slight slew rate and overshoot deviation in the transient response, and so some hard-detected faults of offset-based test are still hardly detected by the transient test, since the on-chip testing circuit is hard to observe this kind of slight deviation. For the purpose of increasing the deviation caused by the faults in the compensation circuit, a current-based test stage is employed to detect the hard-detected faults of the offset-based test stage.

In the current-based test stage, the current is directly injected to compensation circuit, so the deviation caused by the possible faults in the compensation circuit can be utmost reflected on the output of the Op Amp under test. Figure 2.11 shows the

comparisons of the fault-free output response and the faulty responses. *Fault_1* and *fault_2* are short and 50% capacitance variation of the compensation capacitor, respectively. The Op Amp was simulated under current-based test based on the configurations of current-based comparator, voltage follower and comparator, respectively. The injected current in the current-based comparator configuration caused greatest differences between faulty responses and fault-free response, so the hard-detected faults can be easily detected through differentiating the faulty responses from the fault-free response. Consequently, in order to increase fault coverage the offset-based and current-based tests are combined to test the Op Amp.

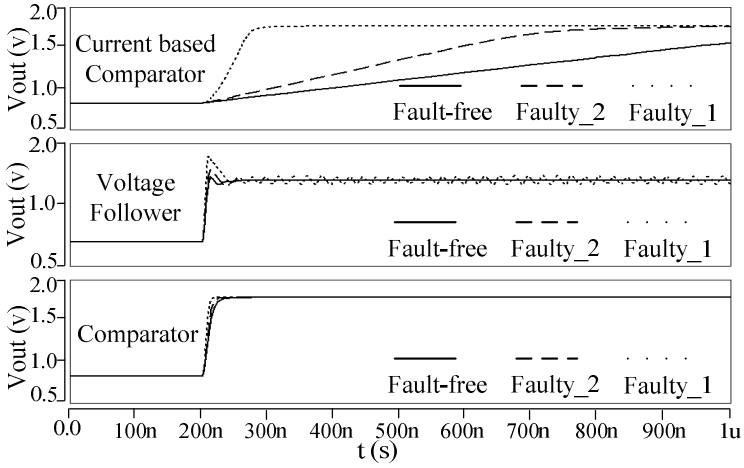


Figure 2.11 The output responses of the Op Amp under current-based comparator, voltage follower and comparator configurations.

2.3.2. The Two-Step Testing System and Its Implementation

Figure 2.12 depicts the Op Amp with the proposed BIST architecture, which is composed of a stimulus generator, response analyzer and isolation circuits of analog switches controlled by external control signals *TM* and *TMC*, which control the whole test procedure. In an analog and mixed-signal system, these two controlling signals can be provided by the digital block on the same chip. *TM* is the test start signal and *TMC* was designed to connect test current to the injecting node to form a test step current.

Figure 2.13 shows the output response of the faults simulation. The marked real line represents the fault-free response when the test voltage V_t is fed to the two inputs of the Op Amp under test at offset-based test step, and then the step current I_t is injected to the

compensation circuit at the current-based test step. The other dotted lines represent the faulty output responses with faults injection, including capacitance variation of the compensation capacitor. In the offset-based test stage, the DC output deviation is monitored, and then the current-based stage is started by signal *TMC* to inject the step current and the output changing rate is monitored by the on-chip checking circuit. Following the input step current the output DC voltage rises to another stable value in a short time interval, which is called propagation delay. In real application, it is impossible to precisely measure the DC output due to the process variation, so ±10% fluctuation of

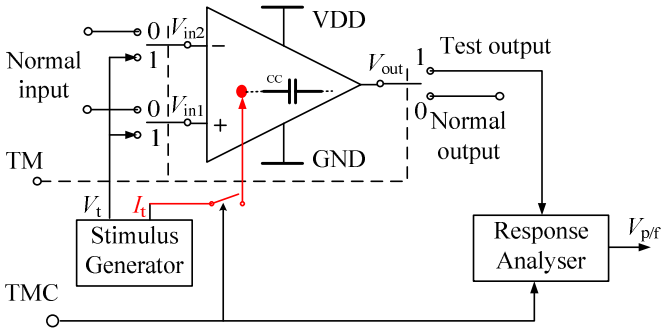


Figure 2.12 The proposed two-step BIST architecture.

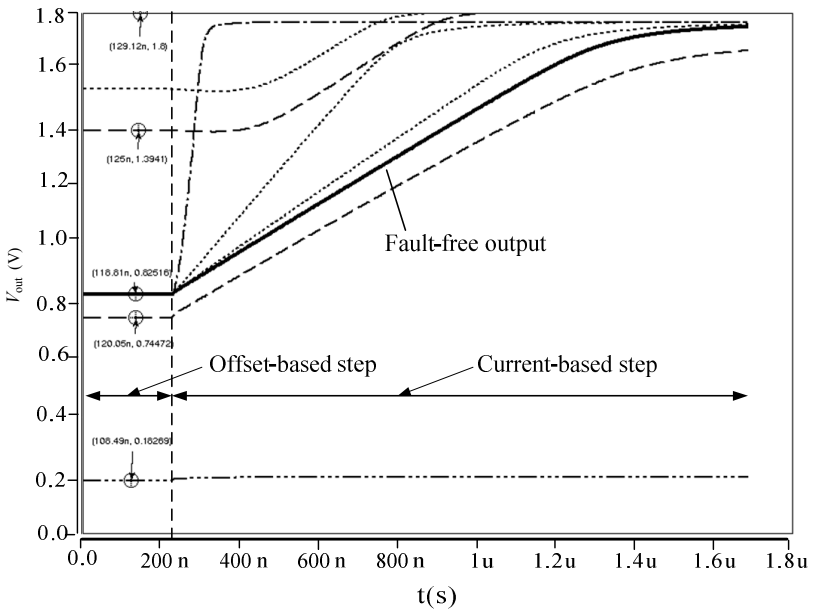


Figure 2.13 Output responses of the proposed two-step test scheme.

the fault-free output is set as the acceptable band for the offset-based test, and ±10% fluctuation of the rising slop is set as the acceptable band to check the deviation at the current-based test stage.

The whole test procedure is shown in Fig. 2.14. Initially, *TM* starts the test by connecting the inputs of V_{in1} and V_{in2} to V_t shown in Fig. 2.12, and output V_{out} to the response analyzer, respectively. If the output is in the expected range in the offset-based test step, the Op Amp passed the offset-based test, otherwise the Op Amp failed the offset-based test and the whole test procedure is terminated. Then, the test current is injected to the compensation circuit, and the propagation delay test circuit is activated to monitor the output changing rate based on the DC output in the offset-based test step. Note that the test result of the offset-based test stage affects the current-based test by clearing or enabling the counter in order to generate a combinational test result signal.

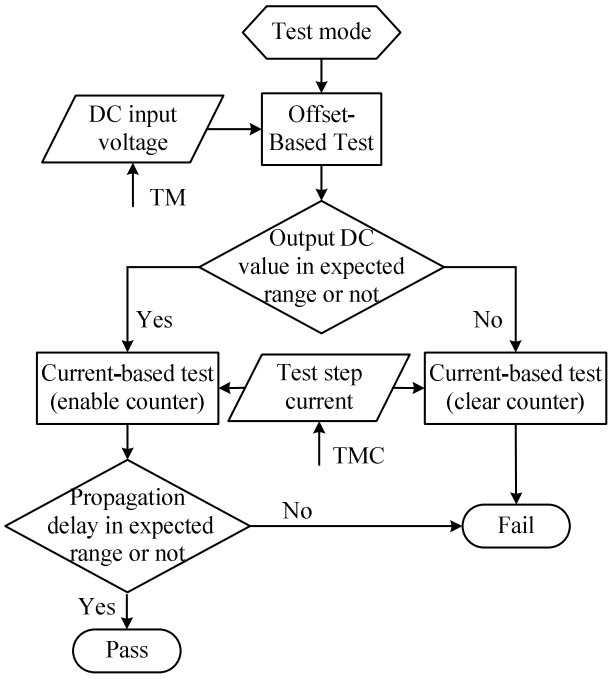


Figure 2.14 The test procedure of the proposed two-step test scheme.

During the propagation delay, the output of the Op Amp moves from the previous stable value to another stable value according to the change of the step current input. After the test current inputs to the test node, the output of the Op Amp cannot immediately skip to another stable value owning to compensation capacitor and the

parasitic capacitance of the transistors, so the propagation delay time can be employed to detect the variation of the compensation capacitor and the parasitic capacitance of the transistors.

Figure 2.15 shows the stimuli generator including a voltage divider and a mirror current sink. The voltage divider is composed of transistors of MS0 of 2.6/0.4 μm (W/L) and MS1 of 0.6/0.4 μm (W/L). The mirror current sink consists of MS2 of 12/0.4 μm (W/L), MS3 of 0.54/0.4 μm (W/L) and MS4 0.54/0.4 μm (W/L). When *TM* starts the test, the output V_t of 0.9V is connected to the inputs of V_{in1} and V_{in2}, and at the beginning of the current-based test, the 0.74μA sink current I_t is passed to the compensation circuit.

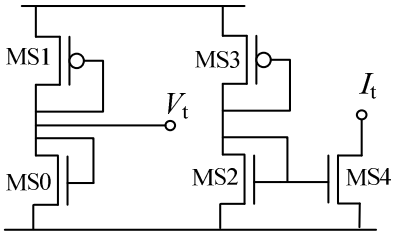


Figure 2.15 The circuit configuration of the stimulus generators.

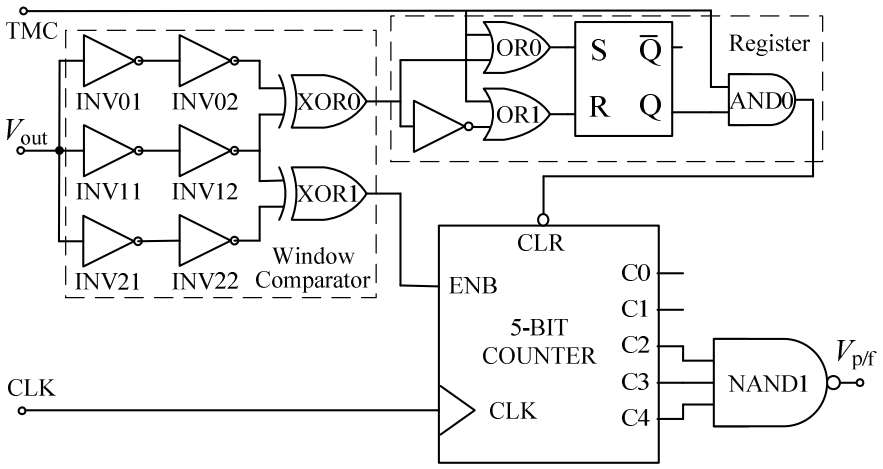


Figure 2.16 Block diagram of the designed response analyzer.

Figure 2.16 depicts the block diagram of the designed output response analyzer including three main blocks: two window comparators, a register and a 5-bit counter. The first window comparator consists of an exclusive OR gate of *XOR0* and four

inverters of *INV01*, *INV02*, *INV11* and *INV12*, and the second one consists of an exclusive *XOR1* and four inverters of *INV11*, *INV12*, *INV21* and *INV22*.

As it is shown in Fig. 2.17, according to the two thresholds, the window comparators were designed to check the output value in the expected band or not and finally create a comparing result. In order to realize the band checking, the aspect ratios of the transistors in the inverters are summarized in Table 2.7, and other transistors used in the response analyzer were set to the aspect ratio of 0.54/0.18 μm (W/L).

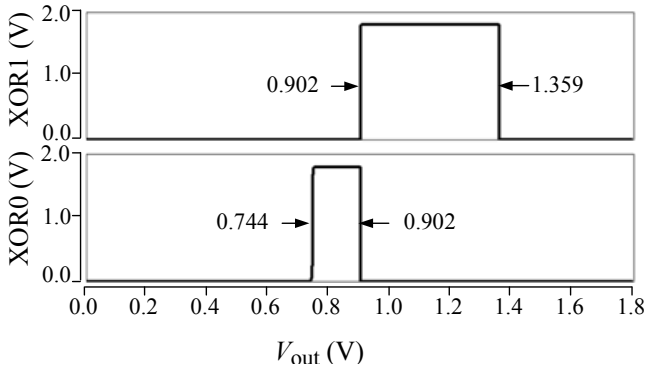


Figure 2.17 The checking band of the two comparators.

Table 2.7 The design of inverters used in window comparators.

Elements	***W/L of pMOS (μm)***	***W/L of nMOS (μm)***
INV01, INV02	0.54/0.4	0.56/0.4
INV11, INV12	2.4/0.4	0.54/0.4
INV21, INV22	40/0.18	0.5/10

The register, consisting of a set-reset latch, two OR gates, an AND gate and an inverter, was designed to store the result of the offset-based test step and then to control the following current-based test step. In the offset-based test stage, the output of *SR* latch indicates the result of the offset-based test. If the Op Amp under test failed the offset-based test, *SR* latch outputs a digital low voltage and, otherwise the current-based test stage is activated by switching *TMC* to high logic, which forces SR latch to store the result of the offset-based test stage at the current-based test stage.

Additionally, the gate *AND0* was designed to combine the offset-based and current-based test stages. Figure 2.18 shows the test operations of the proposed two-step

BIST circuits, when *TMC* is low, the result of the offset-based test is stored in the *SR* latch, so *AND0* outputs a digital low voltage to *CLR* to clear the counter, because *TMC* forces *AND0* output a low voltage. Then, *TMC* goes to high, so the result of offset-based test can be transmitted to *CLR* to control the next current-based test stage. If the Op Amp under test failed the offset-based test, the output of *AND0* would force the 5-bit counter to output logic low voltage at current-based stage, and the test result signal $V_{p/f}$ is derived to high. If not, the final test result depends on the propagation delay time checking in the current-based test step.

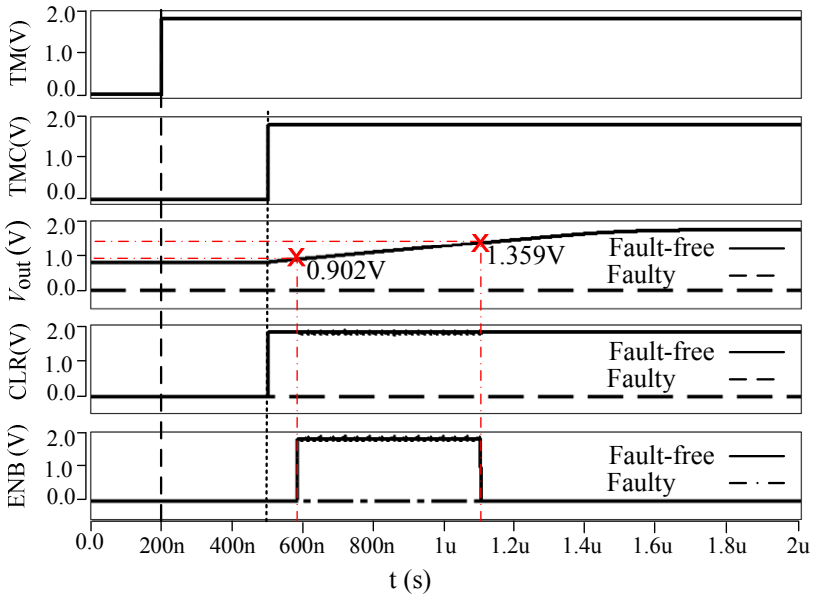


Figure 2.18 Timing waveforms of the BIST system operations.

The 5-bit counter is composed of 5 *T* edge-triggered flip-flops with clear signal *CLR*. Logic low *CLR* forces the outputs *C0-C4* to logic low, and the enable signal *ENB* enables the counter count the edged-triggered input squared clock. The 5-bit counter was designed to measure the propagation delay by connecting the *CLR* and *ENB* to the output of the register and the second comparator, respectively.

In CMOS technology, it is difficult to precisely measure propagation delay time for the fluctuating initial and final voltage due to the process variation. Thus, in this case the time interval is chosen to differentiate the faulty output from the fault-free output. Two observing values must be set in advance to measure the time interval, and the smaller observing voltage should be greater than the bigger boundary value of the

acceptable offset-based test band and the greater observing voltage should be smaller than the acceptable output according the current input. The two voltage observing values are setting by the thresholds of the second window comparator.

Additionally, the frequency of the input clock must be accurately selected. For a fault-free Op Amp, after the two test steps the highest three bits of the 5-bit counter, *C2-C4* must be "111", so that the frequency F_{clock} can be described as

$$(25-3)/TN \le F_{clock} \le 25/TN \tag{2.3}$$

where *TN* is the normal time interval according to the checking voltage range for the fault-free Op Amp.

As it is shown in Fig. 2.19, *T0* is the mentioned normal time interval *TN*, and *T1* is a faulty time interval. Owing to the process variation, F_{clock} should be set between $(2^5\text{-}3)/T0$ and $2^5/T0$, for instance it was set to $30.5/T0$.

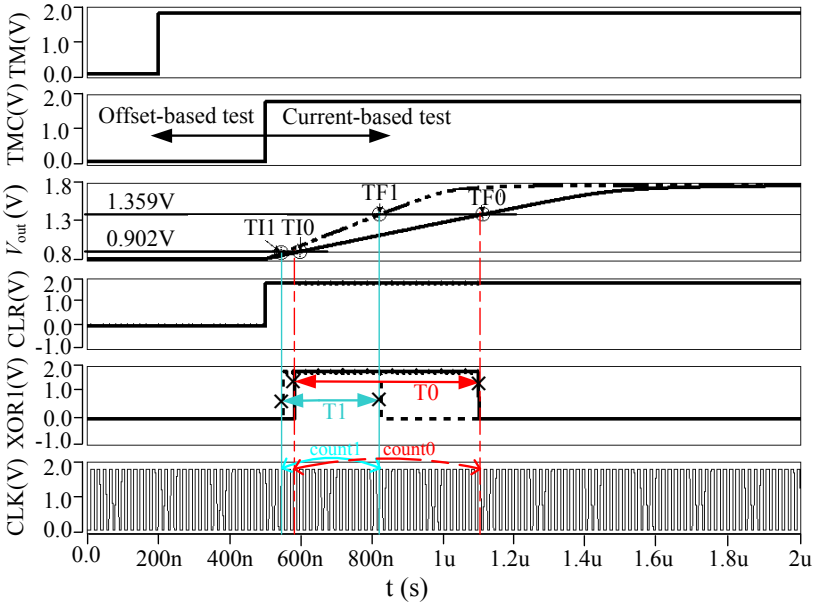


Figure 2.19 The slop detection in the current-based test stage.

The test flow starts by setting *TM* to logic high, and then the current-based test is activated by changing *TMC* to logic high. The two test steps are combined by the register to generate the final test result $V_{\text{p/f}}$. If the Op Amp passed the test, $V_{\text{p/f}}$ should change to digital low after the activation of the current-based test, otherwise the $V_{\text{p/f}}$

remains the digital high. At last, the test ends by recovering *TM* and *TMC* to logic low.

2.3.3. Simulation Results

In addition to the mentioned catastrophic faults in Sect. 1.3, the parametric faults in the compensation capacitor were also considered. Because of the special physical implementation of the capacitor, which is constructed by parallel combination of smaller unit capacitors in CMOS technology, the open in a smaller unit capacitor cannot be reflected by the simple open fault of capacitor like DO or GO in transistors. Thus, the possible Parallel Capacitor Opens (PCO) was modeled as capacitance variation based on the unit capacitance of the smaller unit capacitor used in the Rohm CMOS 0.18 μm technology.

To evaluate the proposed two-step BIST technique, a two-stage Op Amp shown in Fig. 2.20, was considered as test vehicle, and its element parameters are list in Table 2.8. Under the test mode, the inputs V_{in1} and V_{in2} are connected to the output V_t of the stimuli generator shown in Fig. 2.15. The test step current is injected to the Op Amp through I_t.

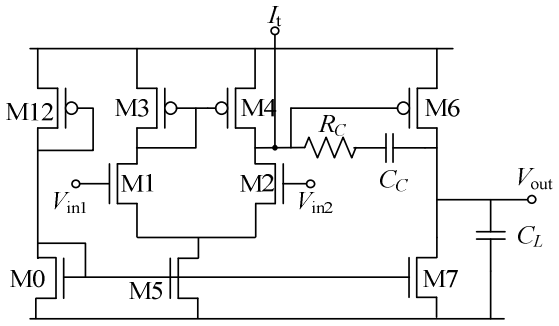


Figure 2.20 The circuit configuration of the two-stage Op Amp under test with inclusion of design for test.

Table 2.8 Summary of elements parameters for the two-stage Op Amp shown in Fig. 2.20.

Elements	*Size (unit)*	*Elements*	*Size (unit)*
M0, M5	5.4/0.4 W/L(μm)	M1, M2	12/0.4 W/L(μm)
M3, M4	10.2/0.4 W/L(μm)	M6	34/0.4 W/L(μm)
M7	9/0.4 W/L(μm)	R_C	18 kΩ
C_C	0.8 pF	C_L	8 pF

The two-stage Op Amp with on-chip BIST circuits was laid out using Rohm CMOS 0.18-μm technology in Cadence environments and simulated by HSpice. As it is shown in Fig. 2.21, due to the 5-bit counter the designed BIST circuits caused a large area cost compared to the transient response test, but the area overhead ratio of the BIST circuits to the original circuit would be decreased when the proposed BIST scheme is applied to a more complicated system, and the 5-bit counter can also be used by other parts.

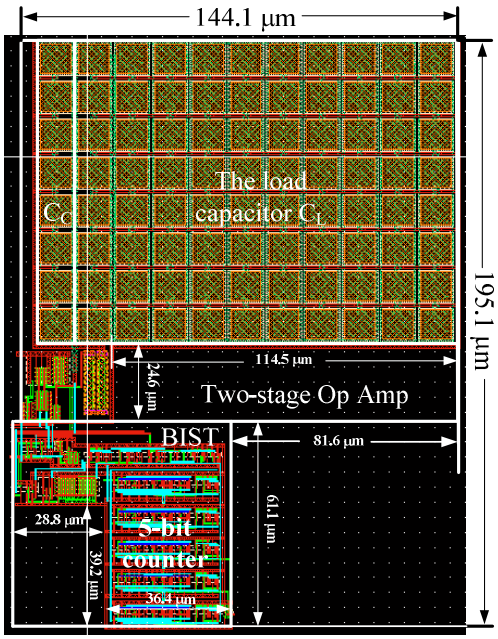
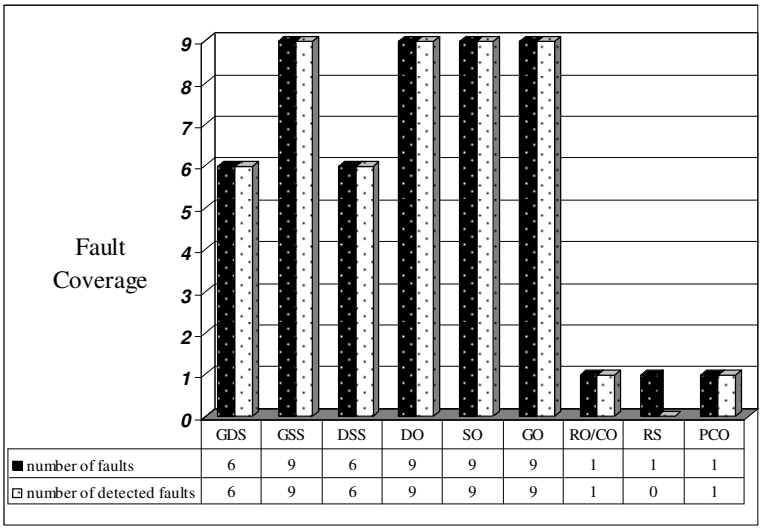


Figure 2.21 The layout pattern of the two-stage Op Amps with the BIST circuits.

For different physical design, window comparators must be carefully designed to match the acceptable band of the offset-based test, even for the same Op Amp. Thus, the ratio aspects of transistors summarized in Table 2.7 must be optimized in the physical design phase. The comparison range of the window comparator would also be changed according to the process variation, so the finally the comparison range is not exactly ±10% fluctuation of the fault-free response, but this change is slight due to the matched two inverter design and is still in the acceptable range.

As it also can be known from the previous introduced test flow and BIST circuits, controlled by *TM* and *TMC*, the designed BIST circuits generate a test signature signal $V_{p/f}$ to declare the Op Amp under test passed or failed the test. With reference to the

previously introduced fault models, total 50 catastrophic faults and a parametric fault for compensation capacitor have been injected for fault simulation. Figure 2.22 summarizes the fault simulation results that show 98% faults can be detected by the proposed BIST system. The undetected fault is the RS in compensation resistor.



	GDS	GSS	DSS	DO	SO	GO	RO/CO	RS	PCO
■ number of faults	6	9	6	9	9	9	1	1	1
⊡ number of detected faults	6	9	6	9	9	9	1	0	1

Figure 2.22 Faults simulation results.

The faults in transistors were mainly detected by the first offset-based test stage of the DC output checking, and the DC output voltage is much more sensitive to the faults in the transistors than the transient response test. For example, some faults in the current biasing circuit, which is composed of M0, M5 and M12 in Fig. 2.20, change the bias current and cause the open loop gain decrease of the Op Amp under test. This bias current change directly excites the output stage of the Op Amp to output significant voltage deviation, but cannot be reflected obviously in the transient response or is difficult to capture for the on-chip test circuit. Thus, the DC test can achieve high fault coverage. However, this offset-based DC test is limited by the large input offset design because the DC output voltage might be derived to the power supply sides. Even though this kind of large offset design is acceptable in some cases, the large offset design should be eliminated to make the transistors work in saturation region.

The current-based test was designed to assist the offset-based test in order to test the short RO/CO and capacitance variation PCO in the compensation circuit. Additionally, some faults in the second stage of the Op Amp could be detected by the

current-based test.

Table 2.9 shows the performance comparisons between the original Op Amp and the Op Amp with BIST circuits, which does not cause significant performance degradation.

Table 2.9 Performance parameters of the original Op Amp and the Op Amp with BIST circuits.

	Simulated Values	
Performances	***Original Op Amp***	***Op Amp with BIST***
Offset Voltage	180 μV	180 μV
DC Gain	71.165 dB	71.16 dB
Unity Gain Bandwidth	28.603 MHz	28.41 MHz
Phase Margin	67.366 Degree	65.898 Degree
Slew Rate	+2.83/-5.42 (V/μS)	+2.79/-5.34 (V/μS)
|Power Supply Rejection Ratio+/-|	93.741 dB /97.592 dB	93.631 dB /97.337 dB

2.3.4. Conclusion

In order to increase the fault coverage of Op Amp test, this paper has proposed a BIST scheme which combines offset-based test and current-based test together to test the catastrophic faults and the parametric fault in the compensation circuit. Using Rohm CMOS 0.18-μm technology, the5-bit counter based on-chip testing circuit was implemented with a two-stage Op Amp and the fault simulation has shown the proposed scheme could be an alternative and effective test approach for Op Amp with high fault coverage. The proposed BIST scheme can also be applied to test other amplifiers on the same chip with different window comparators. The disadvantages of this BIST scheme is large area overhead, but this situation would be improved in the multi-amplifier complicated circuits.

2.4. Conclusions and Discussions

In this chapter, two BIST techniques have been presented to test Op Amps. The first one is to configure the Op Amp into voltage follower, and to observe the SOV of the transient response. Only BIST circuit can test all the Op Amps in a same analog and mixed-signal system, and the proposed BIST circuit caused a little area overhead.

However, as it can be found from the fault simulation results of the three Op Amps, different Op Amp had different fault coverage, and the fault coverage is just about 90% when the cascode current mirror is used, so further improvements need be made.

The two-step BIST technique can achieve high fault coverage based on the combination of the offset-based and current-based test, but the 5-bit counter caused high area overhead.

Different test techniques have different advantages and disadvantages, so suitable test technique should be selected rightly based on the specific circuit configuration and the requirements for overhead, fault coverage and on-chip circuit complexity.

Chapter 3. A Resistance-Matching based BIST Technique for Current-Mode R-2R DAC

This chapter presents a resistance-matching based BIST technique for current-mode R-2R DAC. With the benefit of the extra DFT circuits, the R-2R network can be converted into two resistance-matching branches under the test mode, and the redistribution of the test current in the resistance-matching branches are transformed to two voltage drops at the input terminals of the Op Amp used in the DAC through the current-to-voltage converting circuit, and then the output of the Op Amp is observed to detect the possible defects in the R-2R network. Also, the DAC can be converted in a voltage follower, so the Op Amp can be tested by checking the SOV of the transient response. These two test modes are combined together to generate a final test result. The circuit-level simulation results of the BIST system for an 8-bit DAC are presented to demonstrate the feasibility of the proposed BIST technique with catastrophic fault coverage of 96% for R-2R network and 82.6% for the Op Amp, and approximately 6% area overhead. The parametric faults of resistance variation were also considered.

The rest of this chapter is organized as follows. Section 1 gives the overview on the existing test techniques for DAC. Section 2 presents the proposed resistance-matching based test strategy. Section 3 introduces the associated DFT circuits for the current-mode R-2R DAC. Section 4 subsequently gives the implements of the proposed BIST scheme for an 8-bit DAC. As for illustration, section 5 describes the fault models for DAC and shows the simulation results. Conclusion is finally presented in Section.6.

3.1. Introduction to DAC Testing

3.1.1. DAC Testing

For DAC, a large number of traditional test approaches can be found in [1,16,78-84], and the static parameters such as Integral Nonlinearity (INL), Differential Nonlinearity (DNL), offset, and gain error, and dynamic parameters such as Signal-to-Noise Ratio (SNR) and harmonic distortion, are usually measured to test DAC. Figure 3.1 shows the basic test setup, which is a combination of the static and dynamic

DAC test setups [79].

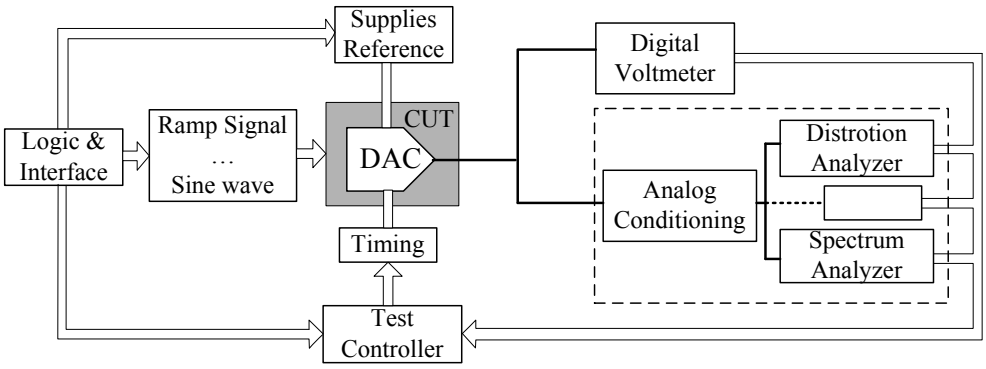


Figure 3.1 Basic setup for DAC testing.

Based on the power supplies and reference setting, when the test setup is used to measure the specifications of the DAC under test, different set of digital codes would be fed to the inputs, the ramp signal is commonly used for static specification measurement and sine wave is often for dynamic specification testing. In the static testing case, the output of the DAC is mainly sent to the digital voltmeter to calculate the static parameters. In the dynamic testing case, a number of instruments like distortion analyzer and spectrum analyzer are utilized to capture the analog performances (spectral parameters or dynamic specifications) after an analog conditioning block, typically a filter. Finally, the analyzing results are sent to the test controller or computer for the required processing. The test signals can be generated by different instruments, and the output analyzing can be replaced by different devices. Also the test controller can be a computer or Digital Signal Processor (DSP).

In addition to the DAC's performance parameters used in the above mentioned traditional functional test, some other electronic characteristics can be employed to test the DAC, like the power supply parameters [85].

3.1.2. BIST Techniques for DAC

Due to the high cost of the traditional off-chip test, BIST technique has recently attracted research activity as a prospective solution for analog and mixed-signal testing. It reduces the tester complexity, eliminates the need for off-chip interfacing, and allows the device to be tested many times during the manufacturing cycle of the product [15].

Also, in the system operation phase, the designed BIST circuits can still test these integrated devices at their idle time.

A variety of BIST schemes have been proposed for DAC. In [86,87], the characteristics, i.e., DNL and INL, of the converters were measured to determine whether the DAC passed or failed the test by on-chip BIST circuitry, but the extra response-processing circuitry for response analysis and complex on-chip stimulus generator would cause large silicon area overhead.

In [88], the DAC was tested by a Digital Signal Processing-based BIST control unit as consecutive digital codes converting the full operating range with 2^N codes for N-bit DAC. The output response of DAC was sampled and converted by a sigma-delta ADC to digital code. Then, according to the least-square fitting algorithm, the characteristics of the DAC is be obtained by calculating the four coefficients from an accumulation of the digitalized responses. The utilization of sigma-delta modulator can decrease the hardware cost to a certain extent, but the generation of ramp signals still caused a high test cost, particular for the high resolution DAC.

The polynomial BIST technique [89] derives the coefficients of the third-order polynomial which best fits the transfer function of the DAC/ADC. Then, sinusoidal stimulus is applied to the CUT, the offset, gain and harmonic distortion that would be computed out. This solution can be applied to flash converters, delta-sigma converters, and analog circuit between the DAC and ADC. However, on-chip accurate analog sinusoidal stimulus and DSP are needed.

In [90], a BIST solution is proposed to test a specific speech CODEC's, but it requires both ADC and DAC on the same chip.

To eliminate the requirement for high precision instruments to measure the performance parameters, such as DNL, INL, offset error, gain error, S.J. Chang [91] proposed a BIST scheme for DAC by converting the DAC output voltages corresponding to the different input codes into different oscillation frequencies through the Voltage Controlled Oscillator (VCO), and further transferring these frequencies to different digital codes using a counter. The on-chip pattern counter, memory to store output codes and DSP would cause high area overhead.

All the above-mentioned specification-based BIST approaches results in high-test costs and does not ensure detection of all defects, causing potential reliability problems

[35]. Thus, several fault-based BIST schemes have been proposed for DAC, as an alternative testing method, targeted here for the detection of manufacturing defects. In [92], a fault-based testing strategy was investigated by observing the power supply current in the digital section of the DAC under test, and the voltage and bias current in the analog section. Additionally, the presented fault-based BIST scheme in work [93] employs a pattern counter to continuously generate stimulus patterns feeding to the DAC under test, and a comparator to compare the output of the DAC under test with gold reference generated by an adaptive ramp generator. With resolution increase, the output binary combination of pattern counter will increase exponentially. Thus, the resistance-matching based BIST is proposed to test the current-mode R-2R DAC.

In most BIST applications, stimulus generators like sine wave generator [94] and ramp generator [95], are commonly employed to excite the faulty CUT to output different outputs from the fault-free circuits, but analog generator cannot create different stimulus like the digital test pattern generator. Different analog generators are needed for different analog circuits under test, even for a single circuit in order to high fault coverage, so this complex test stimulus generation has greatly limited the analog BIST application and caused high test cost including silicon area and test time. The designed stimulus generator should also been tested to make sure they can created expected analog test signals. Thus, with the resistance-matching based BIST implementation in the current-mode R-2R ladder DAC, a fully testable DAC is presented as the new analog stimulus generation strategies for analog BIST in this chapter, because it can generate various analog signals for different analog circuits by controlling the digital inputs. Also, it can be used as a single digital-to-analog converting system, and the proposed BIST scheme can be utilized in the whole cycle of the DAC.

3.2. Resistance-Matching Based Test Strategy

Each of these DAC architectures has a unique set of strengths and weaknesses, and each architecture's weaknesses determine its likely failure mechanisms, and these in turn drive the testing methodology [16]. For R-2R ladder DAC, the accuracy of the converter is determined by the matching of the R-2R resistors and of the current source transistors [96], and the main mismatch caused by the tolerance of the resistors, the effect of R_{ON} of the nonideal behavior of the switches [97]. Considering the thin film

unit resistors used in matching-critical applications, the major contributions are the sheet resistance variations, contact resistance variations, contact size variations, effective length variations of the resistors and edge variations [98]. Some calibration/trimming strategies have been present to improve the match of the R-2R ladder in [99,100]. Testing offset, integral linearity, differential linearity, and gain errors can verify the functionality of DAC. These errors are due to the mismatch of the components [86]. For this reason, the possible mismatch characteristic can be employed to test the R-2R ladder DAC.

Figure 3.2 shows the *N*-bit current-mode R-2R network, which is constituted by the *2R* vertical resistors and the related equivalent resistors $R_{ri(i=0,\ 1,\ \ldots,\ N-1)}$ looking toward the right-hand end of the ladder. The vertical resistance including the R_i and the R_{ON} of the switch S_i should be equal to the resistance of R_{ri}, so the binary-weighted R-2R network can be constituted. The two branches with same equivalent resistance are called resistance-matching branches in this dissertation. The binary input $d_{(N-1)}$~d_0 controlling the switches $S_{(N-1)}$~S_0 are converted to an equivalent analog signal by the binary-weighted resistor ladder.

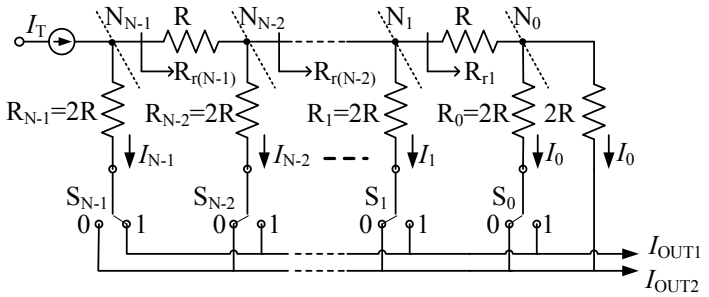


Figure 3.2 The R-2R ladder network.

Through the resistance-matching branches, a test current I_t, which is fed to the node $N_{(N-1)}$ shown in Fig 3.2, is reduced by a weighting factor of 2 from the leftmost vertical *2R* to the rightmost vertical *2R*. The distributed currents $I_{(N-1,N-2,\ldots 0)}$ in the vertical resistors $R_{(N-1)}$~R_0 can be written as

$$I_{N-1}=I_t/2^1, I_{N-2}=I_t/2^2, \cdots, I_1=I_t/2^{N-1}, I_0=I_t/2^N \tag{3.1}$$

If d_i is logic high, the current I_i through R_i flows into I_{OUT1}, otherwise it flows into I_{OUT2}. Therefore, the currents flowing into I_{OUT1} and I_{OUT2} should be equal to each other when the input binary pattern is set as "10···0". Consequently, once a physical defect happened, the resistance mismatch of the resistance-matched branches causes unequal reduction of the test current I_t to I_{OUT1} and I_{OUT2}, so the redistributed currents flowing into I_{OUT1} and I_{OUT2} can be monitored to detect the possible defects in the R-2R network by setting the input binary pattern to "10···0".

In order to intuitively explain the resistance-matching based test strategy, the important part of Op Amp in the DAC is not shown in Fig. 3.2, but the test of the Op Amp cannot be ignore, and it can be tested by measuring the performance parameters [75] like slew rate, setting time, and phase margin from the transient response, but these parameters measuring test requires high accurate output response analyzer, that would increase the test cost, so the SOV checking of the transient response is applied by converting the R-2R DAC into a voltage follower, that will be described in detail in following section.

3.3. The Current-Mode R-2R DAC with DFT Circuits

Figure 3.3 shows the circuit configuration of an 8-bit current- mode DAC and its DFT circuits including from *DFT_1* to *DFT_4*, which were designed to implement the resistance-matching based test strategy. I_T is the test currents to excite the defects in the R-2R network of the DAC under test, V_T is a test voltage reference, and d_7~d_0 are input binary signals that are converted into an equivalent analog voltage according to the reference voltages of V_{REF+} and V_{REF-}.

Compared with the general R-2R network shown in Fig. 3.2, the horizontal *R* resistors were replaced by a parallel combination of two *2R* resistors, which were separately connected to an analog switch. On one hand, the parallel combination design can improve the resistance match of the R-2R network by injecting the same analog switches S_7~S_0 in the vertical branches. On the other hand, as mentioned resistance-matching branches reconfiguration of the R-2R network, the injected analog switches S_{t7}~S_{t0}, can further divide the network into 8 pairs of resistance-matching branches from the Most Significant Bit (MSB) branch to Least Significant Bit (LSB) of the R-2R network.

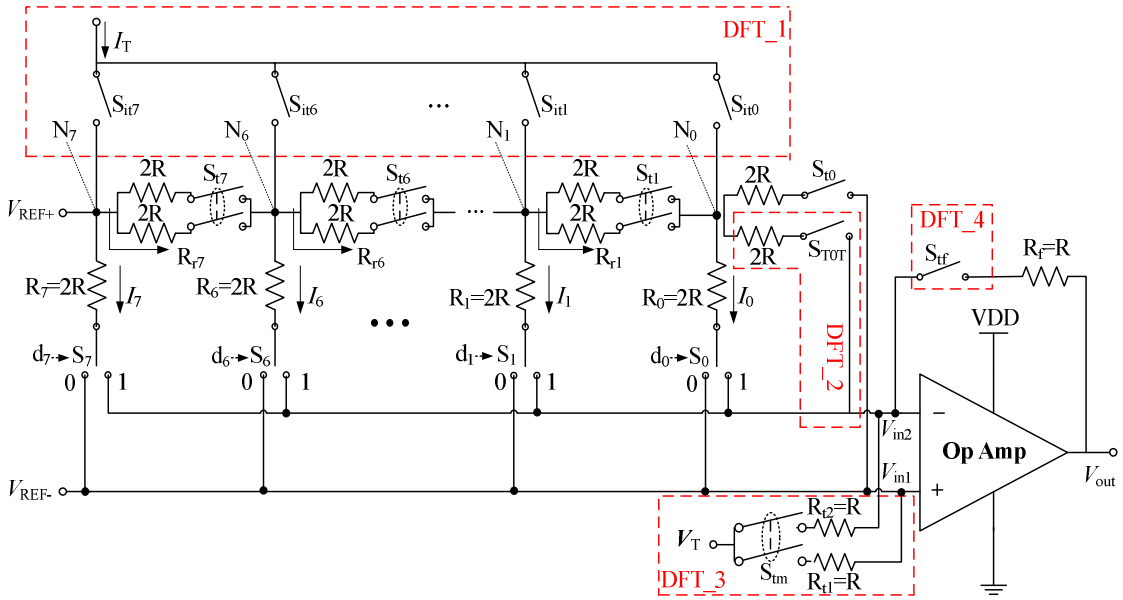


Figure 3.3 The circuit configuration of the current-mode R-2R DAC with *DFT*s.

When all the switches of S_{t7}~S_{t0} are close, test current I_T flows into node N_7 by closing switch S_{it7}, and is reduced equally in the resistance-matching branches of R_7 and R_{r7}. When switch S_{t7} is open, the resistor network is divided into two parts, the left and right parts of node N_6. Then, close switch S_{it6}, the test current $I_{T,}$ flows into the right part of node N_6, and is equally distributed in the new resistance-matching branches of R_6 and R_{r6}. Similarly, if the switches of S_{ti} is open, I_T should flow into the new branches of R_i and R_{ri} through node $N_{(i-1)}$ by closing switch $S_{it(i-1)}$. The possible defects happened in the right-hand of the R-2R network would cause larger resistance mismatch in the lower resistance-matching branches, and that enlarges the current difference between the two matched branches. For example, the defects happened in R_0 cause higher resistance mismatch in branches of R_0 and R_{r0} than that in $R_1$and R_{r1}. Therefore, defect sensitivity of resistance mismatch caused by the possible defects can be improved by the cutting of the added analog switches $S_{ti(i=7,6,...or\ 1)}$, and the defects can be more easily detected in related lower resistance-matching branches. *DFT_1* was design to pass the test current I_T to test node $N_{(i-1)}$ based on the cutting of switch S_{ti}.

When the resistor network was cutting by the switch S_{ti}, the left part of node $N_{(i-1)}$ lost its function, so the binary inputs d_7~d_i are not considered in this case, and the binary input "$d_{(i-1)}$~d_0" is set to "10~0" to force the test current equally flowing into V_{in1} and

V_{in2}. However, the switch S_i, shown in Fig. 3.4, consists of two transmission gates (TGs): *TG0* and *TG1*. When d_i is logic high, resistor R_i is connected to V_{in1} through *TG1*, and so the possible faults in *TG0* would not be detected in this case, since *TG0* is turned off. For this reason digital input d_i must be changed to logic '0' to excite the possible defects in *TG0* by switching the input binary pattern "$d_i d_{(i+1)}$~d_7" to "01~1". As a result, the currents flowing into V_{in1} and V_{in2} become unequal, because the current, flowing through switch S_{t0}, can only follow into V_{in1}. Therefore, as a parallel branch of the *2R* resistor connected to S_{t0}, *DFT_2* was designed to provide a current path to V_{in2} from node N_0 by switching S_{t0} and S_{t0t}, and then the test current can be reduced equally to V_{in1} and V_{in2} when d_0 is set to logic '1'. Consequently, the currents, flowing into V_{in1} and V_{in2}, are observed to test the R-2R network.

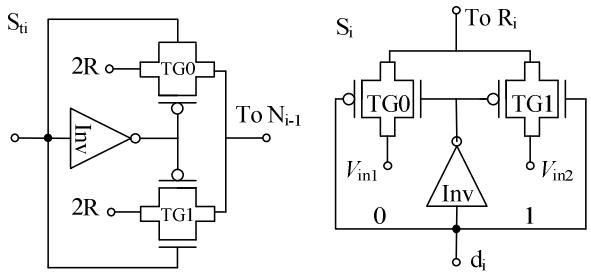


Figure 3.4 The circuit configuration of the switches S_{ti} and S_i.

Whereas, the currents cannot be directly monitored according to the circuit configuration of the R-2R DAC shown in Fig. 3.3, so the currents are firstly transformed to voltages in this work, and then the voltage are observed to determine the R-2R network past or failed the test. By closing S_{tm} and opening S_{tf}, the DAC under test can be converted into the R-2R network test mode shown in Fig. 3.5 for each test node N_i. R_{bi} and R_{ri} represents the two equivalent resistances of the two resistance-matching branches, R_{bi} is the equivalent resistance of the vertical branch including resistor R_i and the R_{ON} of the switch S_i. The test current I_T follows through R_{bi} and R_{ri}, and creates two voltage drops on the test resistors R_{t1} and R_{t2} according to the test reference V_T. Finally, the Op Amp creates an output to send the output analyzer according to the two voltage drops at V_{in1} and V_{in2}.

Also, the proposed R-2R DAC can be configured as a voltage follower by opening switches S_{it7}~S_{it0}, S_{tm} and S_{t0t}, closing S_{tf} and S_{t7}, and setting binary input pattern to

"0~0". The possible defects in the Op Amp can be detected by checking the SOV of the transient response shown in Fig. 3.6. *R*' represents the equivalent resistance of the R-2R network under the op amp test mode.

The two test modes of R-2R network test mode and Op Amp test mode can be realized by the controlling the switches summarized in Table 3.1.

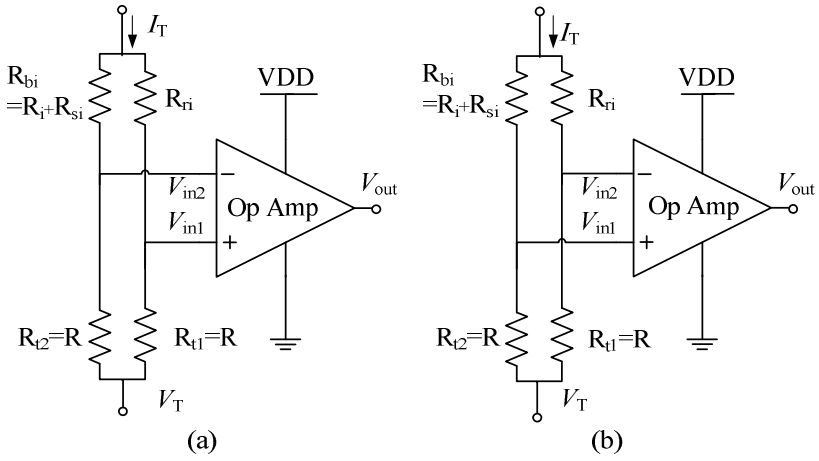


Figure 3.5 Two test types of R-2R network test mode: (a) Test configuration when the binary input is set as "10···0". (b) Test configuration when the binary input is set as "01···1".

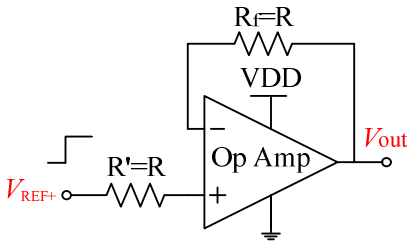


Figure 3.6 Test configuration for Op Amp used in the DAC under test.

Table 3.1 Switch settings under different test modes.

Test mode	S_{tm}/S_{tf}	$S_{IT7}\sim S_{IT0}$ / $S_{t7}\sim S_{t1}$	$d_7\sim d_0$	S_{t0}/S_{T0T}
R-2R network test mode	S_{tm}='1' S_{tf}='0'	$S_{itj(j=7,6..0)}$='1', $S_{itk(k\neq j)}$='0' $S_{t(j+1)}$='0', $S_{tk(k\neq(j+1))}$='1'	d_j='1', $d_{k(k\neq j)}$='0' d_j='0', $d_{k(k\neq j)}$='1'	$S_{t0}=\overline{d_0}$ $S_{T0T}=d_0$
Op Amp test mode	S_{tm}='1' S_{tf}='0'	$S_{it7}\sim S_{it0}$="0∼0", $S_{t7}\sim S_{t1}$="1∼1"	$d_7\sim d_0$="0∼0"	S_{t0}='0' S_{T0T}='1'

3.4. Test System Implementation

3.4.1. The Proposed BIST System

Figure 3.7 depicts the system architecture of the proposed test technique for the R-2R DAC. The stimulus generators, the output analyzer including a window comparator and a SOV checker proposed in Sect. 2.1, and the control logic were designed to implement the proposed BIST system and the test procedure. Finally, the first stage test signatures $V_{p/fn}$ and $V_{p/fo}$ are combined to generate a final signature.

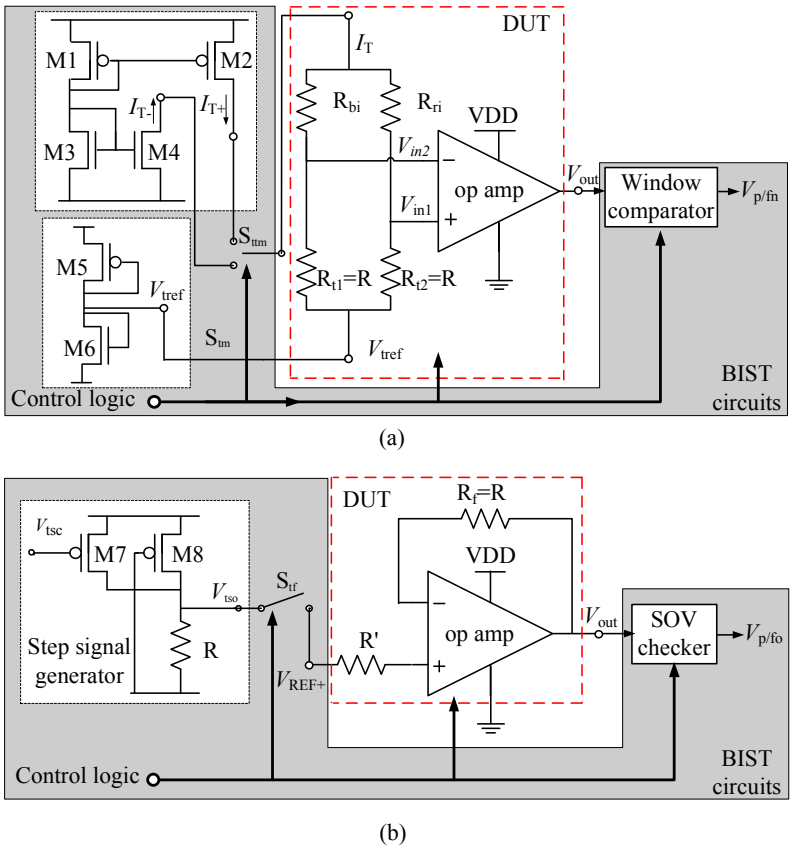


Figure 3.7 Block diagram of the BIST system for: (a) R-2R network test mode. (b)Op Amp test mode.

Figure 3.7(a) shows the R-2R network test mode, the DAC under test was converted into the test structure of resistance-matching branches shown in Fig. 3.5. The test current is generated by the complementary test currents generator. It comprises transistors from M1 to M4, generates test currents I_{T+} and I_{T-} to excite the possible defects in the analog switches of S_{t7}～S_{t0}, because the positive/negative test current just

follows through one transistor of the *TG* in some cases, and the defects existing in another transistor might not be detected by a single positive/negative test current. Note that the complementary test currents are alternately passed to I_T by switching S_{ttm}. The voltage reference V_T is approximately 0.9V and created by the voltage divider of M7 and M8. It constrains the voltage drops at $V_{in1}$and V_{in2} within the Input Common-Mode Range (ICMR) of the Op Amp used in the DAC under test. In this case, the Op Amp works as a comparator to recognize the voltage difference between V_{in1} and V_{in2}, and generate a binary signature signal $V_{p/fn}$.

Figure 3.7(b) shows the Op Amp test mode, the DAC under test was converted into a voltage follower. The step signal, generated by the step signal generator, is composed of a resistor *R* and two parallel pMOS transistors of M7 and M8. The digital input signal V_{tsc} controls the V_{tso} to output two different voltages to V_{REF+}, and then the SOV checker observes V_{out} and generates a fault signature $V_{p/fo}$.

Note that the test currents and voltages might vary with the process or temperature variation, but this varied currents and voltages do not change their original function to excite the possible defects in the DUT.

3.4.2. Output Response Analyzer

The voltage drops at V_{in1} and V_{in2} could not be exactly equal owning to the process variation, so the output V_{out} is not constant but swings within a range under the test mode. The Monte Carlo simulation was applied to define the V_{out} swing ranges based on the resistance variation with a maximum fluctuation of 0.1% and transistor size variation with a maximum fluctuation of 1% in the DAC under test. The swing ranges are called fault-free ranges in this work. Note that the ranges would change in different designs, so the thresholds of the WC should be carefully designed to follow fault-free ranges. *WC0*-*WC2* shown in Fig. 3.8(a), were design to check the three fault-free ranges under different test modes.

Throughout the test procedure, V_{out} is firstly send to the three *WCs* and each *WC* generates a checking result depending on their thresholds. Then, the outputs of these *WCs* are sent to the second checking stage. Under the R-2R network test mode, the valid output of *WC0* is passed to *XOR1* through *NAND_R* by setting *TM_R* to logic high. Conversely, the invalid outputs of *WC1* and *WC3* could not be sent to *XOR1* through *NAND_O* by setting *TM_O* to logic low. Under the Op Amp test mode, the outputs of

WC1 and *WC2* become valid and are passed to *NAND1* and *NAND0*, respectively. The control signal V_{tsc} of the step signal generator, should also be sent to *NAND1* or *NAND0* and to enable the valid output to pass to *NAND_O*. After this, the output of *XOR0* is sent to *XOR1* through *NAND_O* by setting *TM_R to* logic low and *TM_O* to logic high. Finally, the window comparator used in R-2R network test mode and the SOV used in op amp test mode are combined in the output response analyzer to form a final test signature $V_{p/f}$.

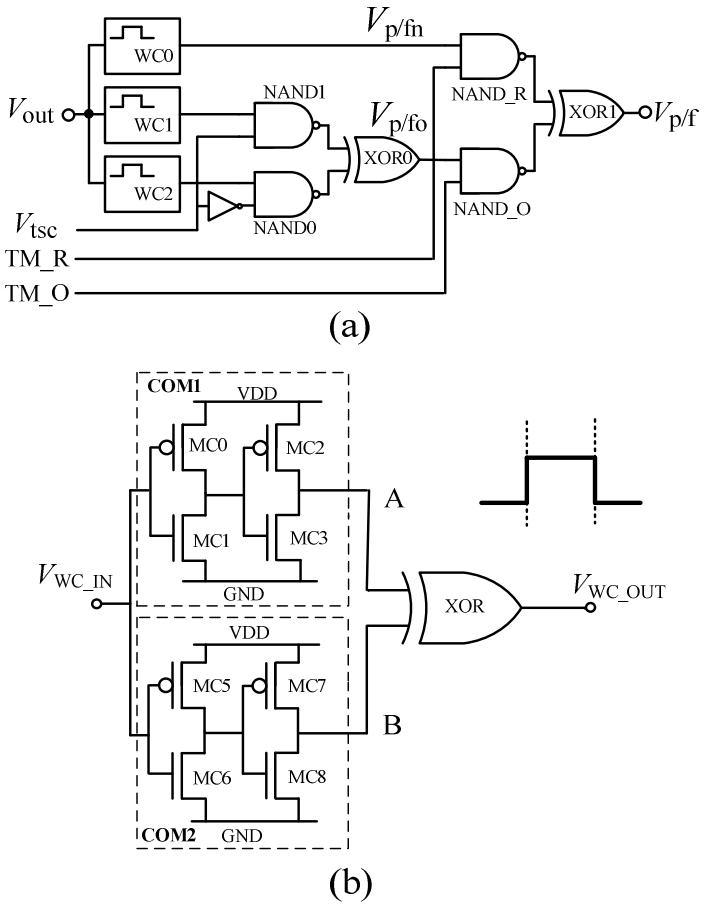


Figure 3.8 Output response analyzer: (a) The block diagram of the output response analyzer. (b) Circuit configuration of the window comparator.

As it can be seen from Fig 3.8(b), the window comparator consists of two comparators *COM1* and *COM2*, and a *XOR* gate. On one hand, *COM1* compares $V_{WC\text{-}IN}$ with its threshold voltage and creates a logic high voltage to the terminal *A* if $V_{WC\text{-}IN}$ is

greater, otherwise a logic low voltage. Similarly, *COM2* has same function as *COM1*. Then the outputs A and B are connected to the *XOR* to generate a final result $V_{WC\text{-}OUT}$.

3.4.3. Control Logic

The control logic is an entirely digital block, which controls the whole test procedure. It converts the DAC under test into different test modes in accordance with the settings of the analog switches seen in Table 3.1, connects DUT to the BIST circuits and controls the BIST circuits. A possible design of the control logic is shown in Fig. 3.9.

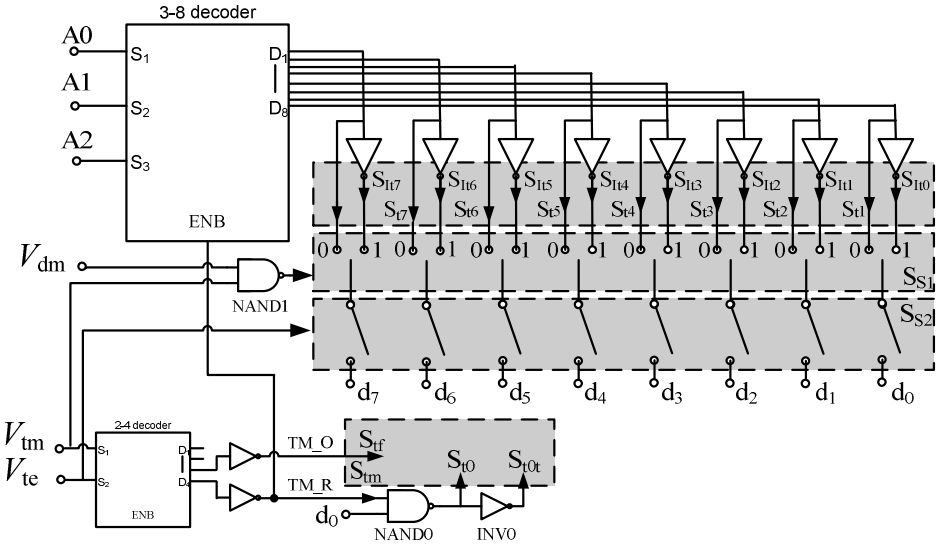


Figure 3.9 The internal test logic controller.

V_{te} starts the test by connecting the output Vout to the output response analyzer, and then V_{tm} converts the DAC into different test modes by generating two controlling signals of *TM_R* (R-2R network test mode) and *TM_O* (op amp test mode).

When V_{tm} goes logic low, *TM_O* goes to high and converts the DAC into a voltage follower by turning on the feedback switch S_{tf} and connecting the V_{tso} to V_{ref+}, and *TM_R* goes to low, the 3-8 decoder turns S_{t7}~S_{t1} on, turns S_{it7}~S_{it0} off, and sets "d_7~d_0" to "0~0". Also, S_{T0T} and S_{t0} are controlled by d_0 and *TM_R* to force all the current follow into V_{in1}. The step signal is fed to the DUT by switching V_{tsc}.

When V_{tm} goes to logic high, *TM_R* and *TM_O* convert the DAC into R-2R network test mode by switching S_{tm} and S_{tf}. *TM_R* goes to high and enables the 3-8

decoder. According to the binary input pattern "*N2~N0*", the 3-8 decoder sets one of its outputs to logic low to pass the test current to the related test node, to create the pair of the resistance-matching branches by switching S_{t7}~$S_{t1}$and S_{it7}~S_{it0}, and to set the input pattern "d_7~d_0". V_{dm} was designed to change reconfiguration type (shown in Fig. 3.5) of the R-2R test mode by switching the binary input pattern through the switches in S_{S1} shown in Fig. 3.9. Additionally, V_{ttm} was designed to pick the test complementary current through S_{ttm} in Fig. 3.7(a).

Note that, V_{te}, V_{tm}, *N2~N0,* $V_{tsc,}$ V_{ttm} and V_{dm} are generated to control the whole test procedure by the high level test bus. The timing diagram (test vectors) of these signals is shown in Fig. 3.10.

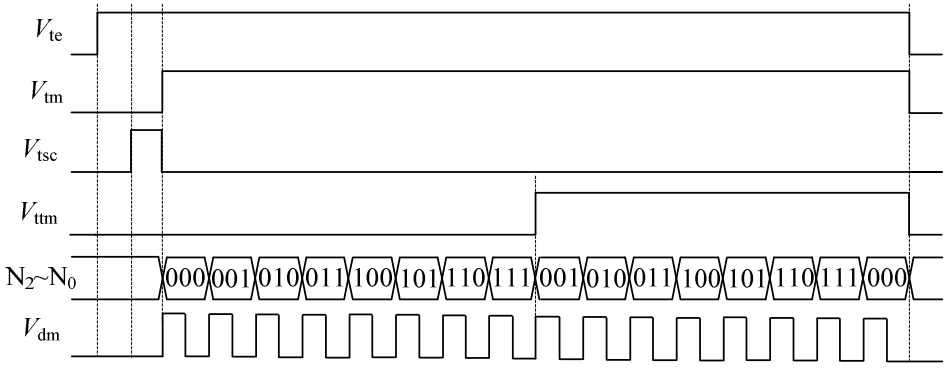


Figure 3.10 The controlling logic of the high level test bus.

3.5. Simulation Results

3.5.1. Fault Modeling for R-2R DAC

Two classes of device-level faults were considered: catastrophic faults, including shorts and opens in MOS transistors, resistors and capacitors, and parametric faults of resistance variation of the resistor used in the R-2R network. Additionally, the possible defects in inverters used in the analog switches shown in Fig. 3.4, were modeled as gate-level Stuck-At (SAT) fault models.

3.5.2. The Simulation Results and Discussion of the 8-bit R-2R DAC

An 8-bit R-2R DAC has been designed as an example to evaluate the proposed test technique, using Rohm 0.18-μm CMOS technology. The circuit was simulated using

HSpice. The resistance of the unit R and the aspect ratios of transistors in the R-2R network shown in Fig. 3.3 were set to 100kΩ and 0.54/0.18 μm (W/L), respectively. Particularly, the aspect ratios of the transistors used in S_{tf} in *DFT_4* were set to 1.2/0.18 μm (W/L) to optimize the performance of the DAC. The switch S_{tf} must be injected into the left side of the feedback resistor R_f to eliminate the R_{ON} variation caused by the varying V_{out}. The Op Amp used in the DAC under test is shown in Fig. 3.11, and the element sizes are summarized in Table 3.2.

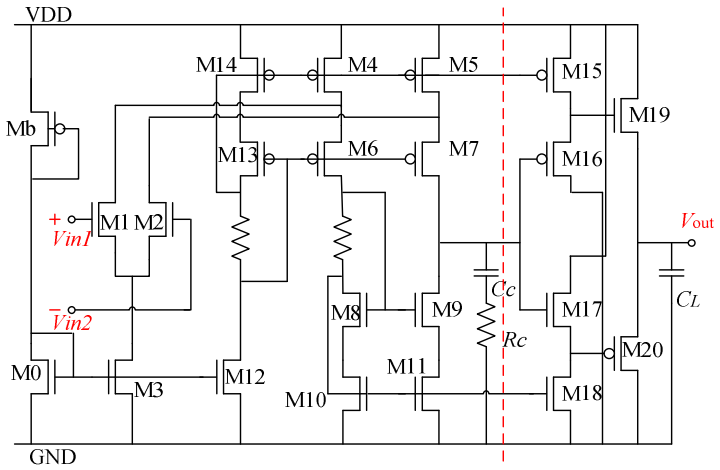


Figure 3.11 The circuit configuration of a buffered Op Amp.

Table 3.2 Summary of the elements parameters of the buffered Op Amp.

Element	***Parameters***	***Element***	***Parameters***
M0~M7, M13, M14	40/0.4 μm (W/L)	Mb	1.6/0.4 μm (W/L)
M8~M11	32/0.4 μm (W/L)	M12	50/0.4 μm (W/L)
M15	10/0.4 μm (W/L)	M16	16/0.4 μm (W/L)
M17, M19	24/0.4 μm (W/L)	M18	12.8/0.4 μm (W/L)
M20	18/0.4 μm (W/L)	R1, R2	6.6 kΩ
C_C	2 pF	C_L	10 pF
R_C	10 kΩ	--	--

The element parameters of the stimulus generator are summarized in Table 3.3. If V_{tsc} is logic high, the output V_{tso} is approximately 0.606V, otherwise 1.202V. The complementary test current generator creates a source current I_{T+} of approximately

8.9μA and a sink current I_{T-} of approximately -8.9μA, and the test reference voltage V_T is approximately 0.9V. In addition, the W/L ratios of the transistors used in the output response analyzer and the thresholds of each window comparator (*WC0*～*WC2*) are listed in Table 3.4.

Table 3.3 Summary of the elements parameters of the stimuli generators.

Sub-circuits	***Element***	***Parameter***
Complementary test current generator	M1, M2	2.8/0.4 μm (W/L)
	M3, M4	0.54/0.4 μm (W/L)
Voltage divider	M5	2.8/0.4 μm (W/L)
	M6	0.54/0.4 μm (W/L)
Step signal generator	M7	3.4/0.4 μm (W/L)
	M8	2/0.4 μm (W/L)
	R	3.35 kΩ

Table 3.4 Summary of Elements Parameters in the output response analyzer and the thresholds of the three *WCs*.

	Elements	***W/L (μm)***	***Threshold (V)***
Transistor in *WC0*	MC0,MC2	48/0.18	V_L= 0.537 V_H= 1.219
	MC1,MC3	0.5/0.18	
	MC5,MC7	1.2/0.18	
	MC6,MC8	11.6/0.18	
Transistor in *WC1*	MC0,MC2	0.46/0.18	V_L= 0.57 V_H= 0.622
	MC1,MC3	4.5/0.18	
	MC5,MC7	0.46/0.18	
	MC6,MC8	2.2/0.18	
Transistor in *WC2*	MC0,MC2	28.8/0.4	V_L= 1.167 V_H= 1.216
	MC1,MC3	0.6/0.4	
	MC5,MC7	33/0.4	
	MC6,MC8	0.6/0.8	
--	others	0.54/0.18	--

With reference to the mentioned fault models, the fault simulation was executed in circuit level. Figure 3.12 shows that the designed BIST system can detect 384 faults of

the total possible 400 catastrophic faults in the R-2R network, resulting in the fault coverage of 96%. The undetected faults are the pMOS GO*s* in S_{t7}~S_{t0} and S_{T0T}, because the pMOS GO on these switches cause a little resistance change due to the parallel design. However, the pMOS GO in the vertical analog switches S_7~S_0 can be detected, because the two *TGs* in S_i conduct alternately.

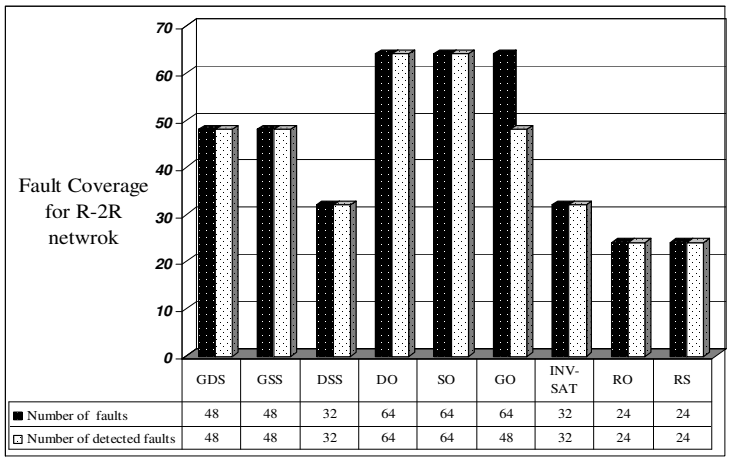
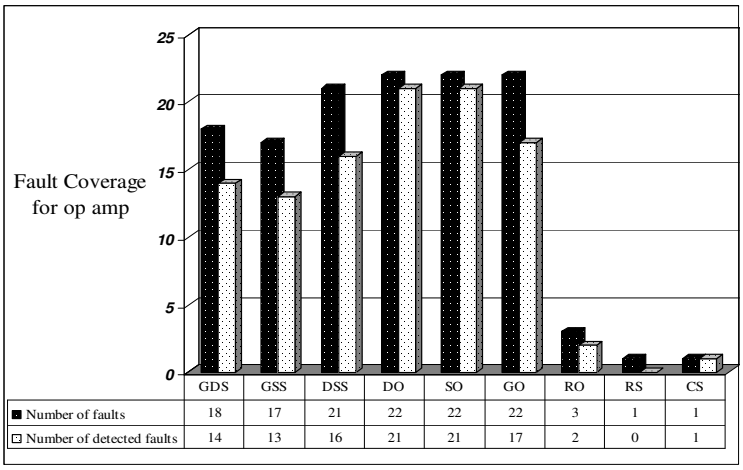


Figure 3.12 Fault simulation results under R-2R network test mode.

The fault simulation results under the Op Amp test mode are shown in Fig. 3.13, 127 catastrophic faults were injected into the Op Amp, and 105 faults were finally detected with the fault coverage of approximately 82.6%. The main hard-detected faults exist in the cascade current mirrors, since the current mirrors can still provide an almost constant current even some faults happened. Also, the faults *RO* and *RS* in the compensation circuit are hard-detected using the stable output checking of the transient response because the faults happened in the compensation circuit mainly change the frequency domain parameters of the op amp. Additionally, the parametric faults of the resistance variation were also considered, more than 2kΩ variation of each 100kΩ resistors in the R-2R network could be detected.

Figure 3.14 shows the physical layout of the 8-bit R-2R DUT with the DFT circuits and the proposed BIST circuits, which caused approximately 6% area overhead of the original DAC under test. Note that the area overhead depends on the DUT and the physical layout patterns, the area overhead ratio can decrease with the resolution increase of the DAC under test. Five layout patterns were designed to verify the

proposed BIST technique, one is a basic DAC with the BIST circuits and the others are faulty DACs with the BIST circuits by injecting some failures.



	GDS	GSS	DSS	DO	SO	GO	RO	RS	CS
Number of faults	18	17	21	22	22	22	3	1	1
Number of detected faults	14	13	16	21	21	17	2	0	1

Figure 3.13 Fault simulation results under Op Amp test mode.

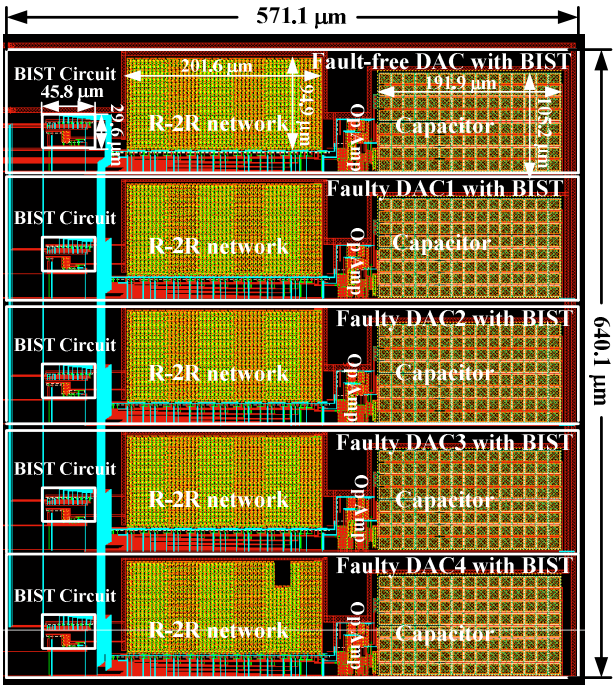


Figure 3.14 Layout patterns of the DUT with the BIST circuits.

To research the effect of the DFT circuits and the BIST circuits to the R-2R DAC, three R-2R DACs were simulated. The first DAC is the general R-2R DAC, and composed of the general R-2R network shown in Fig. 3.2 and the Op Amp shown in Fig.

3.11. The second DAC is the analog switches injected/calibrated R-2R DAC, formed by removing the DFT circuits of *DFT_1~DFT_3* and closing S_7~S_0 and S_{tf} in the circuit shown in Fig. 3.3. The third DAC is the proposed self-testable R-2R DAC in this work. Their INL and DNL characteristics are shown in Fig. 3.15. As it can be seen from the INL and DNL curves of the first and the second R-2R DAC, the maximum |INL| decreased from 1.078 LSB to 0.232 LSB, and the maximum |DNL| decreased from 0.334 LSB to 0.206 LSB, so the injected analog switches in the horizontal branches improved the resistance-matching of the R-2R network and also the testability of the R-2R DAC. Comparing the INL and DNL curves for the second and third R-2R DAC, the INL and DNL characteristics are almost the same, so the inclusion of the BIST circuits does not degrade the INL and DNL characteristics.

An 8-bit current mode R-2R DAC was mainly considered for the proposed resistance-matching based BIST technique, also it can be applied to the *N*-bit R-2R DAC with several modifications. Firstly, in the main body of the DAC shown in Fig.2, the number of the analog switches in *DFT_1* needs be changed to *N* in accordance with the *N*-bit R-2R network, so the test current can be passed to each test node. Then a new *i-N* decoder should be substituted for the 3-8 decoder to setting switches of $S_{it(N-1)}$~S_{it0}, $S_{t(N-1)}$~S_{t1} and digital inputs $d_{(N-1)}$~d_0. Finally, the high level test vector of N_2~N_0 shown in Fig 3.9 should be changed to N_i~N_0, which controls the new *i-N* decoder. Accordingly, compared with the test time of $(4\times8+2)\times T_{clk}$ (T_{clk} is the test clock period) for the 8-bit DAC, $(4N+2)\times T_{clk}$ are need to test the *N*-bit R-2R DAC using the proposed resistance-matching technique. The fault coverage should be almost the same as that in the 8-bit case, because the ratio of undetected faults to the total possible faults does not vary.

Table 3.5 compares the proposed BIST technique with those existing BIST techniques. Most existing techniques employed ramp signals as testing stimulus, and need 2^N digital input codes. The cost test time is $2^N \bullet T_{clk}$, and it would increase exponentially according to the resolution increasing of the DUT. However, the proposed BIST technique in this work needs only $(4N+2) \bullet T_{clk}$ for an N-bit R-2R DAC. In addition to the 10 catastrophic fault models in Sect.1.3, the parametric fault model of resistance variation was also considered. Total 92.8% catastrophic faults and more than 2kΩ resistance variation in each unit resistor 2R were detected. Also, complex and

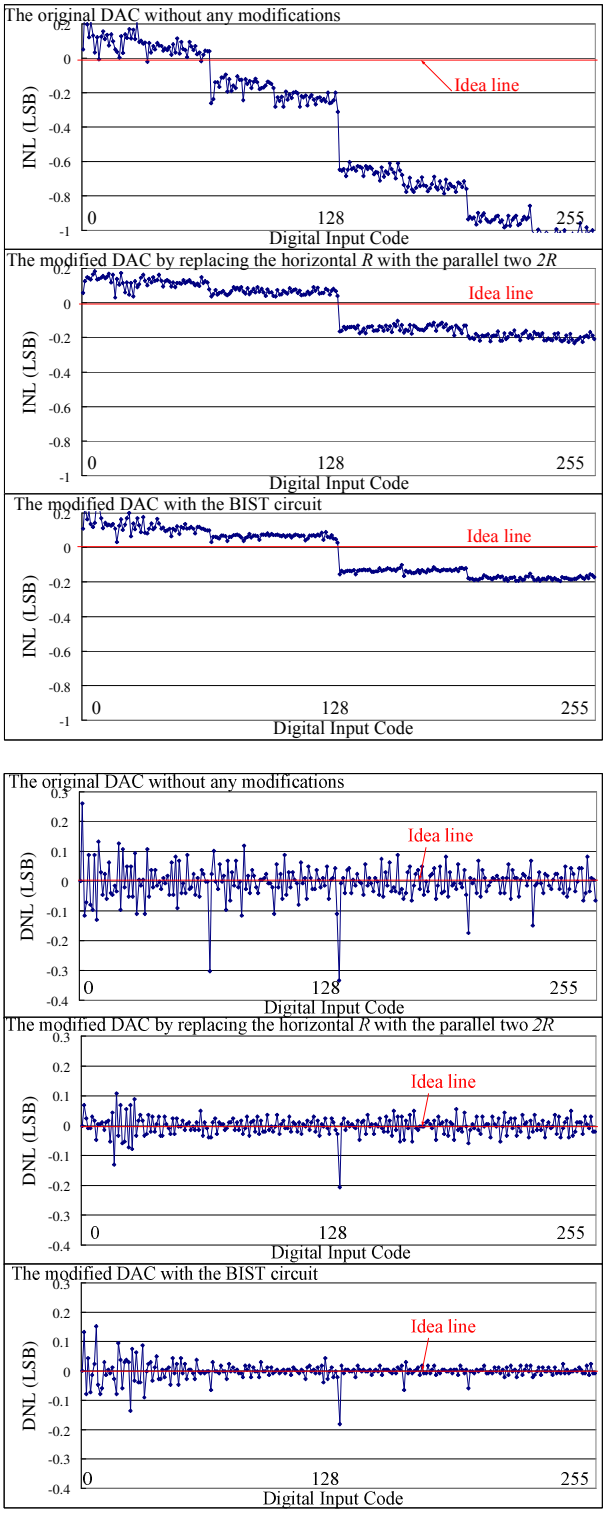


Figure 3.15 INL and DNL comparisons of the general R-2R DAC, analog switches injected/calibrated R-2R DAC and the proposed R-2R DAC with the BIST circuits.

accurate test signals are not necessary, so the cost of stimuli generators design was reduced to offer a low area cost. Additionally, the parallel design of the mentioned in Sect. 3.3 increased the resistance matching of the resistance-matching branches. In summary, the proposed BIST technique presents a good compromise between test time, area overhead and fault coverage.

Table 3.5 Comparisons of the BIST technique in this work with other related BIST.

Features	***Test strategy***	***BIST circuits***	***Test Time***	***Technology***	***Area overhead***	***Fault Coverage***
[86]	Static testing	*N*-bit counter, sample-and-hold and error amplifier	2^N digital input codes	1.2μm	6%	N/A
[88]	INL calculating	Digital ramp generator Sigma-delta modulator	2^N digital input codes	N/A	N/A	N/A
[92]	Parametric test	Built-in current sensors and voltage sensors	N/A	N/A	N/A	96.9% for three faults of short
[93]	Performance measuring	Pattern counter, adaptive ramp generator, Comparator, etc.	2^N digital input codes	0.18μm 2.5V	N/A	96.73%: catastrophic faults
This work	Resistance-matching based testing	Shown from Fig. 3.6 to Fig. 3.8	$(4N+2)\bullet T_{clk}$	Rohm 0.18μm, 1.8V	6%	96%: R-2R network 82.6%: Op Amp 2kΩ resistance variation

3.6. Conclusions

The resistance-matching based BIST technique for the current-mode R-2R ladder

DAC has been presented and can be used through the whole cycle of the DAC from the design stage to production test stage, even in the field operation with acceptable fault coverage. The cutting of the resistor network enhanced the sensitivity of the possible faults in DUT and simplified the output analyzing circuit which checks only one voltage range to determine the test of the R-2R network passed/failed. Two complementary test currents were designed particularly to sensitize the nMOS and pMOS of the injected analog switches in the R-2R network. With the faults sensitization strategy of the network cutting and complementary currents stimulus, the proposed technique has offered high fault coverage of 96% for the R-2R network and 82.6% for the op amp. Also, the parametric faults of more than 2kΩ resistance variation in each resistor of the R-2R network were detected. Therefore, the proposed BIST technique can be an effective alterative test approach for the current-mode R-2R ladder DAC.

Chapter 4. A CM BIST Technique for FD S/H Circuits

This chapter presents a Common Mode (CM) BIST technique for Fully Differential (FD) Sample-and-Hold (S/H) circuits, due to the FD topologies are commonly used to eliminate the clock feedthrough and charge injection to a first order in S/H circuits. The S/H circuits are always used as the input stage of the ADCs. In the FD S/H circuits, the FD Op Amp usually employs a Common-Mode Feedback (CMFB) circuit to keep the CM output to the desired value, and the CM gain in the linearized FD Op Amp is approximately zero. As a result, the CM output variation caused by the variation of the CM input in the acceptable range is small due to the small CM gain, and the performance of the small CM gain in FD Op Amps is employed to test FD S/H circuits based on the CM setup in this study.

Under test mode, the two inputs of FD S/H circuit are connected to a varying input, and then the test controller sets the FD S/H circuit to sample or hold mode, finally the possible faults can be detected by checking the differential outputs, which should vary around the desired CM output of the FD Op Amp used in the FD S/H circuits under test.

The rest of this chapter is organized as follows. Section 1 gives the overviews on the existing test techniques for S/H circuits. Section 2 presents the characterization of the FD S/H circuit, and the CM test strategy for the FD S/H circuit at the end. Section 3 presents the CM BIST implementation. For illustration, section 4 describes the fault models for S/H circuit and shows the simulation results of a flip-around S/H circuit. Conclusion is finally presented in Section 5.

4.1. Introduction to S/H Circuit and Its Test

4.1.1. Charge Injection and Clock Feedthrough in Analog Switch

Most modern analog MOS circuits include an elementary S/H circuit that combines a sampling switch, implemented by as least one transistor, with a holding capacitor. The major limitation to the accuracy of this circuit is the disturbance of the sampled voltage when the transistor is turned off. One cause is noise, which results in random sequences

of small perturbations. The other is charge injection due to the carries released from the channel and to coupling through gate-to-diffusion overlap capacitances [101]. Also, these two effects are known as charge injection and clock feedthrough shown in Fig. 4.1.

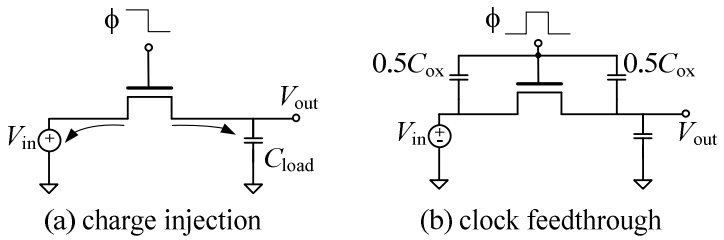


Figure 4.1 Illustration of charge injection and clock feedthrough using an nMOS switch [102].

In general, an MOS switch is not an ideal switch. A finite amount of mobile charge is stored in the channel when an MOS transistor is on. When the transistor turns off, the channel charge disappears through either the source/drain electrodes or the substrate electrode. The channel charge being transferred to the data node superposes an error component to the sampled voltage [103]. This channel charge is the cause of the charge injection. Clock feedthrough is due to the coupling capacitance from the gate to both source and drain. This coupling allows charge to be transferred from the gate signal to the drain and source nodes-an undesirable but unavoidable effect [75].

When MOS switches are on, they operate in the triode region and have zero volts between their drain and their source. Then, through the decreasing of the clock signal ϕ shown in Fig. 4.1, the turnoff of MOS switch can be categorized into two distinct phases. During the first phase, the clock signal is larger than the threshold of the MOS transistor, the transistor is on and a conduction channel extends from the source to the drain of the transistor. As the gate voltage falls, mobile charges exit through both the source end and the drain end. When the gate voltage reaches the threshold voltage, the conduction channel disappears, and the transistor enters the second phase of turn off. During this phase, only the clock feedthrough through the gate-drain overlap capacitance continues to increase the error voltage [103]. In fact, when the transistor enters into the second phase of turn off, the current first decays continuously with time and then tends to saturate until it drop to zero. This indicates that when the gate voltage drops below

threshold, the MOS transistor is operated in weak inversion and thus not only the channel charge in weak inversion but also the feedthrough charges via gate-to-diffusion overlap capacitance contribute to the error voltage [104]. The error is usually very small compare to the charge injection. Also, clock feedthrough is signal-independent which means it can be treated as signal offsets that can be removed by most systems. Many models can be found in [75,101-109] for the detailed descriptions of the charge injection and clock feedthrough.

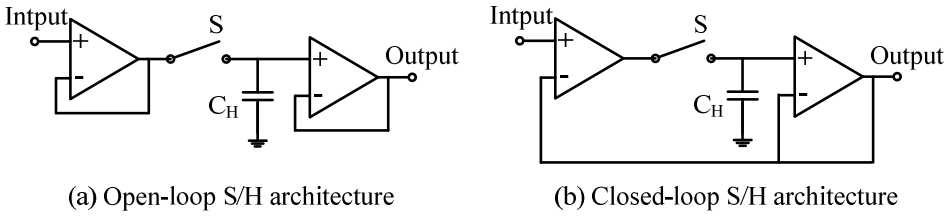
These two nonideal effects typically associated with these switches may ultimately limit the use of MOS switches in the S/H circuits. Additionally, in submicron CMOS technology the supply voltage is reduced to about 1V. This reduction in supply voltage has significant influence on the switching performance of pMOS or nMOS switches [110]. Therefore, many compensation techniques of charge injection and clock feedthrough have been proposed. The single nMOS analog switch can be replaced by dummy switches [75,110, 111], transmission gate switches [75,105], bootstrapped switches [110, 112]. In addition, in different application, different compensation techniques have been used as that in [113-116]. For S/H circuit, the differential architecture is widely used to reduce the effect of the charge injection and clock feedthrough.

4.1.2. S/H Circuits

S/H circuit is an important analog building block with many applications, including ADCs and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing. The circuit has two modes. The sample mode is the digitally controlled state of the S/H circuit during which the output is coupled to the input. The hold mode is the digitally controlled state of the S/H circuit during which the output is held at a fixed level. The S/H circuit is then a digitally controlled circuit which tracks the input signal (after switching transients have settled) during the sample mode and which holds as its output, during the hold mode, a level proportional to the input signal level which occurred as the instant when the circuit switched form the sample to the hold mode [117]. A variety of topologies exists and has been well analyzed in [80,118].

In the S/H circuit, the charge injected to the hold capacitor while the transistor is turned off determines the total error as a result of charge injection and the clock

feedthrough. The simple way of reducing the effect of charge injection and is to large hold capacitor, but the large capacitor would increase the setting time and degrade the performance of the S/H circuit. In addition to the replace the single switch by the dummy switches, transmission gate switches and bootstrapped switches, many charge injection and clock feedthrough cancellation approaches have been proposed based on the conventional open-loop and close-loop S/H circuit architectures shown in Fig. 4.2.



(a) Open-loop S/H architecture (b) Closed-loop S/H architecture

Figure 4.2 Conventional S/H architectures.

The Miller effect provides a mean for dealing with voltages at both ends of capacitor changing at the same time, either independently or dependently [119]. S/H circuit using Miller capacitor has been proposed to reduce the signal dependent charge injection in [120]. The ideal is to use the Miller effect to increase the effective capacitance in hold mode in order to render negligible voltage step resulting from the charge injection. The sample is fast and the switch sizes can be kept small tanks to the small physical sampling capacitor value, which is not multiplied by the Miller effect in sampling mode. The proposed circuit is shown in Fig. 4.3. The equivalent hold capacitance is formed by the combination of capacitors of C_1 and C_2, the MOS pass transistor M2, and an inverting amplifier with gain A. The C_{1B} and C_{2B} represent the parasitic bottom-plate capacitances associated with C_1 and C_2, respectively.

Differential operation is a good way to minimize the influence of clock feedtrough [75]. The circuit is less sensitive to common mode noise, cancels unwanted CM signal/noise and increases the signal swing by a factor of 2 over the single ended structures. Also, the even order distortion tones are significant reduced. Based on the basic architecture of the differential S/H circuit shown in Fig. 4.4, many differential S/H circuits have been proposed. A fully differential double-sampled S/H circuit [121] would give a factor of two increase in the sampling rate compared to the conventional S/H configuration with a similar Op Amp. In [130,122], the conventional closed-loop

S/H circuit was duplicated to implement the pseudodifferential topology, which can reduce the signal-independent error caused by clock feedthrough if the two circuits are matched. Also, a large number of FD S/H circuits [118,123-126] were constructed by FD Op Amps.

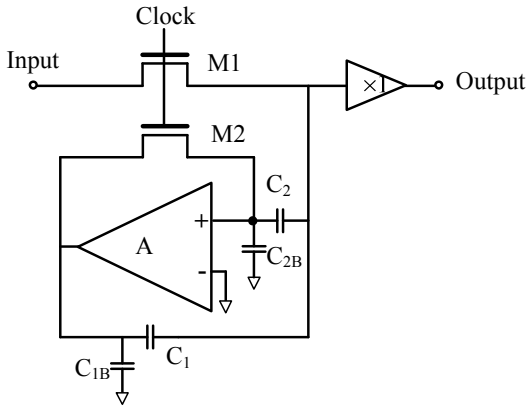


Figure 4.3 S/H circuit using Miller capacitance [120].

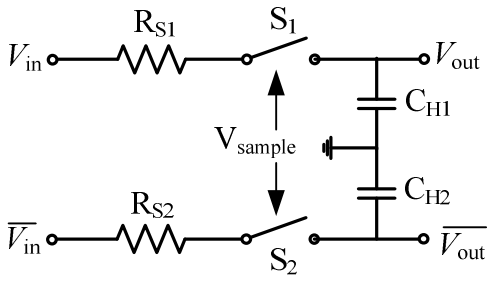


Figure 4.4 Basic differential S/H circuit [110].

In the switched-capacitor topology of S/H circuit show in Fig. 4.5, the (input-dependent) charge injected by S_1 onto C_H does not appear in the held output voltage, since S_2 turn off first. Moreover, as S_2 is connected to virtual ground, its channel charge does not depend on the input signal. In a differential circuit, this charge would simply cause a common-mode offset, which can be easily eliminated by the offset compensation techniques.

Bottom plate sampling [102,127-129] technique is often used to cancel the charge injection in S/H circuit. As shown in Fig. 4.6, when the ϕ_1 switch turns off, the charge injection into C_H is a constant independent of the input signal amplitude. The resulting

offset voltage across C_H is then constant. When the ϕ_2 switch turns off, the resulting charge injection then takes the path of least resistance, this is, into the input source V_{in}. The voltage across C_H is then, ideally, independent of the input signal voltage. Turning the ϕ_1 controlled switch off slightly before the ϕ_2 controlled switch is sometimes called bottom plate sampling. This switch controlling scheme has been applied in many S/H architectures.

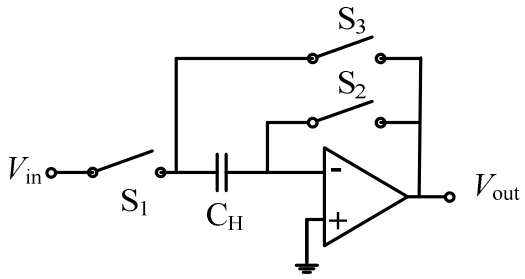


Figure 4.5 Switched-capacitor S/H circuit [80].

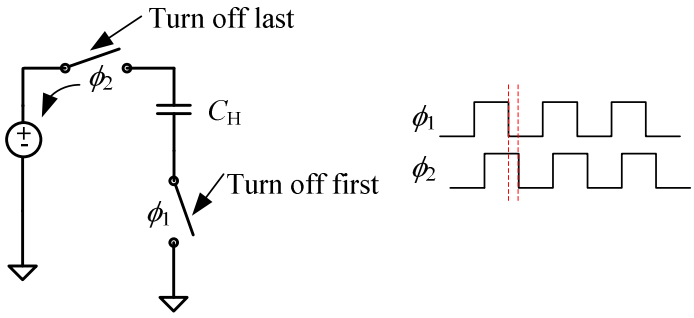


Figure 4.6 Bottom plate sampling [102].

The main ideal Switched Op-Amp (SOP)-based S/H circuit [130,131] is to operates the MOSFET in saturation region instead of the triode region as is the case of the traditional MOS transistor, so the channel will be pinched off and disconnected from the drain. The transistors at the output node in the SOP, are turned off while the MOS transistors are operated in the saturation region. During the sample mode, the SOP behaves like a regular Op Amp. Then, during hold mode, the SOP is turned off and the output of the SOP is held as high impedance, so no channel charge will flow into the output node (hold capacitor). Further more, the remaining clock feedthrough error can be cancelled out by using a differential topology like pseudo-differential S/H circuit.

In modern low voltage application, many charge injection compensation techniques have also been employed in current-mode S/H circuits, and the detail can be found in [132-135].

Each of above mentioned technique has its own advantages and disadvantages, so some of them are often combined to design a high performance S/H circuit.

4.1.3. Overviews on S/H Circuit Testing

As mentioned before, all circuits can be tested by measuring the performance parameters, so the specification-based test of S/H circuit would also be implemented based on the static and dynamic test setups show in Fig. 4.7.

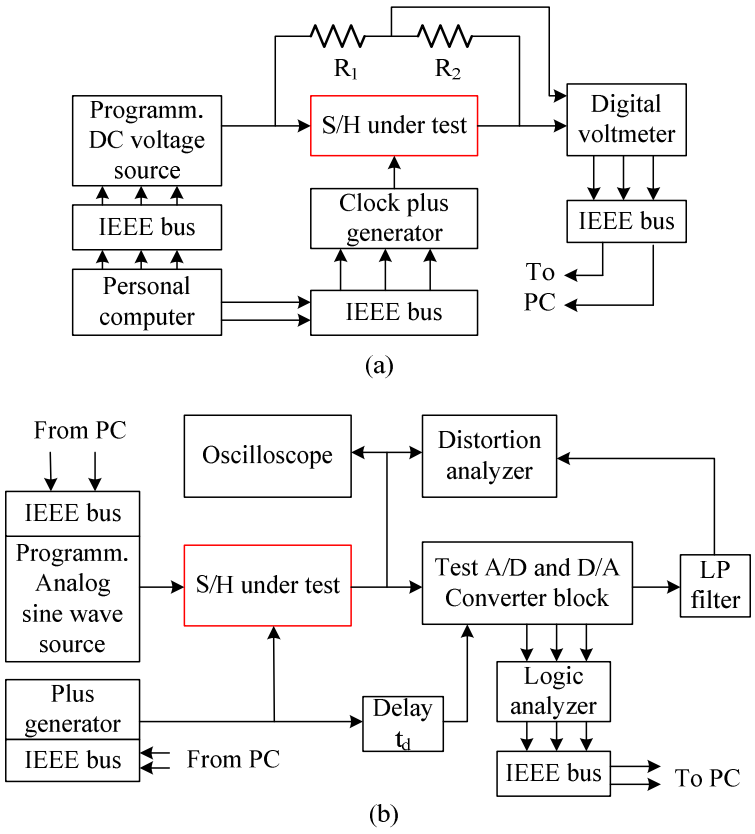


Figure 4.7 Test setup for S/H circuit [110]: (a) Testing DC characteristics. (b) Dynamic measurements.

In [136], the digital voltmeter was applied to test the S/H circuit by measuring the difference between the output and the input voltages based on a logic-control input of

plus generator. Also, some of the performance parameters can be used in the fault-based test like acquisition time and hold-mode droop rate [137].

In the transient response based test technique [138], a 100ns plus was applied to the input of the S/H circuit under test when it is under sample mode, then four arbitrary in the test response including both voltage and supply current were sampled to determine the test result. A single micro-coded finite state machine, a DAC and a window comparator coordinated the BIST scheme.

In [139], the board level test design for a FD Operational Transconductance Amplifier (OTAs) was presented, and it can measure the most DC and AC parameters of an OTA under test. In this case, signal generator, analog oscilloscope and other analyzer are needed to measure the performance parameters.

Then, based on the symmetry characteristics of the FD circuit, the self-checking based test technique was first proposed in [140,141]. The FD circuits are designed with symmetrical inputs and outputs with respect to the analog ground, in some cases, middle of the power supplies, also the internal differential nodes. Given two differential nodes 1 and 2, the signals S_1 and S_2 at node 1 and node 2 should meet the relation of $S_1 + S_2 = 2S_b$, S_b is the bias value depended on the circuit design, or the CM value. Hence, the FD circuits can be tested by monitoring these differential nodes in the FD circuits under test, and it can be used in the self-checking as it is shown in Fig. 4.8. The typical self-checking is to monitor the outputs for final test result. In fact, the internal differential nodes can also be monitored to test the FD circuits, such as in [142] the inputs of all differential amplifiers used in the FD SC filter under test were on-line observed.

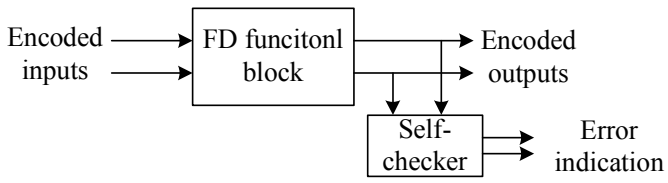


Figure 4.8 The general structure of self-checking [140, 141].

This test scheme is mainly employed for concurrent error checking (on-line test) for FD circuits. In this case, the main challenge becomes to the design of the self-checking circuit, so many self-checking circuits were proposed in [142-147].

As an experiment example of the self-checking, a self-checking FD S/H was proposed in [141]. In addition to the outputs observing, the CM voltage shored on the two hold capacitors was also checked to improve fault coverage with the benefit of an adding testing phase.

With the exciting of the test signals like sine wave, the self-checking circuit can be reused for off-line BIST application during the manufacturing test. However, since the hard precise measurement for analog signal and complex stimulus generator like the oscillator [145,146], these existing test techniques are difficult to BIST application for FD S/H circuits. Therefore, a CM BIST technique is presented for FD S/H circuits, which can be used as the input stage of ADCs and in modern SoC with the proposed CM BIST circuits.

4.2. The CM Test Strategy

4.2.1. FD Op Amp with CMFB

FD Op Amps are widely sued in modern low-voltage IC because they have some advantages over the single-ended Op Amps. They provide a larger output swing and are less susceptible to common-mode noise. Also, the even-order nonlinearities are not present in the differential output of a balanced circuit [77].

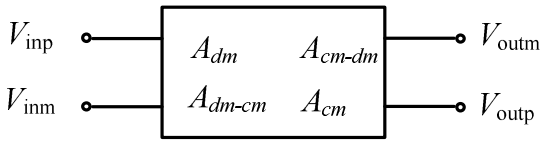


Figure 4.9 The typical architecture of the FD Op Amp.

As it is shown in Fig. 4.9, the typical architecture of the FD Op Amp (differential inputs and outputs) can be described by several transfer functions. With reference to the differential inputs V_{inp} and V_{inm}, the DM input V_{id} and CM or average input are

$$V_{id} = V_{inp} - V_{inm}, \quad V_{ic} = \frac{(V_{inp} + V_{inm})}{2} \tag{4.1}$$

Also, the DM output V_{od}, and CM or average output V_{oc} are

$$V_{od} = V_{outp} - V_{outm},\ V_{oc} = {(V_{outp} + V_{outm})}/{2} \tag{4.2}$$

Then, the relationship between the DM and CM inputs, and the DM and CM outputs can be constructed as

$$V_{od} = A_{dm}V_{id} + A_{cm-dm}V_{ic},\ V_{oc} = A_{dm-cm}V_{id} + A_{cm}V_{ic} \tag{4.3}$$

Where DM gain A_{dm}, CM gain A_{cm}, DM-to-CM gain $A_{\mathrm{dm\text{-}cm}}$, and CM-to-DM gain $A_{\mathrm{cm\text{-}dm}}$ are

$$A_{dm} = \left.\frac{V_{od}}{V_{id}}\right|_{V_{ic}=0},\ A_{cm} = \left.\frac{V_{oc}}{V_{ic}}\right|_{V_{id}=0},\ A_{dm-cm} = \left.\frac{V_{oc}}{V_{id}}\right|_{V_{ic}=0},\ A_{cm-dm} = \left.\frac{V_{od}}{V_{ic}}\right|_{V_{ic}=0} \tag{4.4}$$

The desired output is differential, and its variation should be proportional to the variation in the differential input. Variation in CM is undesired because it must be rejected by another differential stage to sense the desired differential signal [77]. Therefore, the A_{dm} should be larger enough than other three gain coefficients. In the differential amplifiers with perfect symmetry, $A_{\mathrm{dm\text{-}cm}}$ and $A_{\mathrm{cm\text{-}dm}}$ are zero, but in most cases, A_{cm} is not zero even with perfect symmetry. Furthermore, in practice, the regular FD Op Amps are not perfectly balanced (A balanced circuit is symmetric with perfectly matched elements on either side of an axis of symmetry [77]), so $A_{\mathrm{dm\text{-}cm}}$ and $A_{\mathrm{cm\text{-}dm}}$ are not zero. The CM output V_{oc} can even be signal dependent due the high A_{cm}, nonlinearity and device mismatches [148].

Additionally, the feedback around the FD Op Amp just provides stabilization for output DM component, while the CM is still operating in open-loop mode. The require control of the output amplifier CM component must be provided by an additional internal feedback, which is known as CMFB network [149,150]. The CMFB circuit is a circuit sensing the CM voltage, comparing it with a proper reference and feeding back to correct the CM signal with the purposed to cancel the output CM current component, and to fix the DC outputs to the desired voltage. That is to say, the CMFB is used to keep the differential outputs balanced around, and the basic structure of a FD Op Amp with CMFB is shown in Fig. 4.10.

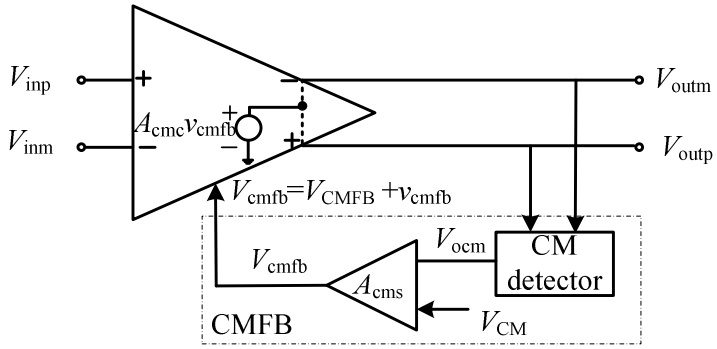


Figure 4.10 The basic structure of a FD Op Amp with CMFB [77].

To set the V_{oc} to the desired DC voltage V_{CM}, the CMFB circuit first calculates the CM output of the FD Op Amp using the CM detector and output the monitored CM voltage V_{ocm} to an amplifier. Then, V_{ocm} is subtracted from the desired output V_{CM}, the difference (V_{ocm} - V_{CM}) is scaled by the amplifier with gain A_{cms}. Finally, the output $V_{cmfb} = A_{cms}(V_{ocm} - V_{CM}) + V_{CMFB}$ is feed back to the FD Op Amp to control the CM output through the internal CM controlling path with the gain A_{cmc}, V_{CMFB} is the DC component of the CMFB output, and exists in the output of the amplifier with gain A_{cms}. In this internal CM controlling path, the changing component v_{cmfb} in the V_{cmfb} is amplified to prevent the CM output V_{oc} variation caused by CM input varying. Consequently, the internal CM controlling path and the CMFB circuit constitute CMFB loop to force $V_{oc} \approx V_{CM}$.

In practice, the CM detector that detects the output CM signal V_{ocm} may have nonlinear characteristics, and the mismatches usually exist in the FD Op Amp with CMFB. As a result, the $A_{dm\text{-}cm}$ and $A_{cm\text{-}dm}$ would not be zero. The detected CM output V_{ocm} which is the output of the CM detector, would impact the CM output of V_{oc} and DM output of V_{od}, and vice versa. The gain paths in the Fig. 4.10 are extracted and shown in Fig. 4.11. A_{dm}, A_{cm}, $A_{dm\text{-}cm}$ and $A_{cm\text{-}dm}$ are the original gain coefficients of the FD Op Amp without CMFB. After the CMFB was injected, four new gain coefficients were added. They are $A_{ocm\text{-}dm}$, $A_{dm\text{-}ocm}$, $A_{cm\text{-}ocm}$ and $A_{ocm\text{-}cm}$. $A_{ocm\text{-}dm}$ is the detected CM output to the DM output gain caused by the mismatches in the amplifier with gain A_{cms} and the CM controlling path shown in Fig. 4.10. $A_{dm\text{-}ocm}$ is the DM output to the detected CM output gain caused by the mismatch in the CM detector. $A_{cm\text{-}ocm}$ is the gain of the CM detector. $A_{ocm\text{-}cm}$ is CMFB loop gain A_{cms} (A_{cmc}). The CM gain from V_{ic} to V_{oc}

is affected by the CMFB loop, and can be calculated using the gain paths model of the FD Op Amp with CMFB. The A_{cm} is changed to A'_{cm}

$$A'_{cm} = \left.\frac{V_{oc}}{V_{ic}}\right|_{with\ CMFB} = \frac{A_{cm}(1 - A_{dm-ocm}A_{ocm-dm}) + A_{cm-dm}A_{dm-ocm}A_{ocm-cm}}{1 - A_{cm-ocm}A_{ocm-cm} - A_{dm-ocm}A_{ocm-dm}}$$

$$\cong -A_{cm-dm}\frac{A_{dm-ocm}}{A_{ocm-cm}} \cong 0 \tag{4.5}$$

As described in Eq. 4.5 [149,150], the addition of the CMFB would significantly degrade the original CM gain to approximately zero in the balanced design. However, the outputs of certain designs might be not balanced due to two potential causes of nonlinear CM detector and the insufficiently large open-loop gain of the CMFB [148]. Therefore, the CM gain of FD Op Amp with CMFB might not be definitely zero, but it should be small when FD Op Amp inherently has as a high CM open-loop gain as possible in order to design a balanced-output FD Op Amp.

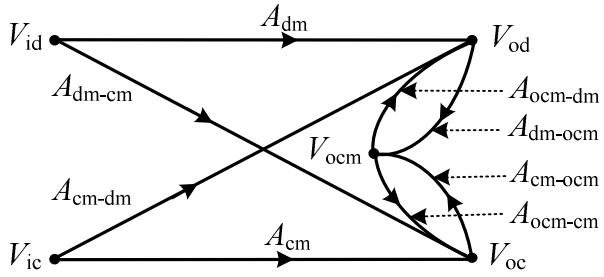


Figure 4.11 Gain paths in the FD Op Amp with CMFB [150].

Figure 4.12 and 4.13 show two FD Op Amp examples. In the case of the two-stage balanced FD Op Amp, the CMFB is merged with the DM circuit at the very front end of the amplifier. The CM detector, consisting of C_1, C_2, R_1 and R_2, senses the CM output and sends it to the gate of M13. Then, compared with the desired CM setting voltage V_{CM} , which is input to the gates of M14 and M15, the currents from M14 and M15 are merged with the differential input stage. The currents in M5 and M6 are controlled by M13 through M11. Consequently, M11~M15 constitute the CMFB network with the

CM detector.

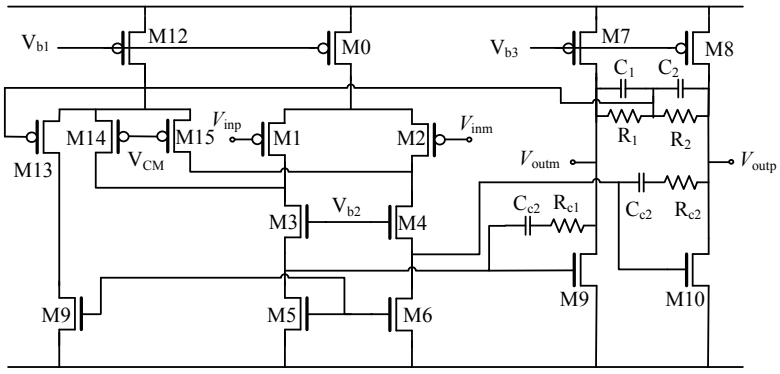
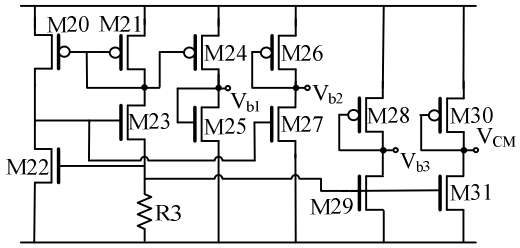
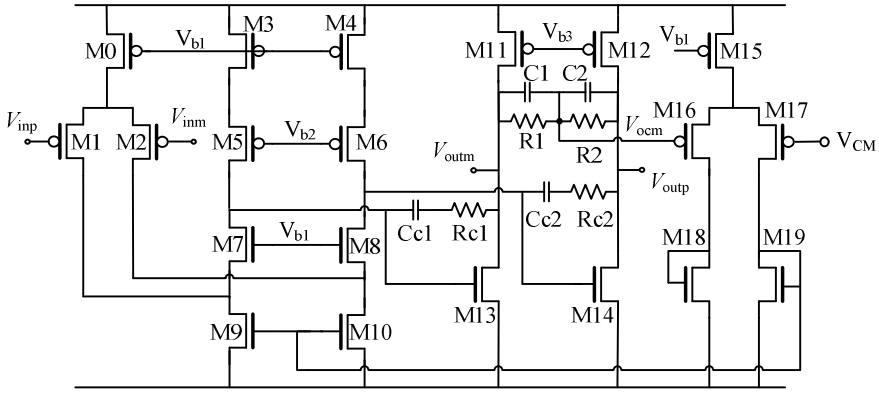


Figure 4.12 A two-stage balanced FD Op Amp [148].



(a) Bias circuit for the FD op amp.



(b) A folded-cascode FD op amp.

Figure 4.13 A folded-cascode FD Op Amp.

In the case of the folded-cascode FD Op Amp, the differential outputs are also sensed by the RC CM detector, consisting of C_1, C_2, R_1 and R_2 shown in Fig. 4.13. Then, the detected CM output is compared with the desired CM voltage V_{CM}, and the difference is amplified to control the currents through M9 and M10 in order to stabilize

the CM output. The element size settings are lists in Table 4.1 for the two FD Op Amps.

Table 4.1 Summary of the elements parameters of the two FD Op Amps.

Circuit	*Element*	*Parameters*	*Element*	*Parameters*
Two-stage FD Op Amp shown in Fig. 4.12	M0~M2	30/0.4 μm (W/L)	M3, M4, M15, M28	10/0.4 μm (W/L)
	M5,M6, M20~M23, M29, M31	20/0.4 μm (W/L)	M7, M8	20/0.2 μm (W/L)
	M9, M10	26/0.4 μm (W/L)	M11, M12	35/0.4 μm (W/L)
	M13, M14	10/0.2 μm (W/L)	M16, M17, M24	40/0.4 μm (W/L)
	M18, M19	6.8/0.4 μm (W/L)	M25, M27	4/0.4 μm (W/L)
	M26	7.6/0.4 μm (W/L)	M30	13.2/0.4 μm (W/L)
	R_1, R_2	10 kΩ	C_1, C_2	1 pF
	R_{c1}, R_{c2}	0.5 kΩ	C_{c1}, C_{c2}	1.4 pF
	R_3	3 kΩ	--	--
Folded-cascode FD Op Amp shown in Fig. 4.13	M0, M12	16/0.4 μm (W/L)	M1, M2, M7, M8	48/0.4 μm (W/L)
	M3, M4	48/0.18 μm (W/L)	M5, M6	24/0.18 μm (W/L)
	M9, M10	36/0.4 μm (W/L)	M11	12/0.4 μm (W/L)
	M13	40/0.4 μm (W/L)	M14, M15	20/0.4 μm (W/L)
	R_1, R_2	20 kΩ	C_1, C_2	1 pF
	R_{c1}, R_{c2}	2 kΩ	C_{c1}, C_{c2}	0.65 pF

Figure 4.14 shows the two FD Op Amps' CM simulation results, where the two inputs are connected to a varying input between the two power supplies. When the CM input changes from 0V to about 0.9V, the CM output are almost stable. However, the CM output changes to another value when the CM input is greater than about 0.9V, because the pMOS transistors in input stage were turned off. Therefore, the variation of the CM input in the acceptable input range causes only a little change to the desired CM value due to the low small-signal CM gain. As a result, the performance of the small CM gain in FD Op Amps was employed to test FD S/H circuits based on the CM setup in this work.

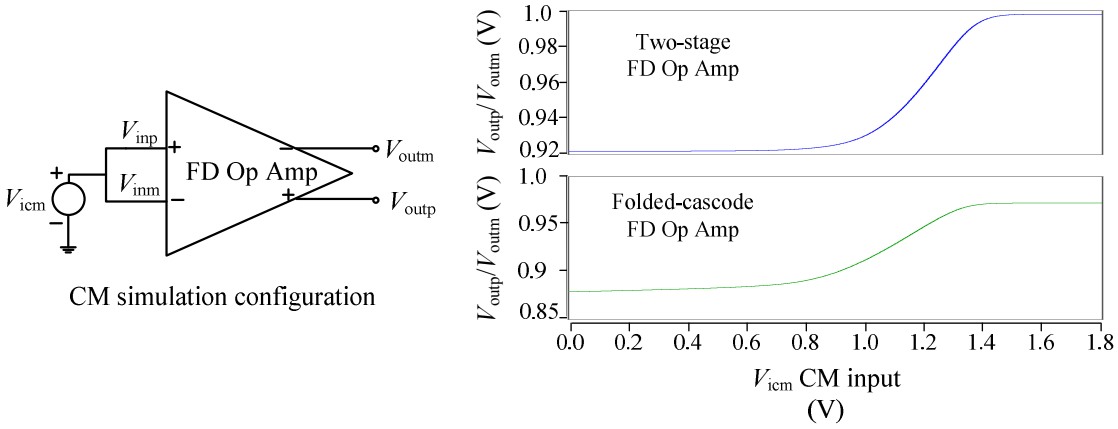


Figure 4.14 The CM input to CM output relationship of the two Op Amps.

4.2.2. CM Test for FD S/H Circuit

Most FD S/H circuits are mainly constituted by the FD Op Amp, and Fig. 4.15 shows a flip-around FD S/H circuit with its operation modes. Under sample mode, S_1 and S_2 are on, and S_3 is off. The left terminals of the hold capacitors are connected to the inputs, so the voltages at these two terminals change following with the inputs. Under hold mode, S_1 and S_2 are off, and S_3 is on. The sampled voltages would be held in the hold capacitors and sent to the output terminals of the S/H. These switches are controlled by the non-overlapping two-phase clock generator shown in Fig. 4.16 with its output waveforms according the clock input V_{CLK}.

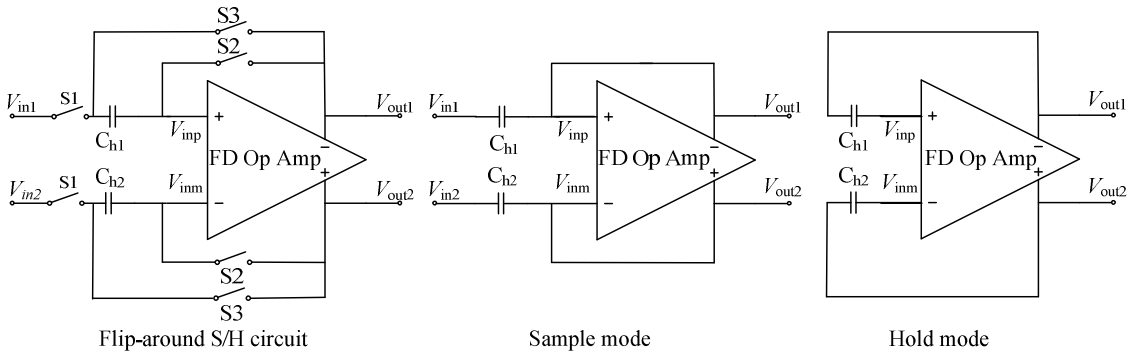


Figure 4.15 A flip-around S/H circuit and its operation modes.

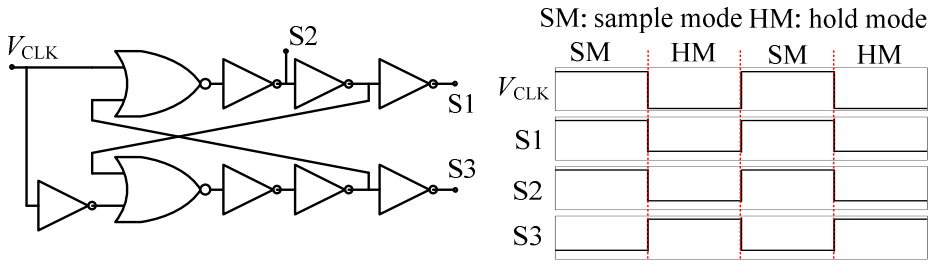


Figure 4.16 A non-overlapping two-phase clock generator and its timing waveforms.

When V_{in1} and V_{in2} shown in Fig. 4.15 are connected to a varying test signal, V_{out1} and V_{out2} output two same voltages fluctuating around the desired CM value, which is set by the CMFB circuit in the FD Op Amp used in the FD S/H circuit.

When switches *S1* and *S2* turn on, and *S3* turns off, the S/H circuit enters into the sample mode. The voltages at the left terminals of the hold capacitors follow the test input voltage. In such a case, the FD Op Amp is operating in a unity-follower configuration with the feedback connection. As a result, due to the small CM gain of the FD Op Amp, the outputs (V_{out1} and V_{out2}) of the FD S/H are held at the desired CM output value even the CM test input changes a lot.

When switches *S1* and *S2* turn off, and *S3* turns on, the FD Op Amp is switched into the hold mode working like a voltage follower. The voltage difference across each hold capacitor in present hold mode is kept to the voltage sampled at the last sampling moment and are expressed as

$$(V_{in1} - V_{inp})\Big|_{sample\ mode} = (V_{out1} - V_{inp})\Big|_{hold\ mode} \tag{4.6}$$

$$(V_{in2} - V_{inm})\Big|_{sample\ mode} = (V_{out2} - V_{inm})\Big|_{hold\ mode} \tag{4.7}$$

Also, under the hold mode the differential points in the FD S/H circuit should have same value

$$V_{inm} = V_{inp}, \quad V_{out1} = V_{out2} \tag{4.8}$$

since V_{in1} and V_{in2} are connected to the CM test signal in the sample mode. As it is

shown from the FD Op Amp's CM simulation results in Fig. 4.14, the same test input to V_{inp} and V_{inm} forces FD Op Amp to output two same voltages, which approximately equal to the desired CM voltage controlled by the CMFB circuit. To meet the conditions of Eq. 4.6, Eq. 4.7 and Eq. 4.8 under this CM test, the inputs V_{inp} and V_{inm} of the FD Op Amp are synchronously driven to another value to force the FD S/H circuit to a new equilibrium under hold mode, and the outputs (V_{out1} and V_{out2}) should be held around the desired CM voltage.

Consequently, the differential outputs of the FD S/H circuit under CM test should have same value around the desired CM output value in the sample or hold mode when the FD S/H circuit performs correctly with the CM test setup (connecting the two inputs to a test signal). Figure 4.17 shows the CM test simulation results of the flip-around FD S/H circuit shown in Fig. 4.15, which is composed of the folded-cascode FD Op Amp shown in Fig. 4.13 and six transmission gate switches. The transmission gate consists of an nMOS transistor of 2/0.18 μm (W/L) and a pMOS transistor of 2/0.18 μm (W/L), and the hold capacitors are set to 0.7pF.

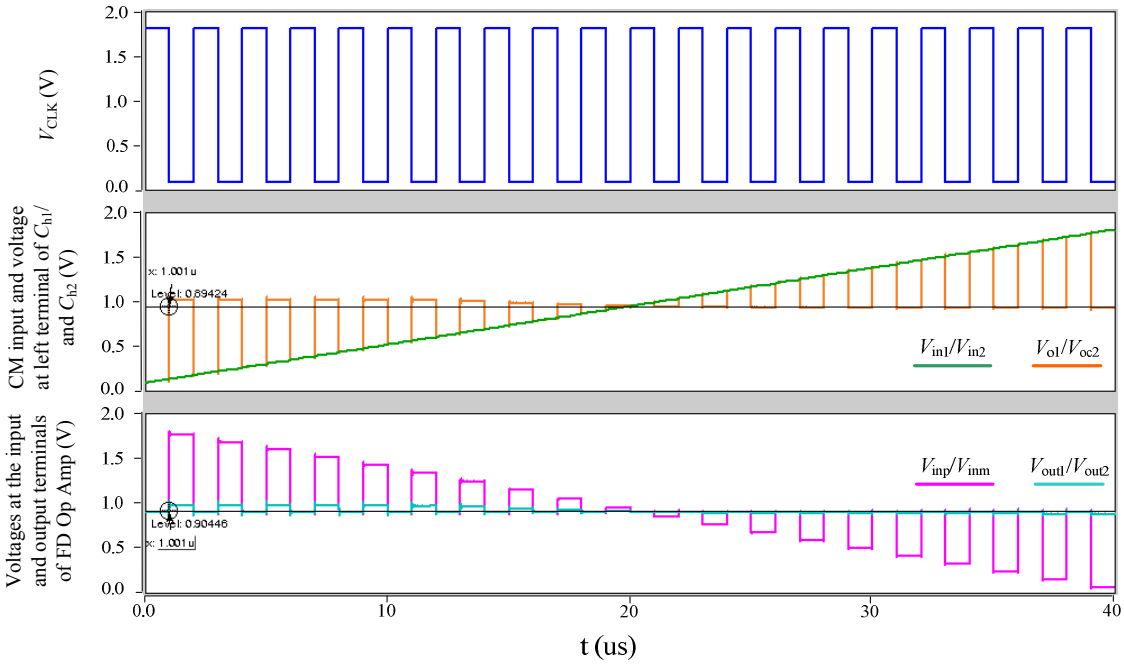


Figure 4.17 The CM simulation results of a FD S/H circuit.

In this CM simulation, the inputs V_{in1} and V_{in2} were connected to test signal which changed from 0V to 1.8V in 40 us. The clock input V_{CLK} switches the operation modes

of the FD S/H circuit. The voltages of V_{o1} and V_{o2} at the left terminals of the hold capacitors changed with the CM input when the FD S/H circuit operated under sample mode, and the inputs (V_{inp} and V_{inm}) and outputs (V_{out1} and V_{out2}) of FD Op Amp were held at approximately 0.899V. When the FD S/H circuit was switched to hold mode, the voltages (V_{o1} and V_{o2}) and the outputs (V_{out1} and V_{out2}), changed from about 0.973V to 0.88V during the CM input changed from 0V to 1.8V. However, they almost stabilized to about 0.88V when the input was greater than approximately 0.9V, because the inputs of the FD Op Amp were changed from 1.765V to 0.057V, that is to say the transistors in input stage of the FD Op Amp were turned off when the CM input was smaller than about 0.9V.

Additionally, V_{out1} and V_{out2} just approximately equal to each other due to the process variation and mismatch in the realistic circuit. Therefore, when the inputs of the FD S/H circuit is connected to the CM test signal, the outputs based fault signature should be summarized as

$$(V_{CM} - \delta_1) \le \frac{V_{out1} + V_{out2}}{2} \le (V_{CM} + \delta_2) \quad and \quad \left|V_{out1} - V_{out2}\right| \le \varepsilon \tag{4.9}$$

where

V_{CM} is the desired CM output value of the FD Op Amp,

δ1 and δ2 are used to set the fluctuations space of the CM output, mainly caused by the mismatch in the symmetrical circuit,

ε is the acceptable maximum difference of the two outputs.

4.3. The CM Test System Implementation

The CM test setup for FD S/H circuit can be implemented by BIST circuits shown in Fig. 4.18, including the CM test signal generator, CM output checker and test controller. The stimulus generator creates a varying test signal to the inputs, and the output analyzer is to implement the outputs checking based on the output fault signatures shown in Eq. 4.9 following the control signals shown in Fig. 4.19.

At t_1, V_{TM} is set to logic high to start the test and turns on the switch S_{TM} to connect the inputs and outputs of the FD S/H circuit under test to the output of the CM test

stimulus generator and the inputs of the CM output analyzer, respectively. Afterwards, at t_2, the test clock signal V_{CLK} goes to logic high and switches the FD S/H circuit to sample mode through its associated clock generating circuit, which controls the switches (S_1, S_2 and S_3). Then, at t_3, V_{TMC} goes to logic low for the purpose of shifting the CM test signal V_{TCM}. Finally, at t_4, V_{CLK} returns to logic low to switch S/H circuit to sample mode. During the CM test, the transient signal is employed as a CM test input to excite the faults existing in the FD S/H circuit with the help of the switching of the control signals, and the output analyzer observes two outputs and creates a final test result $V_{p/f}$. Note that the test clock signal V_{CLK} can also use the normal operation clock waveforms of the FD S/H circuit.

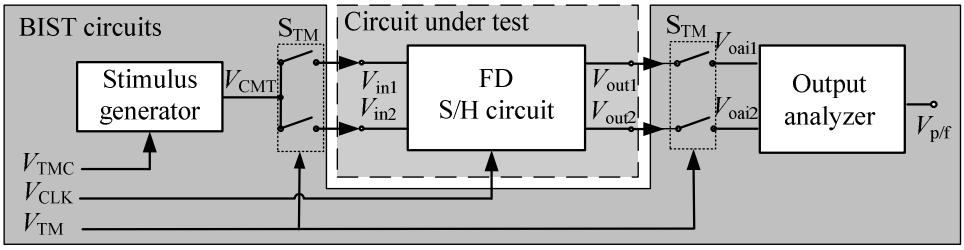


Figure 4.18 The CM BIST setup for FD S/H circuit.

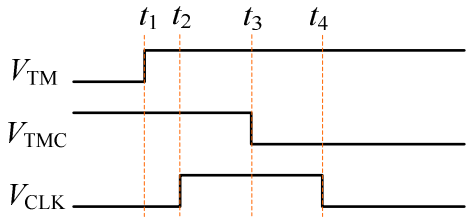


Figure 4.19 The timing waveforms for the CM test controlling signals.

The transient signal which was employed as the CM test input is generated by switching the logic input V_{TMC}, and the stimulus generator shown in Fig. 4.20 would output two different voltages by turning off or on the transistor MS2, so a step signal can be generated by switching V_{TMC}. Note that V_{CMT} must be set carefully to ensure the FD Op Amp working in its linear region after the new equilibrium under hold mode.

As it can be seen from Fig. 4.20, the output analyzer is composed of three stages: a differential amplifier, a window comparator and a SR latch. The differential amplifier at

the first stage was designed to observe the CM voltage and the difference of the FD S/H circuit's outputs. On the one hand, the fault-free outputs (V_{out1} and V_{out2}) should make the differential amplifier's output (V_{ot}) be hold between the two checking thresholds of V_{tl} and V_{th}. On the other hand, the shifted CM value and/or the enlarged difference of the outputs from the FD S/H circuit under test would derive V_{ot} to exceed the thresholds V_{tl} and V_{th} depended on the differential amplifier's differential gain and CMRR. V_{tl} and V_{th} are the V_{ot} voltages corresponding to the boundary inputs of V_{oai1} and V_{oai2}, and the boundaries are determined by the coefficients of $V_{CM,}$ δ_1, δ_2 and ε seen in Eq. 4.9 from the fault-free simulation of the FD S/H circuit under test.

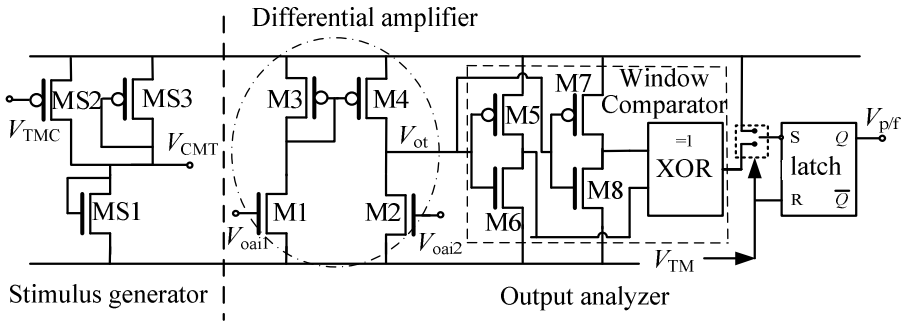


Figure 4.20 The designed BIST circuits for FD S/H circuit CM test.

Figure 4.21 demonstrates the thresholds transferring using the voltage-transfer curves. Two types of simulation were carried out, in the first case, V_{oai2} was fixed to 0.9V, and V_{oai1} varied from 0V to 1.8V, the output V_{ot} can be used to demonstrate the DM amplification characteristic of the differential amplifier. In another case, the inputs of V_{oai2} and V_{oai2} were connected and varied from 0V to 1.8V, so the output V_{ot} is to demonstrate the CM amplification characteristic. Based on the CM and DM amplification characteristics of the differential amplifier, the two thresholds of V_{tl} and V_{th} can be mapped from the real CM output of the FD Op Amp used in the FD S/H circuit, and the coefficients of $V_{CM,}$ δ_1, δ_2 and ε.

Then, the window comparator, including two inverters and a XOR gate, digitizes the analog output V_{ot} with reference to the new fault signature thresholds of V_{tl} and V_{th}. The XOR gate outputs a logic high voltage when V_{ot} swings between V_{tl} and V_{th}, otherwise outputs a logic low voltage.

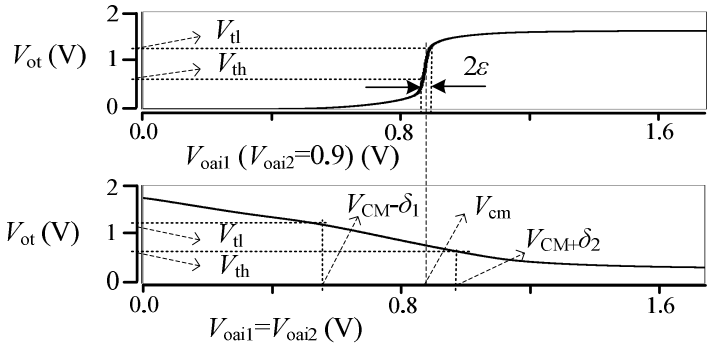


Figure 4.21 Voltage-transfer curves of the differential amplifier.

Finally, the SR latch was added to store the appearance of a logic low voltage at the output of XOR and to generate a final test signature $V_{p/f}$, since some parametric faults existing in the MOS switches or hold capacitors only enlarge the difference between V_{out1} and V_{out2} at the switching moment of the control signals. Consequently, the appearance of logic high at $V_{p/f}$ means the injected fault in the FD S/H circuit can be detected.

The element parameters of the BIST circuits are listed in Table 4.2, and also the related performance parameters are summarized.

In this work, no special test controller was designed because the FD S/H circuit under test is assumed as one part of an analog and mixed-signal system, and the test controlling signals can be easily implemented by the digital part.

Table 4.2 The element size settings and performances of CM BIST circuits.

BIST Circuits Shown in Fig. 4.20		***Sizes of Elements (W/L μm)***	***Performances***
Stimulus generator		MS1: 1.5/0.18 MS2: 0.6/0.18 MS3: 8/0.18	V_{CMT} = 0.6 V when V_{CMT} = '1' V_{CMT} = 1.5 V when V_{CMT} = '0'
Output Analyzer	**Differential Amplifier**	M1, M2: 10/0.8 M3, M4: 32/0.8	Differential Gain: 25.7 dB CMRR: 29.6 dB
	Window Comparator	M5: 10/0.18 M6: 0.5/0.18 M7: 0.5/0.18 M8: 5/0.18 Others: 0.54/0.18	V_{tl}: 0.56 V and V_{th}: 1.1 V
	RS Latch	0.54/0.18	--

4.4. Simulation Results

4.4.1. Fault Models for S/H Circuits

For S/H circuits, open, short and incorrect R_{ON} for the MOS switches (S_1, S_2 and S_3), and open, short and incorrect capacitance for hold capacitors have been presented usually to test S/H circuits in [137]. With reference to the fault modeling in Sect. 1.3, shorts were modeled by connecting a small resistor of 100Ω between each pair of terminals (gate-drain, gate-source, and drain-source). Opens were modeled by inserting a parallel combination of a large resistor of 100MΩ and a small capacitor of 10fF in series into each terminal (drain and source). Particularly, gate open was modeled by means of grounded parallel combination of resistor and capacitor for simulating the real behavior of gate open. In this work, the switches were implemented by transmission gates using CMOS technology, so the incorrect R_{ON} can be realized by one transistor's open or short in the transmission gate.

Additionally, parametric faults of the hold capacitors ware modelled by capacitance variation.

4.4.2. The Simulation Results of the Flip-Around FD S/H Circuit

To evaluate the proposed CM BIST technique, a flip-around FD S/H circuit was designed as a test vehicle, including the folded-cascode FD Op Amp shown in Fig. 4.13 with the desired CM output of about 0.9V, six transmission gates in which all transistors were set to 2/0.18 μm (W/L), and two hold capacitors of 0.7pF.

As it has been mentioned, the mismatch in the FD circuit would cause unbalanced outputs, so the physical pattern must be well designed. Figure 4.22 shows two layout pattern examples of the FD S/H circuit, and the CM simulation results shows that the right one formed two better balanced outputs (0.87931V and 0.87927V) than that of the left one (0.88625V and 0.87342V) when the two inputs were set to 0.9V. Therefore, the left one was employed to make up the final FD S/H circuit with the BIST circuits shown in Fig. 4.23. The FD S/H circuit was laid out using Rohm 0.18 μm CMOS technology, and the proposed CM BIST system caused approximately 4% area overhead.

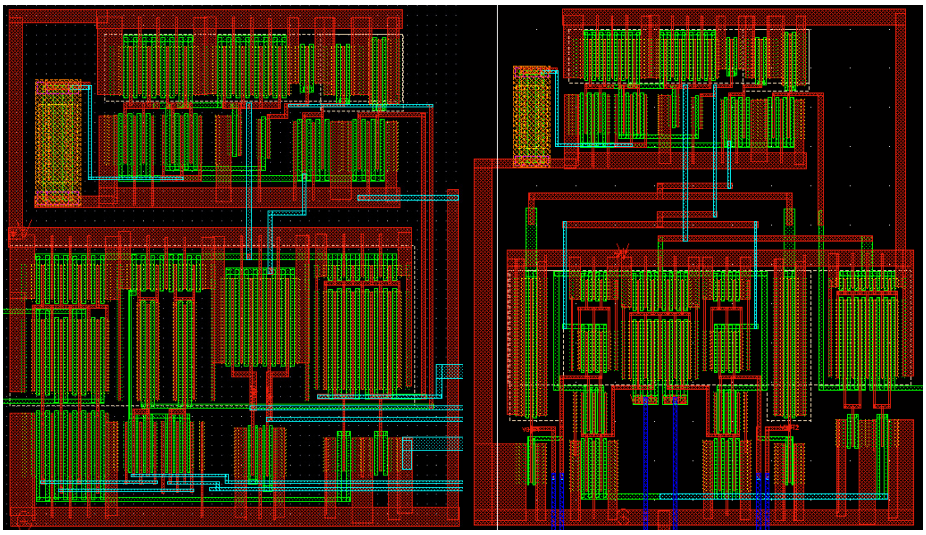


Figure 4.22 Two different layout patterns for the folded-cascode FD Op Amp.

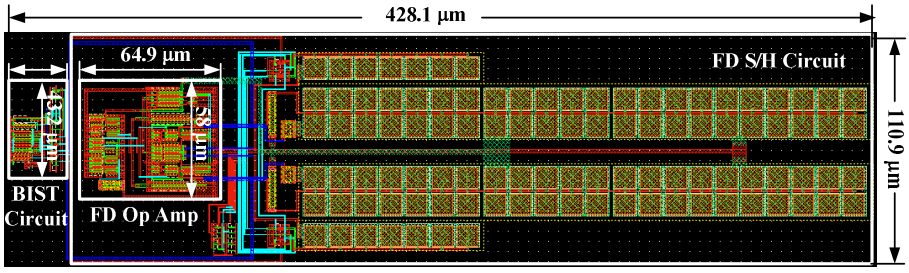


Figure 4.23 The layout pattern of the flip-around FD S/H circuit with the CM BIST circuits.

Figure 4.24 and 4.25 show the CM test fault-free simulation results. As it is shown in Fig. 4.24, in circuit-level, the FD S/H circuit was perfectly matched, so during the CM test the FD S/H circuit outputted two same voltages, which varied between 0.86V and 0.93V. After this, the FD S/H circuit was simulated again with the parasitic parameters extracted for the physical design, Fig. 4.25 shows that the FD S/H circuit outputted two voltages with the maximum difference of 0.92mV and they varied between 0.85V and 0.9V. Therefore, based on parameters of the designed BIST circuits listed in Table 4.2, the thresholds V_{tl} and V_{th} of the differential amplifier in the output response analyzer were designed at 0.56V and 1.1V with the acceptable CM output varying range from 0.87V to 0.94V and maximum difference ε of approximately 15mV owing to the effect of the process variation. In the fault-free case, the test result $V_{p/f}$ should be logic low, so the appearance of logic high at $V_{p/f}$ means the fault injected in

the FD S/H circuit can be detected.

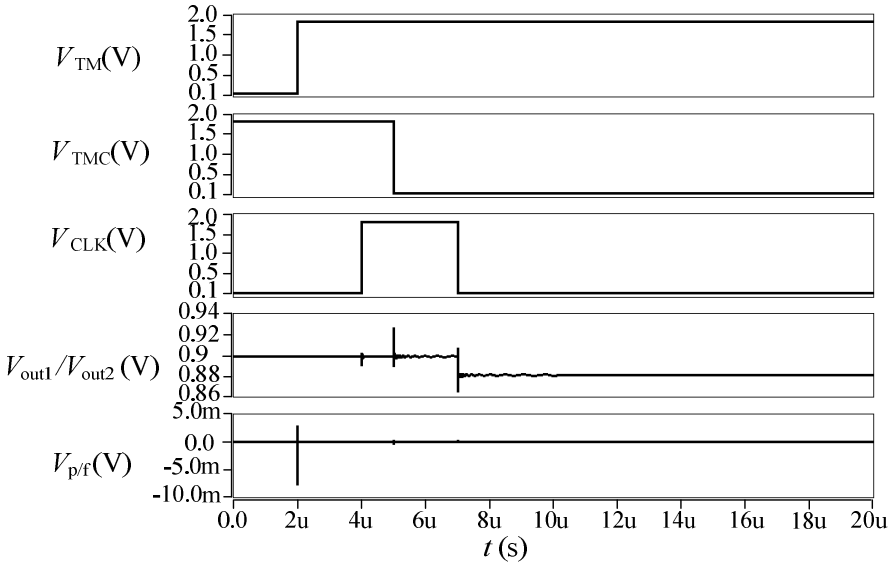


Figure 4.24 Fault-free CM simulation of the flip-around FD S/H circuit in schematic-level.

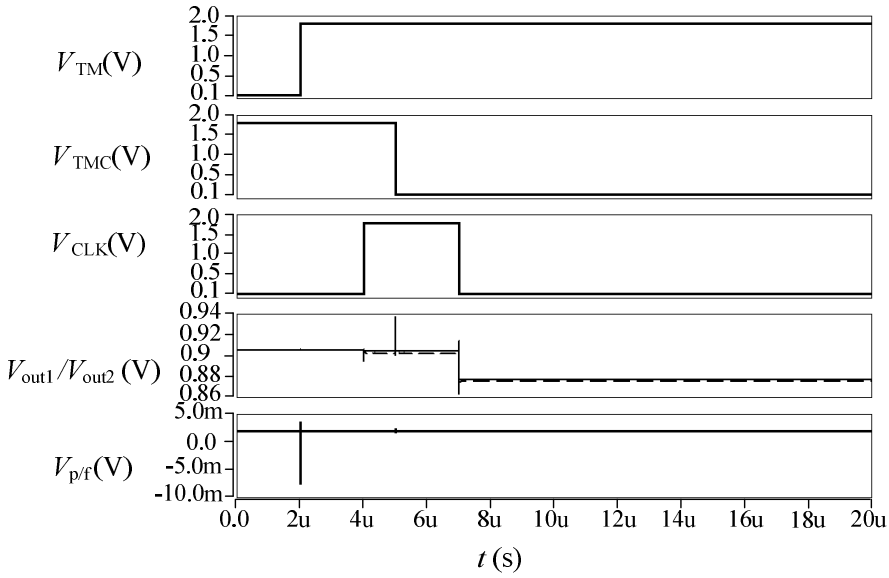


Figure 4.25 The fault-free CM simulation of the flip-around FD S/H circuit after the parasitic extraction form the physical design.

With reference to the fault models introduced previously, 66 faults for transistors used in switches *S1*, *S2* and *S3*, and two faults for each hold capacitor were injected to the FD S/H circuit and only the GO of pMOS transistors in *S3* cannot be detected with

the fault coverage of 97%, and more than 0.2pF capacitance changes of the hold capacitor were detected. The GO of pMOS transistors in *S3* did not change the FD S/H circuit's topology, but change the R_{on} of *S*3, and are parametric faults. These faults would be detected by resetting the thresholds of the differential amplifier used in the output response analyzer, but they should be set based on the test requirement, the fault-free simulation of the FD S/H circuit under test and the possible process variation.

Additionally, 176 faults were detected in the total 195 faults injected in the FD Op Amp with the coverage of approximately 90% by the proposed CM BIST technique, and the main hard-detected faults for the FD Op Amp exist in the voltage biasing circuit shown in Fig. 4.13 (a), because some faults in the bias circuit caused a little change of the four voltage references (V_{b1}~V_{b3} and V_{CM}), and some of them only degraded a little the DM gain of the FD Op Amp. Note that the faults were successively injected to the FD S/H circuit under test.

In comparisons to other S/H circuit testing techniques in the works listed in Table 4.3, the proposed BIST technique does not require a complex generator, and only one transient test signal can achieve high fault coverage, which reduces test cost of silicon area. The fault-free outputs of the S/H circuit under CM test should have same value, which also simplifies the output analyzer design.

4.5. Conclusions

A CM BIST technique has been presented in this chapter for FD S/H circuit used in modern SoC. The proposed CM test setup can capture the transient incorrect outputs caused by the parametric faults like incorrect R_{on} or capacitance, and generate a final test result signal. The FD Op Amp used in the FD S/H circuit can also be tested using the CM setup. With the high fault coverage and low test cost including physical area overhead and test time, the proposed scheme can be an alternative and effective test approach for FD S/H circuits testing in an analog and mixed-signal system.

However, the proposed CM test techniques would cause fault masking when two systematical faults happens, particularly for the systematical parametric faults, so in the future work, this problem should be considered.

Table 4.3 Comparisons of this work and other proposed test techniques for FD S/H circuits.

Features	***Test Strategy***	***BIST Circuits***	***Fault Coverage***	***Area Overhead***
[138]	Performance parameters measuring	N/A (external device)	N/A (possible full coverage)	N/A
[141]	Balance based self-checking with real working inputs	Balance checker, test stimuli	93%: checking output voltage, 100%: improved by checking voltage stored on capacitors	N/A
[147]	Multi-differential points balance checking with frequency varying inputs	Balance checker, oscillator	Almost full coverage for hard faults, possible full coverage for soft faults	N/A
This work	Monitor the same output with CM input	Shown in Fig. 4.20	97%: Switches and capacitors, 90%: FD Op Amp	4%

Chapter 5. Conclusions and Discussions

This dissertation has presented some feasible BIST techniques for data converting system in the analog and mixed-signal LSI system. Chapter 1 has introduced the background of IC testing, DFT, and BIST techniques for analog and mixed-signal circuits, including the specification-based BIST and fault-based BIST techniques. For the typical analog and mixed-signal system, most existing BIST techniques were proposed based on the performance parameters measurement and this is a kind of system test technique which does not consider the internal structure of the data converting system and would cause fault masking and other problems. Therefore, the major objective of this dissertation is to develop new structural BIST for the data converting systems in the analog and mixed-signal system. In this case, the sub-circuits, constituting the data converting system, can be test by its own BIST circuit, and then these BIST are simplified to eliminate the test cost. Hence, the scope of the developed BIST techniques has focused on the basic analog circuits testing and then on the whole the data systems.

As the widely encountered parts in analog and mixed-signal system, Op Amp are widely used, so Chapter 2 has presented two BIST techniques for Op Amps. The first proposed BIST technique is to test Op Amps by checking SOV of the transient response by reconfiguring the Op Amp under test into a voltage follower. Due to the unit feedback circuit and the high gain of the Op Amp, the SOV is almost determined by the input step value for a fault-free Op Amp, so without any parameters modification, the designed BIST system can be applied to test all the Op Amps in an analog and mixed-signal system, even the Op Amps are designed with different architectures. To evaluate the proposed BIST architecture, three Op Amps with different architectures were designed as test vehicles, including a two-stage Op Amp, a cascade Op Amp and a buffered Op Amp. The proposed BIST circuit caused extra area overhead in the original Circuit-under-Test (CUT) of approximately 18.5%. In the case of two-stage Op Amp, 49 faults were detected in the total 52 faults with the coverage of approximately 94.2%. 80 faults of the total 93 faults in the cascade Op Amp were detected with the coverage of approximately 86%, and in the cases of buffered Op Amp, 131 faults were injected in the circuit, 119 faults were finally detected with the coverage of approximately 91%. Therefore, the proposed universal BIST technique can be an effective alternative test approach for Op Amps in the same analog and mixed-signal circuit. Another one is the two-step BIST technique by combining the current-based test with the offset-based test

to detect the physical defects in the Op Amp. In addition to the catastrophic faults, this technique can particularly detect the capacitance variation in the compensation capacitor. The fault simulation in the classical two-stage Op Amp shows that 98% catastrophic faults can be detected. Due to the 5-bit counter the designed BIST circuits caused a large area cost compared to the SOV checking of the transient response, but the area overhead ratio of the BIST circuits to the original circuit would be decreased when the proposed BIST scheme is applied to a more complicated system.

The second proposed BIST technique is the resistance-matching based BIST technique for current-mode R-2R DAC. This is a re-constructing example of the divide-and-conquer strategy. The SOV checking based test technique proposed in the first work has been used to test the Op Amp in the R-2R network DAC. In this case, the DAC was converted into a voltage follower, so the Op Amp can be tested by checking SOV of the transient response. Then, the resistance-matching based test strategy was employed to test the R-2R network based on the tested Op Amp. The circuit-level simulation results of the BIST system for a 8-bit DAC have shown the proposed BIST technique would detect 96% catastrophic faults in the R-2R network and 82.6% in the Op Amp, and the BIST circuits caused approximately 6% area overhead. Additionally, parametric faults of resistance variation were also considered.

Chapter 4 has presented the CM BIST technique for FD S/H circuits which are always used as the input stage of the ADCs. The CM output variation caused by the variation of the CM input in the acceptable range is small due to the small CM gain, so the performance of the small CM gain in FD Op Amps has been employed to test FD S/H circuits based on the CM setup. To evaluate the proposed BIST technique, a flip-around FD S/H circuit has been designed. 66 faults for the analog switches and two faults for each capacitor were injected into the FD S/H circuit, only 2 pMOS gate open faults could not be detected with the fault coverage of 97%, and more than 0.2pF capacitance variation in the 0.7pF hold capacitor were detected. Additionally, 176 injected faults were detected in the total 195 faults to the FD Op Amp, resulting in approximately 90% fault coverage. The proposed BIST circuits were laid out using Rohm 0.18-μm CMOS technology, and caused approximately 4% area overhead.

All proposed BIST techniques have demonstrated possibilities to use unusual signals to excite the circuit under test, like the step signal, and, BIST technique for every sub-circuit used in the data converting system should be well selected based on the requirements of area overhead, test time, fault coverage based on the fault models and the circuit configuration, like the SOV checking based technique was employed in the resistance-matching based BIST technique for R-2R DAC.

The effect to the performance of the data converter caused by analog switches and the BIST circuits should also be considered for analog and mixed-signal circuits, because the whole data converting system was divided into several sub-circuits, so the performance would be degraded and some calibration techniques should be used to eliminate the performance degradation.

For DAC, the comparator, reference and many other sub-circuits have not been considered in this dissertation, so for the future works BIST techniques for these circuits should be proposed. Data converting systems can be constituted by different architectures, so future works are need for these different converters.

Reference

[1] L.T. Wang, C.W. Wu and X.Q. Wen, VLSI Test Principles and Architectures: Design for Testability, Morgan Kaufmann Publisher, 2006.

[2] C.E, Stroud, A Designer's Guide to Built-In Self-Test, Kluwer Academic Publishers, 2002.

[3] A. Grochowski, D. Bhattacharya, T. R. Viwanathan and K. Laker, *"Integrated Circuit Testing for Quality Assurance in Manufacturing: History, Current Status, and Future Trends"*, IEEE Trans. on Circuit and System: Analog and Digital Signal Processing, Vol. 44, No. 8, pp. 610-633, Aug, 1997.

[4] S. Bahukudumbi and K. Chakrabarty, Wafer-Level Testing and Test During Burn-in Integrated Circuits, Artech House Publishers, Feb. 2010.

[5] C. Buck, "*The Economic Benefits of Test During Burn-In: Real-World Experiences*", Proc. IEEE Intl. Test Conf., pp.1086-1093, 1987.

[6] M. Sachdev and J.P.D. Gyvez, Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits, 2nd Ed., Springer, Jun. 2007.

[7] T. Olbrich, V. Liberali and F. Maloberti, "*Design-for-Test Strategies for Analog and Mixed-Signal Integrated Circuits*", Proc. 38th Midwest Symp. on Circuit and System, Vol. 2, pp. 1139-1144, Aug. 1995.

[8] T.W. Williams and K.P. Parker, "*Design for Testability-A Survey*", Proc. of the IEEE, Vol. 71, No. 1, pp. 98-112, Jan. 1983.

[9] P. Kabisatpathy, A. Barua and S. Sinha, Fault Diagnosis of Analog Integrated Circuits, Springer, Jan. 2011.

[10] G.W. Roherts, Chapter 6.2 DFT techniques for Mixed-signal Integrated Circuits, http://www.ece.mcgill.ca/~grober4//ROBERTS/PUBLICATIONS/BOOK_CHAPTERS/DFT_97.pdf

[11] G.W. Roberts, "*Improving The Testability of Mixed-Signal Integrated Circuits*", Proc. of the IEEE 1997 Custom Integrated Circuits Conference, pp. 214-221, May 1997.

[12] S.R. Das, etc., "*Testing Analog and Mixed-Signal Circuits With Built-In Hardware-A New Approach*", IEEE Trans. on Instrumentation and Measurement, Vol. 56, No. 3, pp. 840-855, Jun, 2007.

[13] S. Mir, etc., "*Built-in Self-test Approaches for Analogue and Mixed-Signal Integrated Circuits*", Proc. 38th Midwest Symp. on Circuit and System, Vol. 2, pp. 1145-1150, Aug. 1995.

[14] J. Savir and Z. Guo, "*Test Limitations of Parametric Faults in Analog Circuits*", IEEE Trans. on Instrumentation and Measurement, Vol. 52, No. 5, pp. 1444-1154, Oct. 2005.

[15] B. Vinnakota, Analog and Mixed-Signal Test, Prentice Hall PTR, 1998.

[16] M. Burns and G.W. Roberts, An Introduction to Mixed-Signal IC Test and Measurement, Oxford University Press, 2001.

[17] P.P. Fasang, "*Analog/Digital ASIC Design for Testability*", IEEE Trans. on Industrial Electronics, Vol. 36, No. 2, pp. 219-226, May 1989.

[18] L.S. Milor, *"A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing*", IEEE Trans. on Circuits and System II: Analog and Digital Signal Processing, Vol. 45, No, 10, pp. 1389-1407, Oct. 1998.

[19] G.W. Roberts, "*Metrics, Techniques and Recent Developments in Mixed-signal Testing*", IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 514-521, Nov. 1996.

[20] R.J. Baker, CMOS Circuit Design, Layout, and Simulation, 3rd Ed. Wiley-IEEE Press, 2010.

[21] A. Chatterjee and N. Nagi, "*Design for Testability and Built-In Self-Test of Mixed-Signal Circuits: A Tutorial*", Proc. of the 10th Intl. Conf. on VLSI Designo, pp. 388-392, Jan. 1997.

[22] M. Soma, "*A Design-For-Test Methodology for Active analog filters*", Proc. of Intl. Test Conf., pp. 183-192, Sept. 1990.

[23] K. Arabi and B. Kaminska, "*Oscillation Built-In Self Test (OBIST) Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits*", Proc. of Intl. Test Conf., pp. 786-795, Nov. 1997.

[24] K. Arabi and B. Kaminska, "*Design for Testability of Embedded Integrated Operational Amplifiers*", IEEE J. of Solid-State Circuits, Vol. 33, No. 4, pp. 573-581, Apr. 1998.

[25] J. Font, etc., "*Oscillation-Test Technique for CMOS Operational Amplifiers by Monitoring Supply Current*", Analog Integrated Circuits and Signal processing, Vol. 33, No. 2, pp. 213-224, 2002.

[26] IEEE-SA Standards Board, IEEE Standard for a Mixed-Signal Test Bus, 2000.

[27] W. SAN-UM and M. Tachibana, "*A Fault Signature Characterization Based Analog Circuit Testing Scheme and the Extension of IEEE 1149.4 Standard*", IEICE Trans. Inf. & Syst., Vol. E93-D, No. 1, pp. 33-42, Jan. 2010.

[28] B. Dufor and G.W. Roberts, "*On-Chip Analog Signal Generation for Mixed-Signal Built-In Self-Test*", IEEE J. of Solid-State Circuits, Vol. 34, No. 3, pp. 318-330, Mar. 1999.

[29] M.J. Barragan, D. Vazquez and A. Rueda, "*Analog Sinewave Signal Generators for Mixed-Signal Built-in Test Applications*", J. of Electron Test, Vol.27, No.3, pp.305-320, Jun. 2011.

[30] B. Provost and E. Sanchez-Sinencio, "*On-Chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test*", IEEE Trans. of Solid-State circuits, Vol. 38, No.2, Feb.2003.

[31] W.M. Lindermeir, "*Design of Robust Test Criteria in Analog Testing*", Porc. of IEEE/ACM Intl. Conf. on Computer-Aided Design, pp. 604-611, Nov. 1996.

[32] A. Walke, W.E. Alexander and P.k. Lala, "*Fault Diagnosis in Analog Circuits Using Element Modulation*", IEEE J. of Design and Test, Vol. 9, No. 1, pp 19-29, Jan. 1992.

[33] P.N. Variyam and A. Jhatterjee, "*Specification-Driven Test Generation for Analog Circuits*", IEEE Trans. on Computer-Aided Design of Integrated Circuit and Systems, Vol. 19, No. 10, pp. 1189-1201, Oct. 2000.

[34] J.P. Shen, W. Maly and F.J. Ferguson, "*Inductive Fault Analysis of MOS Integrated Circuits*", IEEE Design & Test of Computers, Vol. 2, No. 6, pp. 13-26, Dec. 1985.

[35] F.C.M. Kuijstermans, M. Sachdev and A.P. Thijssen, "*Defect-Oriented Test Methodology for Complex Mixed-Signal Circuits*", Proc. IEEE Symp. (ED&TC 1995), pp.18-23, 1995.

[36] S. Bhunia, A.R. Ychowdhury and K. Roy, "*Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current*", J. of Electronics Testing: Theory and Applications, Vol. 21, pp. 147-159, 2005.

[37] A. Meixner and W. Maly, "*Fault Modeling for the Testing of Mixed Integrated Circuits*", Proc. of Intl. Test Conf., pp. 564-572, Oct. 1991.

[38] M. Sachdev, "*A Realistic Defect Oriented Testability Methodology for Analog Circuits"*, J. of Electronic Testing, Vol. 6, No. 3, pp. 265-276, 1995.

[39] J. Segura, C. Benito, A. Rubio and C.F. Hawkins, "*A Detailed Analysis and Electrical Modeling of Gate Oxide Shorts in MOS transistors* *", J. of Electronics Testing: Theory and Applications, Vol. 8, No. 3, pp. 229-239, 1996.

[40] R. Rajsuman, "*Iddq Testing for CMOS VLSI"*, Proc. of the IEEE, Vol. 88, No. 44, pp.544-566 Apr. 2000.

[41] L. Milor and V. Visvanthan, "*Detection of Catastrophic Faults in Analog Integrated Circuits*", IEEE Trans. on Computer-Aided Design, Vol. 8, No. 2, pp.114-130, Feb. 1989.

[42] H. Walker and S.W. Director, "*VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits*", IEEE Trans. on Computer-Aided Design, Vol. CAD-5, No. 4, pp.514-556, Oct. 1986.

[43] H.C. Liu and M. Soma, "*Fault Diagnosis for AnalogIntegrated Circuits based on the Circuit Layout*", Proc. of Pacific Rim Intl. Symp. on Fault Tolerant System, pp.134-139, Sep. 1991.

[44] H. Xue, C. Di and J.A.G. Jess, "*A Net-Oriented Method for Realistic Faults Analysis*", Proc. Of IEEE/ACM Intl. Conf. on Computer-Aided Design, pp.78-83, Nov. 1993.

[45] N. Nagi and J.A. Abraham, "*Hierarchical Fault Modeling for Analog and Mixed-Signal Circuits*", VLSI Test Symp. on Design, Test and Application: ASICs and System0on-a-Chip, pp. 96-101, Apr. 1992.

[46] C.J.R Shi and N.J. Godambe, "*Behavioral Fault Modeling and Simulation of Phase-Locked Loops Using a VHDL-A Like Language*", Proc. of ASIC Conf. & Exhibit, pp. 245-250, Sep. 1996.

[47] T. Olbrich. etc., "*Defect-Oriented VS Schematic-Level Based Faults Simulation for Mixed-Signal ICs*", Intl. Test Conf., pp. 511-520, Oct. 1996.

[48] M.A. AbdEi-Halim and H.H, Amer, "Schematic-Based Fault Dictionary : A Case Study", Intl. Design and Test Workshop, pp. 257-260, Dec. 2007.

[49] M.J. Ohletz, "*Realistic Faults Mapping Scheme for the Fault Simulation of Integrated Analogue CMOS Circuits*", Intl. Test Conf., pp. 776-785, Oct. 1996.

[50] M. Slamni and B. Kaminska, "*Testing Analog Circuits by Sensitivity Computation*", European Conf. on Design Automation, Brussels, pp.832-537, Mar. 1992.

[51] N.B. Hamida and B. Kaminska, "*Analog Circuit Testing Based on Sensitivity Computation and New Circuit Modeling*", Intl. Test Conf., pp. 652-661, Oct. 1993.

[52] K. Saab, N. Ben-Hamida and B. Kaminska, "*Parametric Fault Simulation and Test Vector Generation*", Proc. of European Conf. & Exh. of Design, Automation and Test, pp. 650-656, 2000.

[53] W. San-Um and, M. Tachibana, "*A Compact On-Chip Testing Scheme for Analog-Mixed Signal Systems Using Two-Step AC and DC Faults Signature Characterizations*", Proc. of Synthesis And System Integration of Mixed Information Technologies (SASIMI'2009), pp.428–433, 2009.

[54] U. Kac and F. Novak, "*Oscillation Test Scheme of SC Biquad Filters based on Internal Reconfiguration*", J. of Electron Test, Vol.23, No.6, pp.485-495, Dec. 2007.

[55] R. Kondagunturi, E. Bradley K. Maggard and C. Stroud, "*Benchmark Circuit for Analog and Mixed-Signal Testing*", Proc. of IEEE Sotheastcon '99, pp.217-220, Mar. 1999.

[56] J. Park etc., "*Defect-Based Analog Fault Coverage Analysis using Mixed-Mode Fault Simulation*", Proc. of IEEE IMS3TW '09, pp.1-6, Jun. 2009.

[57] S. Natarajan, "*A Simple Method to Estimated Gain-Bandwidth Product and the Second Pole of the Operational Amplifiers*", IEEE Trans. on Instrumentation and Measurement, Vol. 40, No. 1, pp. 42-43, Feb. 1991.

[58] K. Yavuz and Z. Mark, "*Process Variation Independent Built-In Current Sensor for Analogue Built-In Self-Test*", IEEE Intl. Symp. on Circuit and System, Vol. 4, pp. 398-401, May 2001.

[59] K. Ramamurthy, J.G. Kenney and G. Rangan, "*On-Chip Tests for Gain Bandwidth Product and Slew Rate*", IEEE Intl. Symp. on Circuit and System, Vol. 2, pp. 1341-1344, May 1993.

[60] J. Font-Tossello, etc., "*A Digital BIST for Opamps Embedded in Mixed-Signal Circuits by Analysing the Transient Response*", IEEE Intl. Caracas Conf. on Devices, Circuits and Systems, pp. 1012-1-1012-5, Apr. 2002.

[61] M. Soma, "*Fault Coverage of DC Parametric Tests for Embedded Analog Amplifiers*", Intl. Test Conf., pp. 566-573, Oct. 1993.

[62] S.J. Chang, C.L. Lee and J.E. Chen, "*Functional Test Pattern Generation for CMOS Operational Amplifier*", IEEE VLSI Test Symp. , pp. 267-272, May 1997.

[63] J.V. Callvano, V.C. Alves and M.S. Lubaszewski, "Testing a PWM Circuit Using Functional Fault Models and Compact Test Vectors for Operational Amplifiers", Asian Test Symp., pp. 96-100, Dec. 2000.

[64] J.V. Calvano, etc., "*Fault Models and Compact Test Vectors for MOS OpAmp Circuits*", Proc. of Symp. on Integrated Circuits and Systems Design, pp. 289-294, Sep. 2002.

[65] M. Sachdev, "*Catastrophic Defects Oriented Testability Analysis of A Class AB Amplifier*", Intl. Workshop on Defect and Fault Tolerance in VLSI System, pp. 319-326, Oct. 1993.

[66] K. Arabi and B. Kaminska, "*Oscillation-Test Strategy for Analog and Mixed-Signal Integrated Circuits*", Proc. of VLSI Test Symp., pp. 476-482, May 1996.

[67] K. Arabi and B. Kaminska, "*Design for Testability of Embedded Integrated Operational Amplifiers*," IEEE J. of Solid-State Circuits, Vol.33, pp. 573 - 581, Apr.1998.

[68] J. Font, etc., "*Oscillation-Test Technique for CMOS Operational Amplifiers by Monitoring the Supply Current*", Proc. of Analog Integrated Circuits and Signal, vol.33, pp. 213-224, April 2002.

[69] J. Font, etc., "*A BICS for CMOS OpAmps by Monitoring the Supply Current Peak*", J. of Electronic Testing, Vol. 19, No. 5, pp. 596-603, 2003.

[70] G.H. Sanchez, etc., Oscillation-Based Test in Mixed-Signal Circuits, Springer, 2006.

[71] M. Roca and A. Rubio, "*Selftesting CMOS Operational Amplifier*", Electronics Letters, Vol. 28, pp. 1452 - 1454, Jul. 1992.

[72] J. Velasco-Medina and M. Nicolaidis, "*Current-Based Testing for Analog and Mixed-Signal Circuits*", Computer Design: VLSI in Computer and Processors, pp.576-581, Oct. 1998.

[73] J. Velasco-Medina, I. Rayane and M. Nicolaidis, "*AC/DC BIST for Testing Analog Circuits*", IEEE Intl. ASIC/SOC Conf., pp. 223-227, Sep. 1999.

[74] J. Velasco-Medina, I. Nicolaidis and M. Lubaszewski , "*An Approach to the On-Line Testing of Operational Amplifiers*", Proc. of Asian Test Symp., pp. 290-295, Dec. 1998.

[75] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd ed., Vol. 2. Oxford: New York, 2002, pp.269-309, 353,768-775.

[76] P.R. Gray and R.G. Meyer, "*MOS Operational Amplifier Design-A Tutorial Overview*", IEEE J. of Solid-State Circuits, Vol. 17, No. 6, pp. 969-982, Dec. 1982.

[77] P.R. Gray, P.R. Hurt, S.H. Lewis and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 4th Ed., Vol. 2. Wilery: New York, 2002, pp428-pp431.

[78] W. Kester, Data Conversion Handbook, Analog Devices, inc, 2005.

[79] F. Maloberti, Data Converters, Springer, pp.413-432, 2007.

[80] B. Razavi, Principles of Data Conversion System Design, Wiley , Nov. 1994.

[81] W. Kester and D. Sheingold, Chapter 5 Testing Data Converters in Analog-Digital Conversion, http://www.analog.com/library/analogDialogue/archives/39-06/Chapter%205%20Testing%20Converters%20F.pdf

[82] J. Naylor, "*Testing Digital/Analog and Analog/Digital Converters*", IEEE Trans. on Circuits and Systems, Vol. 25, No. 7, pp. 526-538, Jul. 1978.

[83] B. Vargha, j. Schoukens and Y. Rolain, "*Static Nonlinearity Testing of Digital-to-Analog*

Converters", IEEE Trans. on Instrumentation and Measurement, Vol. 50, No. 5, pp. 1283-1288, Oct. 2001.

[84] M. DArco, A. Liccardo and M. Vadursi, "*Test Equipment of DAC's Performance Assessment: Design and Characterization*", IEEE Trans. on Instrument and Measurement, Vol. 59, No. 5, pp. 1027-1034, May 2010.

[85] IEEE Std., "*IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters*", 2001.

[86] K. Arabi, B. Kaminska and M. Sawan, "*On Chip Testing Data Converters Using Static Parameters*", IEEE Trans. on Very Large Scale Integration Systems, Vol.6, pp.409-419, 1998.

[87] J.L. Huang, C.K. Ong, and K.T. Cheng, "*A BIST Scheme for On-Chip ADC and DAC Testing*", Proc. of IEEE Symp. on Design, Automation and Test in Europe Conf. and Exhibition, pp.216-220, 2000.

[88] J. Wei and V.D. Agrawal, *"Built-in Self-Calibration of On-chip DAC and ADC"*, Proc. of Test Conf., pp.1-10, 2008.

[89] S.K. Sunter and N. Nagi, "*A Simplified Polynomial-Fitting Algorithm for DAC and ADC BIST*", Proc. of Intl. Test Conf., pp. 389-395, Nov. 1997.

[90] E. Teraoka, etc., "*A Built-In Self-Test for ADC and DAC in a Single-Chip Speech CODEC*", Proc. of IEEE Symp. Test Conf., pp.791-796, 1993.

[91] S.J. Chang, C.L. Lee and J.E. Chen, "*BIST Scheme for DAC Testing*", Electronics Letters, Vol. 38, No. 15, pp. 776-777, Jul. 2002.

[92] T. Olbrich, etc., "*Design-for-test (DfT) Study on a Current Mode DAC"*, Proc. of Circuits, Devices and Systems, Vol.143, No. 6, pp. 374-379, Dec. 1996.

[93] J. Ramesh, M. Srinivasulu and K. Gunavathi, "*A Novel On Chip Circuit for Fault Detection in Digital to Analog Converters*", Proc. Intl. Conf, Control, Automation, Communication and Enery Conservaion, Vol.3, pp.1–8, 2009.

[94] M.J.Barragan, D. Vazquez and A. Rueda, "*Analog Sinewave Signal Generators for Mixed-Signal Built-in Test Applications*", J. of Electron Test, Vol.27, No.3, pp.305-320, Jun. 2011.

[95] B. Provost and E. Sanchez-Sinencio, "*On-Chip Ramp Generators for Mixed-Signal BIST and ADC Self-Test*", IEEE Trans. of Solid-State circuits, Vol. 38, No. 2, Feb.2003.

[96] R.J. Van De Plassche, "*Dynamic Element Matching for High-Accuracy Monolithic D/A Converters*", IEEE J. of Solid-State Circuits, Vol. 11, No. 6, pp. 795-800, Dec. 1976.

[97] B. Vargha and I. Zoltan, "*Calibration Algorithm for Current-Output R-2R Ladder*", IEEE Trans. on Instrumentation and Measurement, Vol. 50, No. 5, pp. 1216-1220, Oct. 2001.

[98] L. Yu and R. Geiger, "*Unit Resistor Characterization for Matching-Critical Circuit Design*", Proc. of IEEE Int. Symp. on Circuits and Systems, pp. 3457-3461, May 2006.

[99] Y. Lin and R. Geiger, "*Area Allocation strategies for Enhancing Yield of R-2R Ladder*", Proc. of

Analog Integrated Circuits and Signal, Vol. 37, No. 2, pp. 123-132, Nov. 2003.

[100] M.P. Kennedy, "*On the Robustness of R-2R Ladder DAC's*", IEEE Trans. on Circuits and System I: Fundamental Theory and Applications, Vol. 47, No. 2, Feb. 2000.

[101] G. Wegmann, E.A. Vittoz and F. Rahali, "*Charge Injection in Analog MOS Switches*", IEEE J. of Solid-State Circuits, Vol. 22, No. 6, pp. 1091-1097, Dec. 1987.

[102] R.J. Baker, CMOS Circuit Design, Layout, and Simulation, 2nd Ed., Wiley, Nov. 2004.

[103] B.J. Shen and C.M. Hu, "*Switch-Induced Error Voltage on a Switched Capacitor*", IEEE J. of Solid-State Circuits, Vol. sc-19, No. 19, pp. 519-525, Aug. 1994.

[104] M.J Chen, etc., "*Weak Inversion Charge Injection in Analog MOS Switches*", IEEE J. of Solid-State Circuits, Vol. 30, No. 5, pp. 604-606, May 1995.

[105] W. Xu and E.G. Friedman, "*Clock Feedthrough in CMOS Analog Transmission Gate Switches*", IEEE Intl. ASIC/SOC Conf., pp. 181-185, Sept. 2002.

[106] D. Johns and K. Martin, Analog Integrated Circuit Design, Wiley, Nov. 1996.

[107] C. Eichenberger and W. Guggenbuhl, "*Charge Injection of Analogue CMOS Switches*", IEE Proc.-G, Vol. 138, No. 2, 155-159, Apr. 1991.

[108] J.H. Shieh, M. Patil and B.J Sheu, "*Measurement and Analysis of Charge Injection in MOS Analog Switches*", IEEE J. of Solid-State Circuits, Vol. 22, No. 2, pp. 227-281, Apr. 1987.

[109] B. Sheu, J.H Shieh and M. Patil, "*Modeling Charge Injection in MOS Analog Switches*", IEEE Trans. on Circuits and Systems, Vol. 34, No. 2, Feb. 1987.

[110] R. van de Plassche, CMOS Integrated ADC and DAC, 2nd Ed. Kluwer academic publishers, 2003.

[111] C. Eichenberger and W. Guggenbuhl, "*On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques*", IEEE Trans. on Circuits and Systems, Vol. 37, No. 2, pp. 256-264, Feb. 1990.

[112] H. Kobayashi, etc., "*High-Speed CMOS Track/Hold Circuit Design*", Proc. of Analog Integrated Circuits and Signal, Vol. 27, No. 1-2, pp. 161-170, 2001.

[113] T.S. Fiez, etc., "*Signal-Dependent Clock-Feedthrough Cancellation in Switched-Current Circuits*", Proc. of Intl. Conf. on Circuits and Systems, Vol. 2, pp. 785-788, Jun. 1991.

[114] G. Palmisano and G. Palumbo, "*High Performance CMOS Current Comparator Design*", IEEE Trans. on Circuits and System II: Analog and Digital Signal Processing, Vol. 43, No. 12, pp. 785-790, Dec. 1996.

[115] E.A. Vittoz, "*The Design of High-Performance Analog Circuits on Digital CMOS Chips*", IEEE J. of Solid-State Circuits, Vol. 20, No. 3, pp. 657-665, Jun. 1985.

[116] R.E. Suarez, P.R. Gray and D.A. Hodges, "*All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part II*", IEEE J. of Solid-State Circuits, Vol. 10, No. 6, pp. 379-385, Dec. 1975.

[117] S.K. Tewksbury, etc., "*Terminology Related to the Performance of S/H, A/D, and D/A Circuits*", IEEE Trans. on Circuits and Systems, Vol. CAS-25, No. 7, pp. 419-426, Jul. 1987.

[118] B. Razavi, "*Design of Sample-and-Hold Amplifiers for High-Speed Low-Voltage A/D Converters*", Proc. of IEEE Custom Integrated Circuits Conf., pp. 59-66, May 1997.

[119] W. Xu and E.G. Friedman, "*A CMOS Miller Hold Capacitance Sample-and-Hold Circuit to Reduce Charge Sharing Effect and Clock Feedthrough*", IEEE Intl. ASIC/SOC Conf., pp. 92-96, Sept. 2002.

[120] P.J. Lim and B.A. Wooley, "*A High-Speed Sample-and-Hold Techniques Using a Miller Hold Capacitance*", IEEE J. of Solid-State Circuits, Vol. 26, No. 4, pp. 643-651, Apr. 1991.

[121] M. Waltari and K. Halonen, "*A 220-MSample/s CMOS Sample-and-Hold Circuit Using Double-Sampling*", Proc. of Analog Integrated Circuits and Signal, Vol. 18, No. 1, 1999.

[122] T.S. Lee and C.C. Lu, "*A 1.5-V 50-MHz Pseudodifferential CMOS Sample-and-Hold Circuit with Low Hold Pedestal*", IEEE Trans. on Circuits and Systems I: Regular papers, Vol. 52, No. 9, pp. 1752-1757, Sept. 2005.

[123] G. Nicollini, P. Confalonieri and D. Senderowicz, "*A Fully Differential Sample-and-Hold Circuit for High-Speed Applications*", IEEE J. of Solid-State Circuits, Vol. 24, No. 5, Oct. 1989.

[124] S. Haddadian and R. Hedayati, "*A Unity Gain Fully-Differential 10bit and 40MSps Sample-And-Hold Amplifier in 0.18μm CMOS*", World Academy of Science, Engineering and Technology, pp. 467-472, 2008.

[125] T.S. Lee, C.C. Lu and C.C. Ho, "*A 330MHz 11Bit 26.4mW CMOS Low-Hold-pedestal Fully Differential Track-and Hold Circuit*", IEEE Int. Symp. on VLSI Design, Automation and Test, pp. 144-147, Apr. 2008.

[126] F. Centurelli, etc., "*Design Solution for Sample-and-Hold Circuits in CMOS Nanometer Technologies*", IEEE Trans. on Circuits and Systems II: Express Briefs, Vol. 56, No. 6, pp. 459-463, Jun. 2009.

[127] Y.I. Park, etc., "*A Low 10 bit,80 MS/s CMOS Pipelined ADC at 1.8 V Power Supply*", IEEE Intl. Symp. on Circuits and Systems, Vol. 1, pp. 580-583, May 2001.

[128] M. Mousazadeh, K. Hadidi and A. Khoei, "*A Highly Linear Open-Loop High-Speed CMOS Sample-and-Hold*", IEEE Asia Pacific Conf. on Circuits and Systems, pp. 228-231, Dec. 2010.

[129] K. Watanabe and S. Ogawa, "*Clock-Feedthrough Compensation Sample/Hold Circuits*", Electronics Letters, Vol. 24, No. 19, pp. 1226-1228, Sep. 1988.

[130] L. Dai and R. Harjani, "*CMOS Switched-Op-Amp-Based Sample-and-Hold Circuit*", IEEE J. of Solid-State Circuits, Vol. 35, No. 1, pp. 109-113, Jan. 2000.

[131] M. Rashtian, O. Hashemipour and K. Navi, "*A Voltage-Mode Sample and Hold Circuit Based on the Switched Op-Amp Techniques*", Would Applied Sciences J., Vol. 4, No. 2, pp. 266-269, 2008

[132] H.K. Yang and E.I. El-Masry, "*Clock Feedthrough Analysis and Cancellation in Current Sample/Hold Circuits*", IEE Proc. of Circuits, Devices and Systems, Vol. 141, No. 6, pp.

510-516, Dec. 1994.

[133] C.Y. Wu, C.C. Chen and J.J. Cho, "*Precise CMOS Current Sample/Hold Circuits Using Differential Clock Feedthrough Attenuation Techniques*", IEEE J. of Solid-State Circuits, Vol. 30, No. 1, Jan. 1995.

[134] Y. Sugimoto, "*A 1.5-V Current-Mode CMOS Sample-and-Hold IC with 57-dB S/N at 20MS/s and 54-dB S/N at 30 MS/s*", IEEE J. of Solid-State Circuits, Vol. 36, No. 4, pp. 696-700, Apr. 2001.

[135] C. Sawigun and W.A. Serdijn, "*Analysis and Design of a Low-Voltage, Low-Power, High-Precision, Class-AB Current-Mode Subthreshold CMOS Sample and Hold Circuit*". IEEE Trans. on Circuits and Systems I: Regular Papers, Vol. 58, No. 7, pp. 1615-1626, Jul. 2011.

[136] M. Stofka, "*Circuit Lets You Test Sample-and-Hold Amplifiers*", http://www.edn.com/design/analog/4312202/Circuit-lets-you-test-sample-and-hold-amplifiers

[137] M. Soma, "*Fault modeling and test generation for sample-and-hold circuits*", Proc. of IEEE Intl. Symp. on Circuits and Systems, Singapore, vol. 4, pp. 2072-2075, Jun. 1991.

[138] N. Axelos, etc., "*Built-In-Self-Test of Analogue Circuits using Optimized Fault Sets and Transient Response Testing*", Proc. of the 8th IEEE Intl. On-Line Testing Workshop, pp.135-139, 2002.

[139] D. Hsiu-Chun Chiang, R. Schaumann and W.R. Daasch, "*Test Board Design and Measurement Techniques for High-Frequency Fully-Differential CMOS OTAs*", Proc. of IEEE Intl. ASIC Conf. and Exhibit, Portland, OR, pp. 321-326, Sep. 1997.

[140] V. Kolarik, M. Lubaszewski and B. Courtois, "*Towards Self-Checking Mixed-Signal Integrated Circuit*", European Solid-State Circuits Conf., Vol. 1, pp. 202-205, Sep. 1993.

[141] B. Vinnakota and R. Harjani, "*The Design of Analog Self-Checking Circuits*", Proc. of Intl. Conf. on VLSI Design, pp. 67-70, Jan. 1994.

[142] M. Lubaszewski, etc., "*Mixed-Signal Circuits and Boards for High Safety Applications*", Proc. of European Design and Test Conf., pp. 34-39, Mar 1995.

[143] V. Kolarik, M. Lubaszewski and B. Courtois, "*Designing Self-Exercising Analog Checkers*", Proc. of IEEE VLSI Test Symp., pp. 252-257, Apr. 1994.

[144] R. Harjani and B. Vinnakota, "*Analog Circuit Observer Blocks*", IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 44, No. 3, Mar 1997.

[145] M. Lubaszewski, etc., "*Design of Self-Checking Fully Differential Circuits and Boards*", IEEE Trans. on VLSI Systems, Vol. 8, No. 2, pp. 113-128, Apr. 2000.

[146] S. Mir, M. Lubaszewski and B. Courtois, "*Unified Built-In Self-Test for Fully Differential Analog Circuits*", J. of Electronic Testing, Vol. 9, No. 1-2, pp. 135-151, 1996.

[147] S. Mir, etc., "*Built-in Self-Test and Fault diagnosis of Fully Differential Analogue Circuits*", Proc. of IEEE/ACM Intl. Conf. on Computer-Aided Design, pp. 486-490, 1994.

[148] M. Banu, J.M. Khoury and Y. Tsividis, "*Fully Differential Operational Amplifiers with*

Accurate Output Balancing", IEEE J. of Solid-State Circuits, Vol. 23, No. 6, Dec. 1988.

[149] P.M. VanPeteghem and J.F. Duque-Carrillo, "*A General Description of Common-Mode Feedback in Fully-Differential Amplifiers*", IEEE Intl. Symp. on Circuits and Systems, Vol. 4, pp. 312-320, May 1990.

[150] J.F. Duque-Carrillo, "*Control of the Common-Mode Component in CMOS Continuous-Time Fully Differential Signal Processing*", Proc. of Analog Integrated Circuits and Signal, Vol. 4. No. 2, pp. 131-140, 1993.

List of Publications

Journals

1. Jun Yuan and Masayoshi Tachibana, "*A common-mode BIST technique for fully-differential sample-and-hold circuits*," IEICE Electronics Express, Vol. 9, No. 13, pp.1128-1134, Jun. 2012.

2. Jun Yuan and Masayoshi Tachibana, "A *Resistance-Matching based BIST Technique for Current-Mode R-2R Digital-to-Analog Converter*", IEICE Trans. on Fundamentals of Electronics, Communications and Computer Sciences (Submitted).

Conferences

1. Jun Yuan and Masayoshi Tachibana, "*A BIST Scheme based on Resistance Match for Current-Mode R-2R Ladder Digital-to-Analog Converter*", 3rd International Conference on Computer Research and Development (ICCRD 2011), ShangHai, China, Mar.2011.

2. Jun Yuan and Masayoshi Tachibana, "A BIST Scheme for Operational Amplifier by Checking the Stable Output of Transient Response", 20th European Conference on Circuit Theory and Design, ECCTD 2011, Linkoping, Sweden, Aug. 29-31, 2011.

3. Jun Yuan and Masayoshi Tachibana, "A Two-Step BIST Scheme for Operational Amplifier," Workshop on Synthesis and System Integration of Mixed Information technologies (SASIMI-2012), Beppu, Japan, Mar.2012