論 文 内 容 の 要 旨

Recently, oxide thin-film transistors (TFTs) have attracted considerable attention for use in next generation large-area flat panel displays (FPDs), due to their superior electrical properties, in particular high mobility, steep subthreshold swing (S), and good electrical stability. Since these electrical properties are highly dependent on the density of localized states (DOS), there have been many studies of the effects of DOS in oxide semiconductors on the electrical properties of the TFTs. My research mainly focuses on evaluating TFT performance and reliability, analyzing degradation mechanisms by using 2D device simulation, purposing novel structure and novel method to develop high performance and high stability oxide TFTs for future industrial applications.

In chapter 1, a brief overview of the TFTs history is interpreted at the beginning. Amorphous oxide TFTs are expected to be applied in next generation flat panel displays as compared with conventional a-Si:H and poly-Si TFTs. A two-dimension (2D) device simulation is an effective method to analyze the degradation mechanism and optimize the fabrication process of oxide TFTs. On the other hand, bias instability at high temperature and negative bias illumination stress (NBIS) remain critical issues. Further improvement of bias stability at high temperature and NBIS are required for oxide TFTs. In additional, a self-aligned structure is an essential for oxide TFTs to achieve system-on-panel and high-resolution LCD and OLED displays to solve parasitic capacitance drawback of CGD and CGS in bottom-gate structure.

In chapter 2, the basic knowledge of ATLAS was introduced at the beginning; then, the properties of fluorinated silicon nitride (SiNx:F)/IGZO stacked layers were analyzed. We purposed a novel F doping conception, introduced an etch-stopper layer between IGZO channel and SiNx:F passivation layer, the fabrication processes of bottom-gate with etch-stopper structure oxide TFTs were described. A novel method for making thermally stable source and drain region through selective deposition of SiNx:F) on top of the IGZO film. The fabrication processes of

self-aligned bottom-gate oxide TFTs were described in detail. Some basic knowledge of evaluation oxide TFTs was also mentioned.

In chapter 3, the electrical properties of bottom-gate amorphous InSnZnO (a-ITZO) thin-film transistors (TFTs) with different channel thicknesses (T_{ITZO}) were investigated. The difference between the influence of front- and back-channel interface traps on subthreshold swing (S) and turn on voltage (Von) of a-ITZO TFTs was further analyzed using device simulation. It was confirmed that not only front-channel interface traps but also back-channel interface traps are important factors of S and turn on voltage (V_{on}) for thinner channel TFTs in order to achieve high performance oxide TFTs.

Chapter 4 and Chapter 5 discussed fluorine (F) passivation of traps in IGZO for oxide TFTs. Improvements of performance, positive bias and temperature stress (PBTS) and NBIS stability of IGZO TFTs were achieved by SiNx:F passivation as compared with SiOx passivation. The fluorine passivated IGZO TFT has enhanced operation temperature, drastically improved NBIS stability.

Advanced optimization fabrication parameters of F concentration in SiNx:F passivation were further discussed in chapter 6. The electrical property and reliability of IGZO-TFT with high F concentration in SiNx:F passivation were investigated.

In chapter 7, a bottom-gate and self-aligned (BGSA) IGZO TFT, by combining the back-side-exposure technique and IGZO homojunction formed by the direct deposition of SiNx:F on the IGZO, is demonstrated. The electrical characteristics of BGSA IGZO TFT were investigated at different bias stress with or without illumination.

Chapter 8 summarized this thesis work and gave some advices for future work in this field.