Fault diagnosis technology based on transistor behavior analysis for physical analysis

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Abstract

The novel method has been developed to detect accuracy fault elements in transistor level circuit, analyzing the characteristics of circuit operation influenced on leakage fault and being combined with diagnosis software, based on switching level simulation. This method is based on behavior of CMOS transistor to which applied unstable voltage produced by leakage fault. Unsettled logic brings the transistor's operation point to saturation area with multi-impedance value and forms penetration current nets passing through it. Output value on the net is calculated with each element impedance value and miss-logic signal is spread to output terminal. An evaluation of this technology corroborates to be precise method by using the circuit in which embedded arbitrary fault portions.
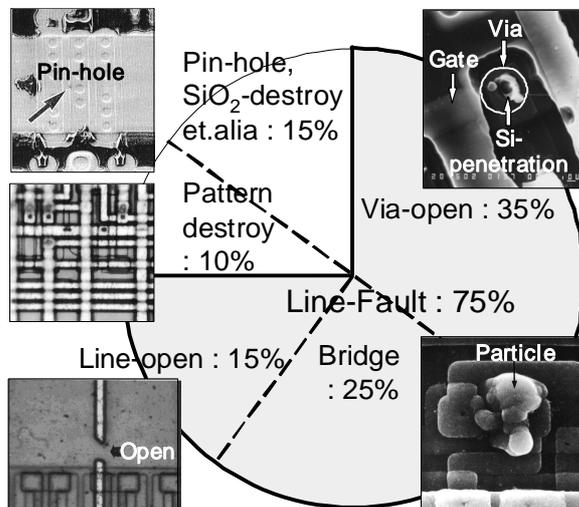
1. Diagnosis concept and flow

Fig.1. Fault mode classification by Liquid Crystal Technology(0.5μm rule's LSI) –reference[2]

Published papers have reported that leakage fault modes, which entail logic fault, occupy over 90% total fault modes[1] and 75% of them cause metal line damage with open and bridge[2] (see Fig. 1). Using the information, a CAD-based fault parts detection technique has been developed to enhance the physical analysis of advanced LSI with scaled down structure and multi-metal layers. The proposed technique progressively narrows doubtful fault portions down by layout

information and logic one. Figure 2 shows a simplified diagnosis flow. The diagnosis flow starting from the fault circuit, which has un-adjusted relation between input and output logic by publicly known technology, takes out possible defect portions in the circuit using layout date. Each portion is embedded on the circuit and fault diagnosis is executed to detect a relation between in and out logic of it. The detected logic is compared with real fault logic and the portion with the logic according with it is determined as highly reliable fault portion. After that, physical analysis of each reliable portion is started.

The paper consists of 5 sections.   First, I describes detection way of possible defect portions by layout the date and then, presents diagnosis method to take out the doubtful fault points by novel method combined with switching level simulation(SLS). In this section, the method concept and diagnosis procedure are introduced. Next, comparison with SPICE (Simulation Program with Integrated Circuit Emphasis) is discussed and application to real fault LSI is explained. Finally, concluded.
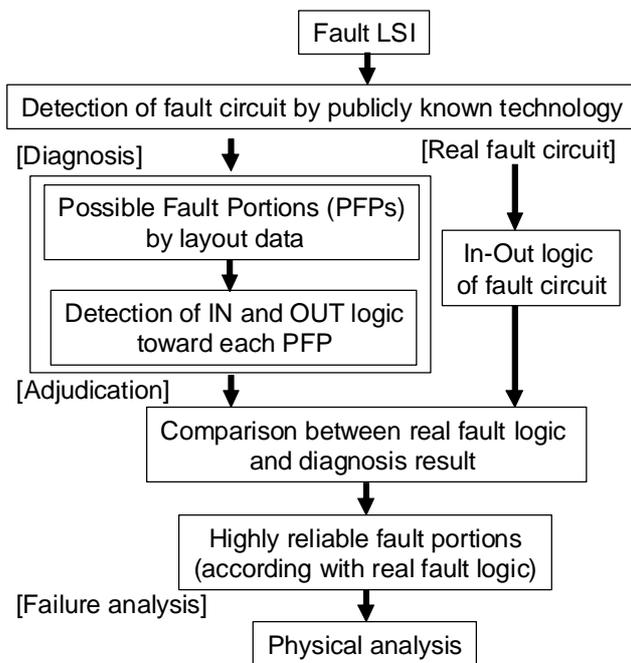
Fault LSI

Detection of fault circuit by publicly known technology

[Diagnosis]   [Real fault circuit]

Possible Fault Portions (PFPs)
by layout data

In-Out logic
of fault circuit

Detection of IN and OUT logic
toward each PFP

[Adjudication]

Comparison between real fault logic
and diagnosis result

Highly reliable fault portions
(according with real fault logic)

[Failure analysis]

Physical analysis

Fig.2. Simplified diagnosis procedure

2. Detection of possible defect portions by layout

Vout |dVout/ dVin|=1 I_{DS} PchTr   NchTr I_{DD} A

A   Non-saturation
                                                          (NchTr)

                                                          Saturation
                                                          (NchTr)

|dVout/ dVin|=1   A

                    Vin V_{DS} Vin
Middle domain   Middle domain

Fig.3. Vin-Vout curve   Fig.4. V_{DS}-I_{DS} curve   Fig.5. V_{IN}-I_{DD} curve

Possible defect portions of open or bridge are extracted by using layout data. Open is focused on via. For the diagnosis, Transistor (Tr) connected to the line with via is detected. Bridge is focused on adjacent line pair and crossed one. They are embedded in the fault circuit, and output logic of circuit is taken out by the diagnosis technology.

3. Detection of doubtful fault portions by Diag.,

In this section, After the method concept is introduced, diagnosis procedure is presented.

3.1   Fundamental concept for novel diagnosis

The Fundamental concep is the method to calculate the voltage of each circuit node by incorporating impedance value detected from operation point of Tr into SLS which treats each Tr as on/off switch. The impedance value is depend upon Tr formation, composed of L (gate length) and W (gate width), and Tr operation point.

3.1.1. Tr formation

For Tr with various structure, one pair Tr forming Inverter circuit is selected as normal Tr (nTr), and standard impedance is set up using L/W value of nTr. Impedance value of various Tr (vTr) is calculated by the ratio of nTr's L/W value to vTr's one.
3.1.2. Tr operation point

First, middle domain(MD) is defined within |dVout/dVin|<1 decided by Vin-Vout curve. Most of line voltages with defect are located in MD, and   operation point of Tr to which the fault voltage is applied does hence lie in saturation area and brings large impedance value with on-state.
The operation point of Tr located in MD is presented by using Vin-Vout, VDS-IDS, and Vin-IDD curve of Inverter circuit (see Fig. 3, Fig. 4, and Fig. 5 respectively). As input voltage is set up to middle level(VDD/2), indicated as point "A" in Fig.

3-5, Tr operation point is settled into saturation domain and it's impedance value turns into several times of non-saturation domain's one, illustrated as dVDS/dIDS line on VDS-IDS curve. Figure 4 denotes that N_channel (Nch) Tr's impedance of point "A" and P_channel (Pch) Tr's one are calculated to five times and three times of non-saturation domain's impedance value. Penetration current (IDD) is generated simultaneously because of on-state of each Tr (see Fig. 5).

For effective diagnosis, additional ratio on operation point is prepared on ahead by LSI electrical characteristics. Figure 6 denotes an additional ratio toward nTr impedance. These detected data are incorporated in switching level simulation and applied to decide the impedance value of each vTr structure.
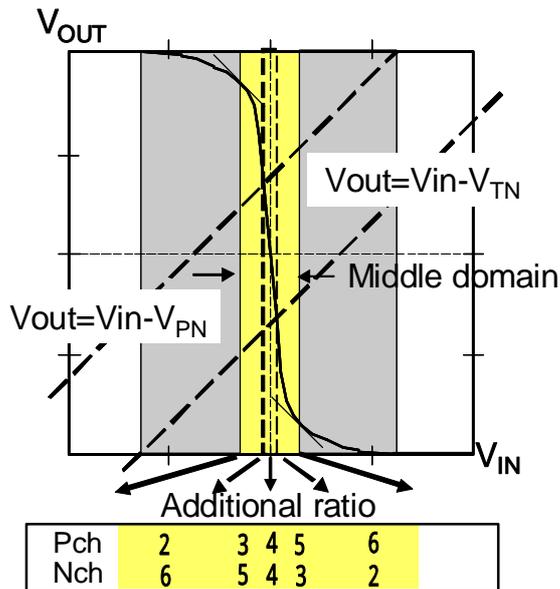
Fig.6. additional ratio toward nTr impedance.

3.2. Diagnosis procedure

Fault diagnosis arising from bridge fault and via-open fault is presented. The diagnosis procedure is the step flow to detect the relation between in and out logic each possible fault circuit.

3.2.1. Bridge fault

For bridge fault, penetration current net connected with bridge is taken out and the net is replaced with impedance net and each node logic value is calculated. A couple of repetition works draw out the optimum value and output logic is calculated. After this, above the same procedure is executed.
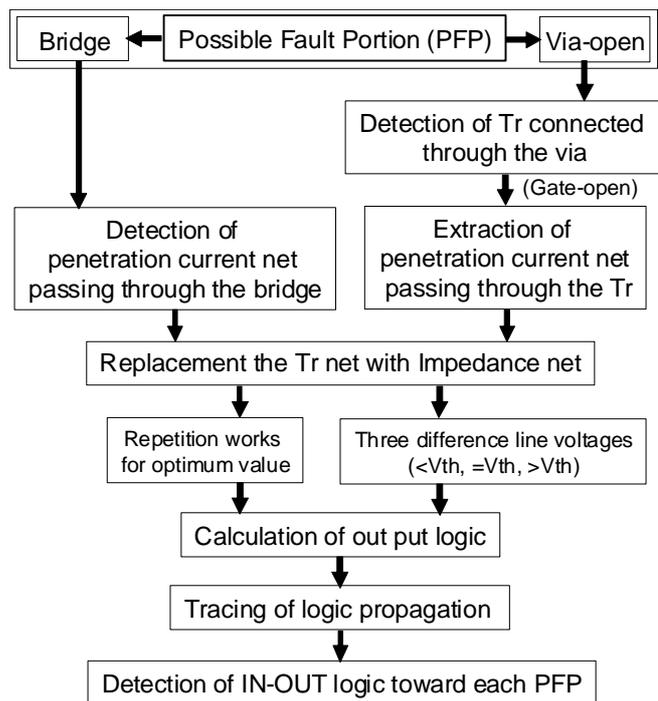
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        ┌─────────┐        ┌──────────────────────────┐        ┌──────────┐
        │ Bridge  │◄───────│ Possible Fault Portion (PFP) │──────►│ Via-open │
        └─────────┘        └──────────────────────────┘        └──────────┘
             │                                                        │
             │                                          ┌─────────────────────────┐
             │                                          │ Detection of Tr connected │
             │                                          │     through the via       │
             │                                          └─────────────────────────┘
             │                                                        │ (Gate-open)
             ▼                                                        ▼
    ┌──────────────────┐                            ┌──────────────────────┐
    │  Detection of    │                            │    Extraction of     │
    │ penetration current net │                     │ penetration current net │
    │ passing through the bridge │                  │ passing through the Tr │
    └──────────────────┘                            └──────────────────────┘
             │                                                  │
             ▼                                                  ▼
    ┌──────────────────────────────────────────────┐
    │  Replacement the Tr net with Impedance net    │
    └──────────────────────────────────────────────┘
             │                                       │
             ▼                                       ▼
    ┌──────────────────┐              ┌──────────────────────────┐
    │ Repetition works │              │ Three difference line voltages │
    │ for optimum value│              │    (<Vth, =Vth, >Vth)    │
    └──────────────────┘              └──────────────────────────┘
             │                                       │
             ▼                                       ▼
    ┌──────────────────────────────┐
    │   Calculation of out put logic │
    └──────────────────────────────┘
                    │
                    ▼
    ┌──────────────────────────────┐
    │ Tracing of logic propagation  │
    └──────────────────────────────┘
                    │
                    ▼
    ┌──────────────────────────────────────┐
    │ Detection of IN-OUT logic toward each PFP │
    └──────────────────────────────────────┘
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Fig.7. diagnosis procedure (except for SD-open)

3.2.2. Via-open fault

There are two different via-open types, One is the type that line with open-via is connected to Tr source or drain (SD) terminal. The other is Tr gate terminal.

SD terminal open type

SD open fault cuts off carrier transfer. The carrier, set up by the logic before cut off state, connected to open place opposite to the fault Tr, and hence, output logic synchronized with input one read out. The relation between input and output logic of fault circuit is finally detected.

Gate terminal open type

Tr connected through the line with open-via is detected and then, penetration current net through the Tr is extracted. For diagnosis, three different voltage states (<Vth, = Vth, > Vth) are arranged on the line because of unsettlement logic state result from gate electrode open. The Tr net is replaced with impedance net and output logic is calculated. After this, Fault logic propagation is traced and the relation between input and output logic of fault circuit is finally detected.

4. Comparison with SPICE simulation

The simple technology was compared with SPICE simulation for detection accuracy and operation times. Experimental items were output voltage with bridge and via-open fault.

4.1. Bridge fault

The former example is simple circuit consist of Inverter (Iv) and 2-INPUT NAND (2inN) shown in figure 8. Bridge is formed between Iv Output and 2inN output. As input logic (1,1) is applied to terminal (In1, In2), normal circuit has ON-state of NchTr:N1,N3 and PchTr:P2, and output value was "H"level. But The bridge fault brings ON-state of NchTr:N1,N2,N3 and PchTr:P2 Output logic is calculated as 0.23VDD ("L"level) (see Eq.1).

$$V_{out} = \{1/(1+n_{N2})+1\}^{-1}/[\{1/(1+n_{N2})+1\}^{-1}+n_{P2}] \cdot V_{DD}$$
$$= 1/(n_{P2}+1) \cdot V_{DD} = 0.23 \cdot V_{DD} \qquad (1)$$

As input logic(0,1) is applied to terminal (In1, In2), normal circuit has ON-state of NchTr:N2,N3 and PchTr:P1, and output value was "L"level. But The fault circuit brings ON-state of NchTr: N2,N3 and PchTr:P1,P2. Output logic is calculated as 0.82VDD ("H"level) (see Eq.2)

$$V_{out} = [n+1\{1/1+1/n^{-1}+(n+1)\}] \cdot V_{DD}$$
$$= \{(n+1)(n+2)\} \cdot V_{DD} = 0.82 \cdot V_{DD} \qquad (2)$$

SPICE indicates that input logic (1,1) leads to 0.22 VDD and input logic (0,1) leads to 0.83 VDD. Both result denoted same output voltage.

(In1, In2)	(0, 1)	(1, 1)
SPICE ○	0.83	0.25
Novel Diag ➤	0.82	0.23

Fig.8. Inverter and 2-INPUT NAND circuit with bridge fault. Diagnosis result of SPICE and Novel technology at (In1,In2)=(0,1)/(1,1)

4.2. Via-open fault

The latter example is 2inN circuit. Open via is formed at input 1 (In1). For additional logic, three voltage state (<Vth, = Vth, > Vth) are arranged on the line because of unsettlement logic state. As INPUT terminal IN2 is applied to logic"1", fault circuit brings ON-state of NchTr: N1, N2 and PchTr: P1 shown in figure 9. Output logic is calculated (see Eq.3).

$$V_{out} = \left[\frac{n_n+1}{\{n_n+1 +n_p\}}\right] V_{DD}$$
$$= \{(n_n+1) / (n_n+n_p+1)\} V_{DD} \qquad 3$$

As In1 are applied < Vth, = Vth and >Vth, Vout are calculated to 0.78VDD, 0.56VDD and 0.33VDD respectively. SPICE results based on the above three voltages indicate 0.82VDD, 0.56VDD, 0.23VDD respectively. These result shows approximately same values.
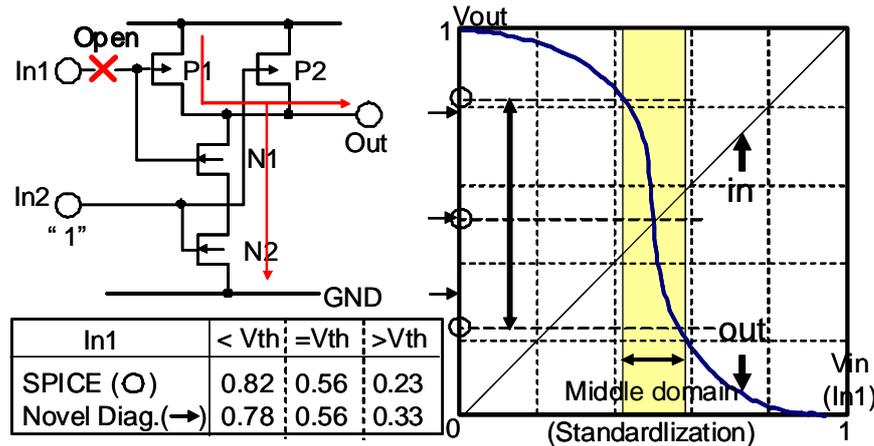

In1	< Vth	=Vth	>Vth
SPICE (○)	0.82	0.56	0.23
Novel Diag.(→)	0.78	0.56	0.33

Fig.9. 2-INPUT NAND circuit with open fault Diagnosis result of SPICE and Novel technology at In1= (<Vth, =Vth,>Vth) and In2="1"

The experimental result indicated that both of them took out the approximate same logic transformation. This method's operation time was 1/100 times of SPICE.

5.   Application of real fault LSI [5]

The technology was applied to real fault LSI, designed by sub-micron rule. Faulty circuit was detected by input-output values from observed responses by tester using cause-effect diagnosis, circuit which was 4 INPUT ANDOR (4inAO) gate circuit with output value, indicate unstable behavior (see Fig.10, 11).
Generally, combinational circuit has simple behavior that an arbitrary input logic set up unique logic to inner logic element. But the detected 4inAO gate indicated unstable output logic. An appearance ratio of miss-logic toward input logic (0011), (1011), (1100) and (1110) denoted 94%, 82%, 0% and 78% respectively (see Table 1).

Table 1 Appearance ratio of miss-logic

INPUT Logic				Appearance ratio
A0	A1	B0	B1	
0	0	1	1	94%
1	0	1	1	82%
1	1	0	0	0%
1	1	1	0	78%

Next, Possible fault portions (PFPs) in 4inAO were detected by layout information, being 11 pairs of adjacent-line, 14 pairs of crossed-line, and 8 peaces of via (see Table 2).

Each PFP was embedded in the 4inAO circuit and executed the fault diagnosis. As a result, via_0025 (element number) was detected as candidate fault portion, bring unsettled fault phenomenon. Via_0025 is the hole pattern to connect power supply line (VDD) and circuit electrode line, which links PchTr_M2 source terminal and PchTr_M3 one (see Fig.10, 11).

Cross section, fabricated by FIB (Focused Ion Beam) and TEM (Transmission Electron Microscope), indicated via_0025 without plug-metal. Figure 12 shows the cross-section images of open-via_0025 and normal via by SEM.

To confirm the diagnosis accuracy, detailed analysis by SPICE was examined. SPICE indicated the unsettled behaviour that input logic (1110) brought two different output value by "1" and "Middle-level". The phenomenon is explained that non-connected current source cuts off carrier transfer (M10: off-state) and the carrier, being set up by the logic before cut off state, is held and acts on the output logic, (link line : VDD-M10-M3-M2) (see Fig. 13).

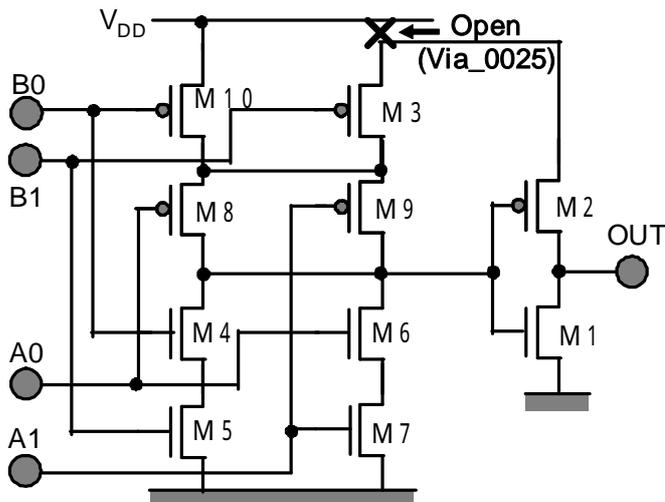Operation time was about 1 minute used by SUN ULTRA-SPARC 1.2GHz.

Fig.10. 4inAO circuit, pointing out via_0025
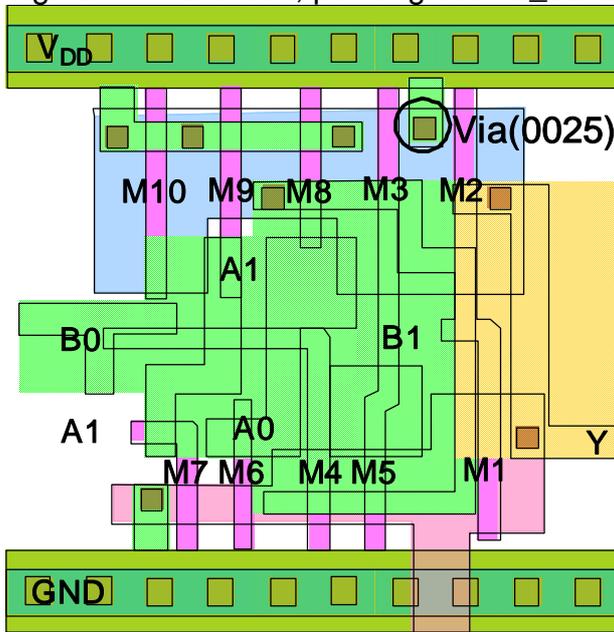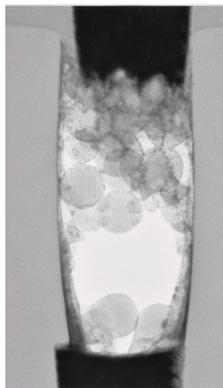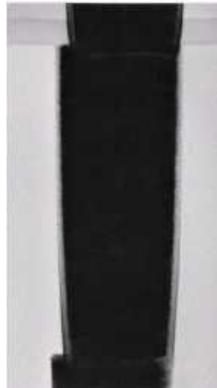

Fig.11. 4inAO layout, pointing out via_0025

Open-via_0025   Normal-via

Fig.12. Cross-section images of open-via_0025 with cave and normal via by SEM.
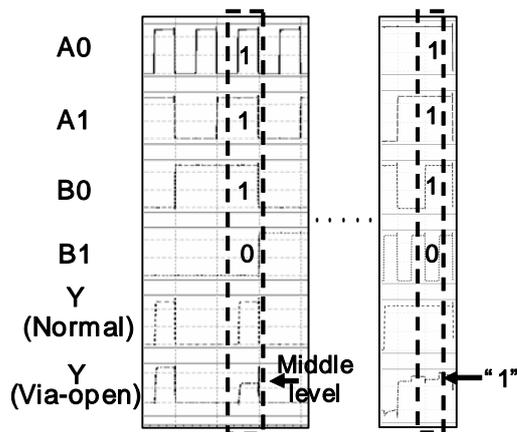
Fig.13. SPICE result of 4inAO circuit with via_0025 open state indicated unstable behavior. Input logic (1110) indicates two different output values by "1" and "Middle-level".

6. Conclusion

The novel technology based on behavior analysis of Tr brings simple treatment, short operation times with 1/100 times of SPICE and accurate diagnosis result. This technique, quickly handled, is applied to assist a physical analysis for recent advanced LSI.
The technology has been improved to expression of oscillating phenomenon arising from defect, improvement of precise fault transformation and enlargement of circuit scale.

References

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