論 文 内 容 の 要 旨

Metal oxide thin-film transistors (TFTs) have attracted considerable attention for use in next-generation high-definition and large-area flat-panel displays (FPDs) due to their exceptional electrical properties, such as high mobility (>10 cm^2/Vs), large-area uniformity, and compatibility with low-temperature process. For reliability enhancement, a passivation layer is essential to protect the back channel of the TFT. A PE-CVD deposited passivation layer has many advantages over the others however; often the plasma introduce defects on the back channel of the In–Ga–Zn–O (IGZO) TFT. With the PE-CVD deposition condition such as deposition temperature, dilution ratio, and source gas chemistry strongly influence the back channel surface defects. The influence of PE-CVD source gas chemistry and deposition temperature of SiO_2 passivation on the IGZO back channel interface has extensively investigated in this work.

In addition to the interface defect, sputter IGZO suffer structural and electrical defects during sputtering. Thus, a thermal annealing step at around 300 °C, which is higher than the softening temperature of flexible plastic substrates, is commonly applied to repair the defects and achieve desired electrical properties for the TFTs. To obtain the superior oxide TFTs directly onto a plastic substrate, it is a great challenge to develop the defect passivation. In this study we report, a new technique to passive the IGZO bulk defect within the flexible substrate's softening temperature.

This thesis divided into two major parts. First part consist of chapter 2 to 5, is about the passivation layer and the interfacial processes at In–Ga–Zn–O surface on performance and reliability of the thin–film transistors. The second part presents, a novel technique for low temperature activation and defect reduction for amorphous oxide semiconductor (AOS).

Chapter 1 is an overview of the TFT technology and of material for TFTs. Among several materials, In–Ga–Zn–O (IGZO) shows enormous potential to use in high reliable display application. Since it shows TFT switching properties even deposited at room temperature, IGZO is a strong candidate for an active channel of flexible TFTs. The remained issues and their possible solution will describe briefly.

Chapter 2 discuss the influence of source gas chemistry in PE-CVD SiO_2 passivation on performance and reliability of IGZO TFTs. For the oxide TFTs, a passivation is an important processing requirement in order to improve TFT's reliability since the ambient species of oxygen and water adsorb on the oxide semiconductor surface, and affects the electrical properties and bias stress stability of the transistors. A plasma-enhanced chemical vapour deposition (PE-CVD) has high throughput with a large-area uniformity; however, plasma

damages including ion bombardment and hydrogen incorporation into the oxide semiconductor are known drawbacks. For the SiO_2 passivation deposition, silane (SiH_4) and nitrous oxide (N_2O) are widely used as source gases of PE-CVD. In the previous report, influences of the gas ratio of SiH_4–N_2O and the deposition temperature (T_D) of passivation SiO_2 on the electrical properties of oxide TFT have been investigated. Source gas of tetraethoxysilane (TEOS) and O_2 mixture is a safe alternative to explosive SiH_4 for PE-CVD SiO_2. Although, there are little reports of oxide TFTs with SiO_2 passivation deposited by PE-CVD using TEOS–O_2 as precursors. However, there are no systematic investigations of an influence of the source gas chemistry in PE-CVD SiO_2 passivation on the electrical properties and bias stress stability of bottom-gate oxide TFTs. First, the electrical properties and positive bias temperature stress (PBTS) stability of bottom-gate IGZO TFT with the PE-CVD SiO_2 passivation deposited using SiH_4–N_2O–N_2 (denoted hereafter as "SiH_4-SiO_2") and TEOS–O_2 gas chemistries were evaluated and compared. The electrical properties exhibited different tendencies between two gas chemistries with changing the T_D.

The transfer characteristics of the TFTs with SiH_4-SiO_2 passivation indicate the donor-type defect is mostly nearby the conduction band (E_c), in the other word those impurities are in shallow state. In contrast, the TFTs with TEOS-SiO_2 passivation showed different tendencies as compare to those with SiH_4-SiO_2 passivation. The on current of the TEOS-SiO_2 passivated TFTs are mostly identical, and the T_D influences the hump in sub-threshold region, suggests the defects created by TEOS-SiO_2 are mainly localized donor type defects. The plausible cause for the big change of transfer characteristics is explain by the difference in plasma dissociation and a surface reducing process between $SiH_4/N_2O/N_2$ and $TEOS/O_2$ gas chemistry.

In addition, the subthreshold swing (*S.S.*) degradation, which is occur in the TFTs with TEOS-SiO_2 passivation at a T_D of 310 °C or higher is explain by an electron injection barrier lowering. The *S.S.* degradation is correlate to the V_{th}-roll-off, which is usually observes due to a drain induced barrier lowering (DIBL). As the donor-like state form at a backchannel of the TFT during the TEOS-SiO_2 passivation, an electron injection barrier lowering at a source contact can explain the V_{th}-roll-off. Due to the donor-like defect, the Fermi level (E_F) at the back-channel will be pinned. The induce donor-like states reduce the electron injection barrier (E_{BB}). Because of the electron injection barrier lowering, carrier injection from source to channel contribute to generate the subthreshold leakage current in more negative gate voltage region even for very little drain voltage. Moreover, the source contact barrier lowering was confirmed by activation energy (E_a) of the TFT which was extracted using the Arrhenius model. In addition, it was revealed that a stacked SiO_2 passivation that is deposited at a different T_D is an effective technique to improve the performance and reliability of the IGZO TFT.

Chapter 3 elucidate a relationship between passivation film density and reliability of IGZO TFTs will.

Reliability under positive gate bias stress (PBS) of IGZO TFTs is of crucial importance for the practical application of the TFTs. It is known that the electron traps at a gate dielectric/channel interface is one of the main cause of a positive threshold voltage shift without sub threshold swing degradation under the PBS. In addition, ambient molecules have strong effects on the PBS reliability especially for the TFT without a passivation layer. Since a passivation layer is essential for improving the PBS reliability, many efforts have been made to understand the effects of the materials and deposition conditions of a passivation layer on the electrical properties and reliability of the IGZO TFTs. Till to date, there have been no research studies reported on the effect of the permeability of ambient molecules through the passivation layer on PBS reliability.

The effects of the film density of PE-CVD deposited SiO_2 passivation layer of IGZO TFTs, on PBS stability was investigated by a comparison of the results of the PBS test between ambient air and vacuum. The film density was varied by changing the SiO_2 deposition temperature. The SiO_2 passivation became dense as the deposition temperature increase. Subsequently, the PBS stability improved as the T_D increased. This result, suggests that the permeability of ambient molecules through the passivation layer decreased. To understand the mechanism of PBS improvement, the reliability was compared between ambient air and vacuum. Results indicate that the high film density of SiO_2 passivation layer effectively suppressed the diffusion of ambient molecules through passivation and improved the PBS reliability in air. Thus, a dense passivation is essential for reducing an ambient effect under PBS.

Chapter 4 discuss the effect of the TEOS/O_2 dilution ratio of SiO_2 passivation on performance of the IGZO TFTs. In previous studies, influences of the gas ratio of SiH_4/N_2O was investigated and reported that, almost all of the hydrogen diffused from the passivation layer, acts as shallow-donor in IGZO. In contrast, finding from chapter 2, suggests TEOS /O_2 plasma generate hydroxyl (i.e. OH, H_2O) which also influence the electrical properties of IGZO TFT. Experimental results shows that with increase the oxygen partial pressure of TEOS /O_2 the TFT exhibit better characteristics with good *S.S.* and positive turn on voltage. Suggest that the oxygen radicals and or -OH reduce the weakly-bonded oxygen and trap states in the IGZO channel, result in improving the *S.S.*.

Recently negative gate bias illumination stress (NBIS) is a serious issue for oxide TFTs. The enhancements of NBIS were observed due to photo-excitation of electrons from high-density electron traps existing in an IGZO at an energy level close to the valence band maximum (near-VBM state). The -OH groups in the film have been reported to relate the density of the near-VBM. Formation of OH- bonds in IGZO is an important factor to passivate the near-VBM state. Interestingly, the TFTs with higher oxygen partial pressure deposited SiO_2 passivation exhibit excellent NBIS stability. The XPS analysis uncovers an increase of M-OH bonds in the IGZO-bulk, those who was passivated by a SiO_2 of high oxygen partial

pressure. This implies a possibility of NBIS suppression by TEOS/O_2 based SiO_2.

The second part is focusing on the defect reduction and processing of AOS TFTs for the flexible electronics. Chapter 5 introduce a new discovery and invention for low temperature activation and defect reduction for oxide semiconductor. AOS TFTs are very promising for flexible devices because the oxide semiconductor channel can be deposited by sputtering at room temperature. However, during the AOS sputtering process, various types of high-energy particles, such as recoil argon and oxygen ions, are incident on the film, which results in structural and electrical defects. Thus, a thermal annealing step at around 300 °C, which is higher than the softening temperature of flexible plastic substrates, is commonly applied to reduce the defects and achieve desired electrical properties for the TFTs. This annealing step is often referred to "activation annealing" of the TFT. To obtain the superior oxide TFTs directly onto a plastic substrate, it is a great challenge to develop the defect passivation and/or low-temperature activation methods below softening temperature of the plastics (150–200 °C).

In the previous reports, several approaches such as wet O_2 annealing, simultaneous ultraviolet and thermal treatment, high-pressure gas annealing, electric-field-aided activation, and plasma treatment have been proposed for low-temperature activation of the oxide TFTs. However, none of them are in situ type, which bring the extra cost for TFTs fabrication. This work reveals that an additive gas during film formation is effective for low temperature activation process, which has never been reported.

Conventionally, the IGZO films are sputter by using $Ar+O_2$ gas where the carrier density control by the oxygen partial pressure R(O2). However, a low temperature annealed TFT exhibit huge hump, indicates defects remain in the IGZO channel. In contrast, TFT properties were drastically improved after annealing at 150 °C by the $Ar+O_2+H_2$ sputtering. XPS and TDS analysis clearly indicates large amount of the presence –OH bonds in the $Ar+O_2+H_2$ sputter films compare to $Ar+O_2$. . In addition to the activation process development this chapter also discusses about the photosensitivity, NBIS, PBS of the $Ar+O_2+H_2$ sputter IGZO TFTs alongside physical and electrical characterization of the films.

Chapter 6 demonstrates a high K gate dielectric for low temperature fabrication process. Polymer foils such as polyethylene naphthalate (PEN) which are preferable for flexible electronics application offer a low temperature (~ 160 °C) budge. Previous chapter reveals a promising process for low temperature IGZO channel formation. However, the maximum process temperature often limited by the gate insulator. For example, the most common gate insulator, which is PE-CVD deposited SiO_2, require a temperature of above 300 °C. Another important issue is the power consumption, which can be reduced by using a high K gate insulator. Nevertheless, most the reported high K gate insulator have critical drawback of being deposited by

costly and slow process like atomic layer deposition or a limited breakdown field. The introduced anodic aluminum oxide was grown at room temperature using ethylene glycol and ammonium tartrate with a current density of mA/cm^2. The aluminum oxide exhibited very high breakdown field of over 5 MV/cm and negligible roughness.

Chapter 7 summarize this thesis work and listed some suggestion for future work. Difficulties that need to be address are identified and possible solutions are proposed.